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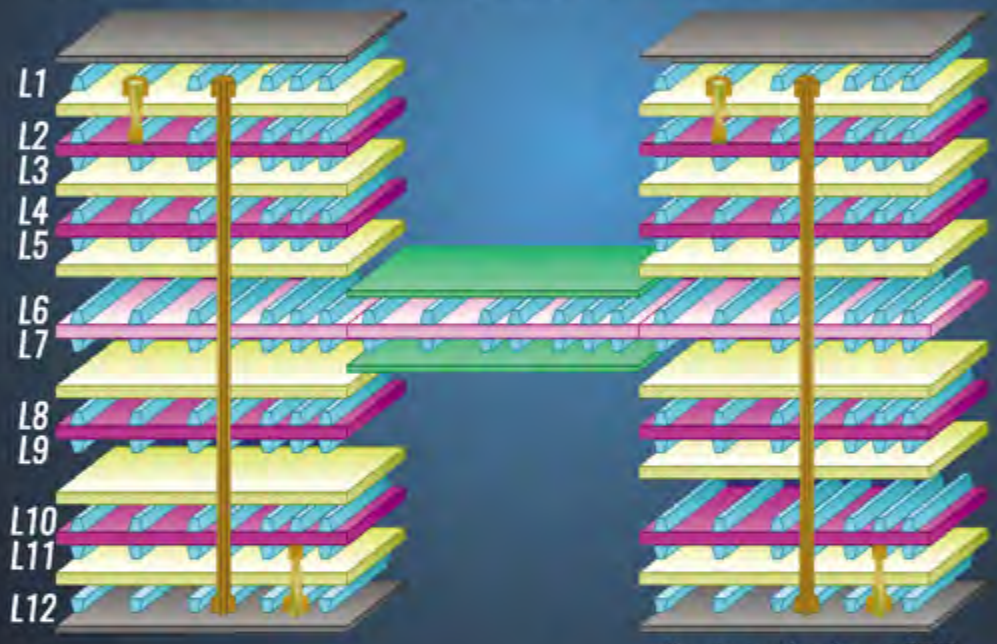

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FEATURES

THERMAL MANAGEMENT

The Heat is On
Thermal interface materials (TIM) are used between components to help with heat dissipation. Claire Wemp, Ph.D., a thermal applications engineer at DuPont, discusses the use of TIMs, as well as her involvement in the Society of Women Engineers.
by MIKE BUETOW

PACKAGING (COVER STORY)

A Plethora of Pitches
The evolution of integrated circuit package technology drove the electronics industry to its present state, but a closer look at the past reveals missed opportunities to create a more coherent set of IC standards, as well as lessons to be learned for future choices to improve design efficacy and product performance and reliability.
by JOSEPH FJELSTAD

INSPECTION

Selectively Assembling High-Value Components Based on Warpage in Order to Improve Reliability
Surface warpage, or flatness, is an established source of reliability issues in surface mount devices, particularly when these surfaces are considered as they warp due to heat generated in production or real-world use. While measuring samples for thermal warpage is a common practice, an experimental concept is presented based on measuring warpage on SMD devices and the PCB landing areas where they would attach in assembly, then deciding which sample to place on which PCB.
by NEIL HUBBLE and CHANCE RABUN

LEGISLATION

Public Sector Efforts 'Chip Away' at PCB Funding Deficit
The PCBAA is ramping up efforts to secure funding for R&D and capacity in the US. PCBAA executive director David Schild explains.
by MIKE BUETOW

ON PCB CHAT (PCBCHAT.COM)

PCB Chat

EDA SOFTWARE MARKET UPDATE
with WALLY RHINES

THERMAL INTERFACE MATERIALS
with CLAIRE WEMP, PH.D.

HIGHLY ACCELERATED LIFE TESTING (HALT)
with DR. CHRISTOPHER JACKSON

US PCB INDUSTRY LEGISLATION UPDATE
with DAVID SCHILD

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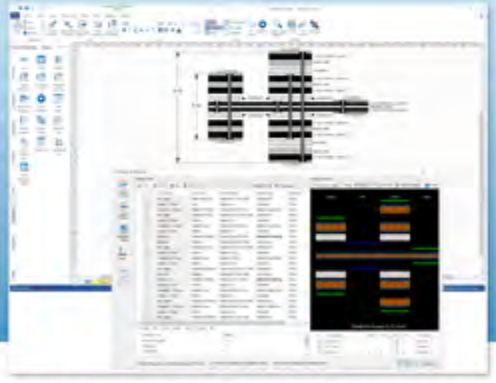

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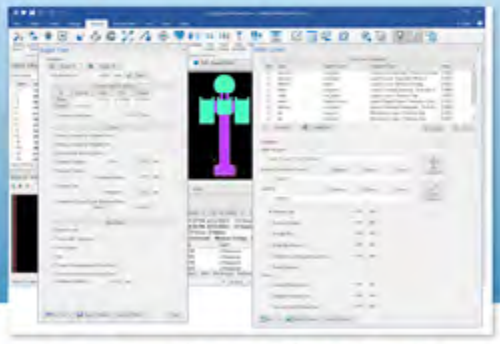
A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



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The ’80s Revival

IN A BLAST from the past, Marc Carter, one of the leading proponents of integrating electronics design and manufacturing technical skills into the educational system, shared a review of the Nepcon West trade show written by the LA Times … in 1986. The flashback is priceless.

Most readers won’t remember Nepcon, but it was the giant of that and any era when it came to electronics manufacturing. It would draw 30,000 to 40,000 engineers and other industry professionals to Anaheim, CA, each February to peruse the 1,000 or so exhibitors from all over the world. It was truly staggering.

The review Carter shared dwelled on surface mount equipment, which was just getting going in the US at the time. (Phil Marcoux, one of PCEA’s advisors, is credited with installing the first such line in the US while running an EMS called AWI in the early 1980s. One of the first SMT boards I’ve seen – or even know of – was used in the early Saturn rockets now on display at the US Space and Rocket Center in Huntsville, AL, and is featured on this month’s cover photo.) Most assembly process equipment then, however, was either through-hole or, if SMT, it was semiautomatic, a far cry from the robot- and software-intensive Industry 4.0-run factories in some regions today.

Per the article, about 10% of US manufacturers and 30% of their Japanese counterparts were using SMT at the time, with penetration in Europe nestled somewhere between the two regions.

Perhaps the most stunning change between then and now is the demographics. Attendees from offshore, including one quoted from Nan Ya, walked Nepcon looking for equipment not available in the Pac Rim. The US should be so lucky now.

One prescient manufacturer's representative said this: "The boom days (for electronics) are over. Opportunities are going to have to be sought out and developed." (Do you agree?)

Joe Fjelstad, he of more than 200 patents in flex circuits and packaging – and countless more pending – is one who continues to try to seek and develop those opportunities. I've been hearing the words "Fjelstad" and "guru" for so long, I was stunned when I learned he's not much older than me.

A few months back I challenged Fjelstad to consider what ideas were conceived and discarded years or decades ago but might be relevant today. He returned to us our cover story this month, which investigates the unstructured evolution of integrated circuit package technology – and its consequences.

The article is a few clicks away and I'm not going to summarize it here. Rather, it's the side conversations that led up to the contribution that I want to share.

Fjelstad's mind is comprehensive and frighteningly dynamic, and conversations with him inevitably wander into all sorts of unexpected and neat areas.

Among other things, we talked about the renaissance of polymer thick film, for instance, a technology some four-decades-old that the US government is investing tens of millions in today. And we covered the seismic geographical shifts that took place, in some cases almost by accident.

To wit: Back in the 1980s and early 1990s, the consensus was Japan's investments in miniaturization coupled with its patience and long-range strategic thinking (remember the 100-year plan?) and superior marketing skills were going to dominate the electronics industry forever. Never underestimate those key decision points. Japan missed on array packaging, opening the door to geographical competition. (I should mention, the US and European bare board industries did something similar in the late 1990s and early 2000s, focusing almost exclusively on high-layer-count boards at the expense of HDI. And while it's understandable why they did so at the time – order backlogs were pushing nine to 12 months – in retrospect that was a very big miss.)

One of the side effects of economic recessions and the race to lower-cost builds is the loss of a few more of the (already few) remaining seers. "We lose the dreamers, the imagination," Fjelstad says.

We contemplated this ongoing conundrum of the industry today, which is that we are surrounded by great engineers, but they are tasked with improving what already exists.

So many new inventions come from outside the industry and get adapted for ours. As Fjelstad says, engineers today aren't given the freedom and challenge to ask, "How do I make this disappear in favor of something that doesn't even exist?"

We are ready for a new generation of architects, but where are they and, more importantly, who are they?

Assuming, of course, they are human and not ChatGPT-driven, we need look no further than our own conference and exhibition, PCB West, which takes place next month at the Santa Clara (CA) Convention Center. Our free sessions on Sept. 20, the same day as the exhibition, include presentations on developments that are expected within the next three years and their projected impact on the hardware and PCB engineering. These include development/convergence of AI, regenerative design, Mod-Sim and model-based systems engineering (MSBE). We could be on the cusp of a world with no netlists, highly automated data search and automated routing development that were the stuff of daydreams just a few years ago.

Nepcon West might be gone and (almost) forgotten, but the opportunities to be sought out and developed are staring right at us. Don't miss them.

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MIKE BUETOW is president of PCEA (~~pcea.net)~~; mike@pcea.net.

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American Standard Circuits Acquires Sunstone Circuits

WEST CHICAGO, IL – American Standard Circuits and Sunstone Circuits in July announced a merger of their respective printed circuit board fabrication operations.

Terms of the deal between the two privately held manufacturers were not disclosed, but all current operations will be maintained, the companies said. Matt Stevenson, who has been with Sunstone more than 17 years, has been named vice president and general manager of the merged entity, ASC Sunstone Circuits.

In a statement, the companies called the deal a "strategic alliance [that] brings numerous advantages to customers."

"Together, we bring an unmatched combination of expertise, capabilities and resources to our customers," said Anaya Vardya, CEO, American Standard Circuits, in a statement. "This merger will enable us to deliver greater value, innovation and responsiveness, solidifying our position as the premier PCB manufacturing partner."

The combined firms will offer a broad range of PCB types, materials, and certifications, including single-sided, double-sided, multilayer, RF/microwave, flex/rigid-flex, HDI, ultra HDI, and metal-backed boards.

Sunstone Circuits will continue to offer its quickturn prototype and low-volume services, while ASC, which has multiple operations, provides higher-volume runs.

"The acquisition is complementary," Vardya elaborated in an interview with PCD&F/CIRCUITS

ASSEMBLY. “Sunstone does a lot of quickturn. ASC has many outlets for the follow-on production,” citing facilities in West Chicago and overseas.

There is “virtually no overlap of customers,” he added.

The addition of Sunstone, which is capable of accelerated prototyping (24-48hr.) and operates outside Portland, OR, gives ASC factories in the US Central and Pacific time zones, plus overseas.

Sunstone will maintain its dynamic online PCB quoting options and automated front-end design and engineering tools. Customers now have access to a comprehensive and user-friendly design software solution that includes powerful tools for schematic capture, PCB layout and integrated parts library, the companies said.

Sunstone’s longstanding relationship with Screaming Circuits will continue post-merger, while its customers will now have access to ASC’s global sourcing division and network of partners and suppliers of components, materials, and manufacturing services from various locations globally.

“We have customers that require a total solution,” Vardya said. “We always wanted to be a total solution for customers.”

Terry Heilman, CEO, Sunstone Circuits, added: “This merger represents a transformative opportunity for our customers. By leveraging the strengths of both companies, we are positioned to provide a comprehensive range of PCB solutions and deliver unparalleled customer experiences. We are excited to embark on this journey together.”

Heilman and Sunstone Vice President and COO Rocky Catt will remain with the merged entity for an unspecified period.

One of the older PCB fabricators in the US, Mulino, OR-based Sunstone was founded in 1972 and has 104 employees. American Standard Circuits was founded in 1988.

Vardya said ASC will “continue to look” for other acquisitions. “Our plan is to grow organically and through acquisition. It’s one reason we aligned with private equity a few years ago.”

Ansys and Altium to Connect ECAD,

Simulation Tools

PITTSBURGH – Altium and Ansys are partnering to improve the electronic design and development process by digitally connecting Altium's electronic computer-aided design (ECAD) tools and Ansys Electronics Desktop.

The integration, set to be available in the second half of 2023, is meant to create a new level of digital continuity while helping to reduce development time and the risk of design errors, the companies said in a release.

The companies said the connection will facilitate seamless collaboration, streamlining the exchange of design data and enabling engineers to work together more effectively within a fully integrated workflow. By eliminating the need for import/export translations and replacing manual, ad-hoc communication methods, the integration supports predictive accuracy, synchronization, and productivity, while reducing the risk of errors. As a result, the digital bridge also minimizes the potential for respins and delays.

"As companies innovate to meet the demand of today's competitive landscape, they face new product complexities and engineering challenges that require extensive cross-domain collaboration and advanced simulations. And the outdated, manual integration methods being utilized are holding them back," said Tomek Brzuchacz, head of CAD software at Altium. "This digital connection between ECAD and simulation enables electrical engineers and simulation engineers to work together with ease and accuracy, helping companies to accelerate design time and minimize additional costs."

"Electronics designers and engineers work tirelessly to produce the countless connected devices and applications demanded by today's market, and it is critical to equip these innovators with the same level of connectivity during design and development," said John Lee, vice president of the electronics, semiconductor and optics business unit at Ansys. "With a bidirectional link between Ansys and Altium solutions, electrical engineers will no longer be slowed down or interrupted by data communication and can focus on design, innovation and collaboration."

SEL Hosts Ribbon-Cutting for New PCB

Factory

MOSCOW, ID – Schweitzer Engineering Laboratories hosted a ribbon-cutting ceremony for its new printed circuit board factory here on Jun. 28.

The 162,000 sq. ft. facility houses the operation to fabricate the printed circuit boards used in its products that protect, monitor, control and automate electric power systems around the world. The facility is expected to employ around 60 people, with positions ranging from a variety of engineering roles, including chemical, mechanical, software and computer-aided manufacturing to equipment operators and maintenance workers.

Construction on the facility began in spring 2021.

ECIA Releases New Component Training Modules

ATLANTA – ECIA Foundation announced the release of the second stage of its e-learning modules for teaching the basics of the electronic components industry to new employees.

Phase II of the members-only PACE training program consists of five new courses covering the following topics:

- Supply Chain Management: The Hidden Value of Distributors
- Establishing the Distribution Strategy: Supplier Needs vs. Customer Wants
- CRM, ERP and More: The Platforms Powering the Digital Supply Chain
- Demystifying Sales: Pricing, Roles and More
- Driving the Future with Electronics: Evolving Industries and Applications

ECIA developed the introductory five courses and an interactive platform with Lectrix Group, a sales strategy and marketing group. Since its launch in May 2022, the program has seen more than 1,000 learners and received positive reviews.

“The response to this program has far exceeded our expectations,” said David Loftus, president and CEO, ECIA. “It was intended to capture and underline the importance of the channel to the broader tech industry. This curriculum provides the next generation of electronic component industry champions a baseline working knowledge of our industry, and that will help attract and retain the talent that is so essential to our member companies.”

Phase I courses cover the basics of the electronic component channel and includes these topics:

- An Introduction to the Electronics Industry: Manufacturers, Independent Manufacturers’ Representatives, and Distributors
- The Supporting Industry Partners
- Taking a Product to Market: How a Component Manufacturer Launches a New Product
- An Introduction to Basic Electronic Components
- Electronics Industry Terms and Conditions

Member companies can gain access to the training by creating a profile on the ECIA website and then visiting ecianow.org/PACE.

US Outlines CHIPS Act Funding Opportunities

WASHINGTON – The US Department of Commerce in late June announced an expansion in funding opportunities for large semiconductor supply chain projects, as well as a separate process for smaller projects coming later in the year.

As part of the CHIPS and Science Act, the Department of Commerce is overseeing more than $50 billion to revitalize the US semiconductor industry, including $39 billion in semiconductor manufacturing incentives. The first funding opportunity seeks applications for projects to construct, expand or modernize commercial facilities that produce leading-edge, current-generation and mature-node semiconductors.

This same funding opportunity is now open to materials and manufacturing equipment facility

projects with capital investments equal to or exceeding $300 million.

Large-scale supply chain projects that are now eligible will follow the five-part application process laid out in the first funding opportunity: statement of interest, pre-application (optional but recommended), full application, due diligence and award preparation and issuance. Applicants will be evaluated based primarily on the extent to which the application addresses the program's economic and national security objectives, but they will also be evaluated based on commercial viability, financial strength, project technical feasibility and readiness, workforce development, and broader impacts.

An additional funding opportunity will be released in the fall for supplier projects below the $300 million threshold with a tailored application that smaller businesses can navigate.

"After the pandemic exposed holes and bottlenecks in our semiconductor supply chains that sent shockwaves across our economy, the CHIPS and Science Act is a historic opportunity to ensure our microchip supply chain resilience," said US Secretary of Commerce Gina Raimondo. "Thanks to President Biden's Investing in America agenda, we're already seeing billions in private sector investment bolster the semiconductor supply chain. We're laying out our vision for how we'll build on that progress by responsibly making investments to ensure resiliency and success for the clusters we will create."

Alongside the funding opportunity for larger supply chain projects, the Commerce Department also released a "Vision for Success" outlining strategic objectives for investments in the semiconductor supply chain. The goals in the vision paper include: 1) strengthening supply chain resilience, including by reducing chokepoint risks flowing from the geographic concentration of critical semiconductor inputs; 2) advancing US technology leadership, including by incentivizing major US manufacturing equipment and materials suppliers to increase their footprints in the United States and attracting non-US suppliers of the world's most advanced equipment, materials, and subsystems to establish large-scale footprints in the US; and 3) supporting vibrant US fab clusters, including by ensuring that each CHIPS-funded cluster is supported by an ecosystem of reliable suppliers.

Arkema to Acquire Controlling Stake in PIAM

COLOMBES, FRANCE – Arkema will acquire a 54% stake in South Korean polyimide film producer PI Advanced Materials for €728 million ($791 million).

PIAM had sales of more than €200 million in 2022, and expects sales to grow 13% per year, driven by demand for polyimide in lithium-ion batteries, 5G antennas, high-resolution OLED displays or flexible screens, and supported by recent capacity expansions.

The transaction will be fully financed in cash, and after approval by Chinese and Korean antitrust authorities, should be finalized by the end of 2023, Arkema said.

"PIAM is an outstanding company with a unique technological positioning, state-of-the-art manufacturing facilities and invaluable customer relationships," said Thierry Le Henaff, chairman and CEO, Arkema. "This acquisition is fully aligned with our strategy to be at the forefront of high-performance materials for high growth end markets supported by megatrends such as electric vehicles and advanced electronics.

"After the divestment of PMMA, the acquisition of Ashland adhesives and the current start-up of our bio PA11 plant in Singapore, Arkema is delivering another significant milestone of its strategy focused on innovative materials for a sustainable world," said Le Henaff.

With two production sites and two R&D centers in South Korea, PIAM employs approximately 320 people.

NI Stockholders Approve $8B Emerson Merger

AUSTIN, TX – National Instruments stockholders approved the company's acquisition by Emerson Electric during a special meeting in June, with stockholders receiving $60 per share in cash for every share of NI common stock they own.

The $8.2 billion merger agreement was first announced by Emerson earlier this April.

"Today's vote by our stockholders validates our belief that this transaction represents the best outcome for all NI stakeholders," said Eric Starkloff, CEO, NI. "We thank our stockholders for their support and look forward to accelerating our position as a leading provider of software-connected

automated test and measurement systems in this next chapter as part of Emerson."

The proposed transaction is expected to close in the first half of Emerson's fiscal year 2024, subject to the completion of customary closing conditions.

Technoprobe to Acquire Harbor Electronics

MERATE, ITALY – Technoprobe, an Italian manufacturer of chip testing solutions, signed a binding offer in July to acquire California-based PCB maker Harbor Electronics.

Under the terms of the offer, which includes a 30-day exclusivity period to finalize and sign the final acquisition agreement, Technoprobe will pay around $50 million net of any adjustments related to changes in the target company's cash holdings.

Harbor Electronics, founded in the 1980s in Santa Clara, CA, and acquired in 2015 by the Shenzhen-headquartered Fastprint Circuit Tech group, is a manufacturer of advanced PCBs for testing systems for major semiconductor manufacturers. Last year, the company reported revenues of around $52 million, an EBITDA of about 16%, and a net financial position of about $5 million.

With the acquisition, Technoprobe will further strengthen its technological competencies in the testing area by vertically integrating its production process through the in-house production of advanced printed circuit boards for its probe cards and final test boards, the company said in a release.

"The acquisition of Harbor Electronics has an important strategic value because it allows us to consolidate the process of vertical integration of the production process of our probe cards by leveraging the significant technological synergies of two important players in the testing field," said Technoprobe CEO Stefano Felici. "In addition, the distinctive skills of Harbor Electronics will allow us to increase our knowledge in the final testing segment."

Amara Raja Electronics Acquires Stake in Design Alpha

CHITTOOR, INDIA – Amara Raja Electronics announced the acquisition of a stake in engineering design firm Design Alpha. The acquisition will position Amara Raja Electronics (AREL) as a fully integrated electronics systems design and manufacturing (ESDM) company, unlocking numerous opportunities in the electronics manufacturing business, the company said in a statement.

Based in Kochi, India, Design Alpha specializes in supporting deep science and engineering development by offering design expertise and services. AREL did not disclose the percentage of shares it acquired.

Besides opening doors to partnerships with large multinational corporations and expanding their customer base, the acquisition will also facilitate seamless integration of design and manufacturing processes, along with the provision of value-added services to enhance product performance, efficiency, and reduce time to market, the company said.

"The acquisition will accelerate product development for AREL and allow us to leverage specialist knowledge," said AREL director Vikramadithya Gourineni.

Congressman Visits Pro-Tech Interconnect Solutions

CHASKA, MN – PCB manufacturer Pro-Tech Interconnect Solutions recently hosted a tour of its facility here by Rep. Tom Emmer.

Pro-Tech's Chaska facility has 83 employees and manufactures PCBs for the military, aerospace, medical and commercial industries.

"Manufacturing products like chips and semiconductors here at home doesn't just provide good-paying jobs to Minnesotans. Investing in the production of this essential technology is important to our national security," Emmer said. "Thank you to the team at Pro-Tech for sharing their work with us."

"Pro-Tech Interconnect Solutions LLC is the only 100% woman-owned and operated "rigid" printed circuit board manufacturer in the USA," said Pro-Tech President Melanie Bera Anderson. "We build boards for the F-35 jet, medical implants and equipment, to commercial controls."

Pro-Tech was founded in 1968, and since 2018 has been operated by American Circuit Corp.

IPC: European Electronics Industry Needs Further Support from EU

BRUSSELS, BELGIUM – Key segments of the European electronics manufacturing industry face significant challenges and require more support, according to a new report from IPC.

The report says the recently enacted European Chips Act is a welcome step, but "the near singular focus" on the semiconductor industry "has obscured critically important segments of the electronics ecosystem," specifically printed circuit boards and electronic assembly, without which semiconductors cannot function.

Over the past 20 years, the European PCB sector experienced a steep decline, the report says, shrinking from approximately 20-30% of global production to just 2% today. Over this time, the EU has become "highly dependent on China," which now accounts for some 65% of total EU PCB requirements.

The EMS sector has experienced "solid" average annual growth in recent years, fueled by factory investment by large global companies and by the growth of the downstream markets the sector serves, including automotive, industrial, aerospace, defense, and healthcare. However, the EU imports roughly 90% of required EMS products and services.

The European Commission is continuing to examine vulnerabilities in its industrial supply chains. In June, the European Commission's Directorate General for Internal Market, Industry, Entrepreneurship and SMEs (DG GROW) hosted a meeting on electronics assembly and printed circuit board manufacturing with key industry stakeholders, including companies from the renewable energy, aerospace/defense, automotive, and industrial sectors. The structured dialogue was called on the heels of an IPC meeting in April that brought together leaders of government and industry to press for an EU strategy to strengthen silicon-to-systems innovation and manufacturing.

USI Opens Second Factory in Poland

KOBIERZYCE, POLAND – Universal Scientific Industrial inaugurated its second factory here in June, and expects to create up to 1,000 jobs once the facility is fully operational by the first quarter of 2024.

“This new plant will strengthen our manufacturing capabilities and enable us to meet the growing demand for electric vehicle and green energy solutions in the European market,” said senior vice president Brian Shih, USI.

USI is a subsidiary of ASE Technology and parent company of AsteelFlash.

“Today we are proud to create a milestone for USI/AsteelFlash customer service,” said Felix Timmermann, executive director of USI Poland and executive vice president of Asteelflash. “We are strengthening our readiness to support our customers’ manufacturing and relocation efforts and ensuring that we are doing the best we can for our customers. We are convinced that this new activity will unleash our potential here and will be the start of something big.”

“We hope that the presence of such an important investor for the industry as USI, and its direct association with the Taiwanese ASE Technology, will attract new investments in Poland and contribute to the development of the electronics and semiconductor industries, sectors for the Polish, European and global economies,” said Marcin Fabianowicz, head of direct investments in Poland as managing director of the Polish Investment and Trade Agency.

GPV to Open 3rd Factory in Slovakia

PIESTANY, SLOVAKIA – GPV has entered a lease agreement for a new electronics factory here near its two existing factories in Slovakia. The additional factory is expected to start production from early 2024.

The new factory comprises a total of 18,000 sq. m., and the company will initially use 11,000 sq. m. with the option to expand and use the additional space at a later stage if needed.

In a release announcing the move, GPV said customers have been requesting additional production capacity in Europe, and after GPV’s merger with Enics in October 2022, the company managed to expand production capacity to better accommodate customer needs in the short time while continuing to look for a possibility to establish additional production capacity in Europe.

“With the additional space in Slovakia, we will have an even stronger operational footprint in best-cost Europe. We have a strong pipeline driven by increased demand from satisfied customers and we have a strategic ambition to regionalize European demand also in the light of the ESG agendas. Furthermore, we experience a big appetite toward best-cost Europe from existing and new potential customers, who wish to be served close to their core markets,” said Bo Lybæk, CEO, GPV.

The company said the additional factory will strengthen its site profile to respond with the requirements from the European core regions, and it will pave the road to support growth in the coming years.

“We expect to be able to combine the strengths from our 19 existing operating business units to further increase our competitiveness in the high-mix EMS market. I look forward to following the process, and I see this as an important strategic step in strengthening our operational footprint to serve our customers even better,” Lybæk said.

Scientists Develop Technology to Quickly 3-D Print Flexible Smart Devices

SINGAPORE – Scientists from Nanyang Technological University, Panasonic and Singapore Center for 3-D Printing have developed a new multi-material printer using multi-wavelength high-power lasers for quick and easy 3-D printing of smart, flexible devices.

The multi-material printer works by utilizing varying wavelengths of laser, creating thermal and chemical reactions capable of transforming common carbon-based materials (polyimide and graphene oxide) into a new type of highly porous graphene. The resulting structure printed with this new graphene is not only light and conductive, but it can also be printed or coated onto flexible substrates like plastics, glass, gold and fabrics, creating flexible devices.

Electronic devices and components have traditionally been made of rigid materials such as metals, silicon, and ceramics, but there has been an increasing interest in the creation of flexible wearable electronics that can be bent, twisted, and easily conformed to various surfaces.

“Our project aims to find a way to 3-D print new materials like organic polymers and carbon-based materials like graphene, which has properties that allow them to be printed or coated onto flexible

substrates like plastics or fabrics, creating flexible and stretchable circuits," said project co-leader Murukeshan Vadakke Matham, an associate professor from NTU School of Mechanical and Aerospace Engineering (MAE) and SC3DP, the national center of excellence in 3-D printing housed at NTU.

"3-D printed flexible electronics paves the way for more comfortable and mobile wearable devices as it can be lighter and smaller," added Murukeshan, who is also principal investigator at Singapore's National Additive Manufacturing Innovation Cluster (NAMIC). "We can now create unique structures that were previously impossible with traditional rigid electronics."

The newly created 3-D printer has already attracted interest from various companies, including American multinational manufacturer Jabil-MTI Penang.

Jabil-MTI Penang aims to integrate 3-D printed graphene-based electronics into a smart infusion system. A proof of concept has been demonstrated through a prototype of a low-cost intravenous (IV) fluid bag with an embedded printed sensor powered by artificial intelligence. The device monitors the status of the IV drip, regulates parameters such as pressure flow and temperature, and transmits the information to a smartphone in real-time. This allows medical personnel to remotely monitor, control and detect abnormalities efficiently.

The research team also tested the possibility of integrating 3-D printed components into the fabrication of high-performing electronics like pressure sensors and heaters.

"We greatly value NTU and Panasonic teams' creative thinking and innovative approach, and we are excited about the possibilities for future collaborations," said Jabil-MTI Penang project manager Lim Lai Ming. "We eagerly look forward to exploring further opportunities to work together and leverage both their teams' exceptional innovation expertise."

"Our technology allows the creation of highly porous and conductive graphene-based material for use in different applications," said project co-leader Dr. Low Mun Ji, general manager of Panasonic. "Compared to traditional graphene manufacturing methods, our method is faster, cheaper, and highly compatible with a wide range of materials."

Incap Acquires US-based Pennatronics

HELSINKI – Incap has gained a foothold in the US with the acquisition of the Pennsylvania-based EMS company Pennatronics in a cash and stock transaction.

The enterprise value of the acquired company is $18.6 million, and the agreement also includes a potential additional earn-out of a maximum of $3 million. The transaction will be paid in cash except for the amount of approximately $1.6 million which will be paid in Incap's shares.

Pennatronics has 102 employees working out of a 6,000 sq. m. production facility near Pittsburgh, PA, and offers complete electronics manufacturing services including PCB assembly and box-build assembly, as well as engineering and sourcing services. The company saw $30 million in revenue in its last financial year, and its EBITDA was $2.9 million.

Incap said the acquisition is in line with its growth strategy and will establish Incap's presence in the US market and create a foothold for further expansion in the country. Pennatronics' US production facility complements Incap's current production facilities located in Estonia, India, the UK and Slovakia.

The company said the acquisition will broaden Incap's customer base and will allow for US-based services to be offered to existing and new customers while Pennatronics' customers will benefit from opportunities to source services from Europe and India, and in the long term, the acquisition is expected to bring cross-selling opportunities and synergy benefits.

"I am very excited about widening our geographic presence and gaining foothold in the US market," said Incap CEO Otto Pukk. "I am also very happy to welcome the Pennatronics team of 102 professionals onboard. The acquisition will benefit both companies' existing customers with opportunities to source from new areas and I am convinced that, together with Pennatronics, we can create new opportunities to expand our business in line with our growth strategy."

After the acquisition, the former owners of Pennatronics, Ralph B. Andy and Keith D. James, are committed to support Incap over the transition period.

"I am enthused about the opportunity for our seasoned management team and dedicated employees to join forces with Incap," said Andy, who serves as president and CEO. "The Pennatronics team is excited to become Incap's first factory and cornerstone facility in the US to help fuel their future growth. This combination will enable us to take our business to the next level and provide our customers with enhanced capabilities and even greater value. I wish Incap North America a

successful future as they expand their production footprint into the US.”

Note Grows in UK With DVR Acquisition

STOCKHOLM – Note has expanded its manufacturing capacity in the UK with the acquisition of electronics manufacturer DVR. The EMS company will pay GBP9 million ($11.4 million) in cash, plus potential earnouts of up to GBP3 million ($3.8 million) based on future growth and profitability targets.

DVR is located in Basildon, Essex, and the British EMS market, which corresponds to the Scandinavian market in size, is expected to have clearly higher growth than the European EMS market in general, Note said in a release announcing the acquisition. Through the addition of a fourth plant in England, the company said it gains greater coverage and becomes a larger player in the growing British EMS market.

“Our business continues to develop strongly, and we are now making our third acquisition in the past year. We are very excited that DVR will now become part of the Note Group,” said Note president and CEO Johannes Lind-Widestam. “The acquisition strengthens our position in the UK EMS market, which we strongly believe in and which is expected to have a strong growth in the coming years. DVR has a strong customer portfolio with exciting projects and we also see opportunities for synergies with our existing customers and suppliers. We look forward to continuing the profitable growth journey together with customers, staff and management at DVR.”

DVR offers PCB and box-build manufacturing, with a substantial number of its customers in the industrial and greentech segments. The company was founded by the Hellings family and has been run and developed most recently under the leadership of David Hellings, who will continue his role as CEO of the company. The company has around 95 employees.

“I have come to appreciate Note as a company that shares our core values of long-term customer relationships and high quality in what we do,” Hellings said. “We have many exciting customers and projects in our portfolio and see great advantages for both us and our customers to become part of a larger group and continue to develop our business together.”

Entech Expands in Australia and

Malaysia

ADELAIDE, AUSTRALIA – Entech Electronics will expand in its native Australia and add its first plant in Malaysia, the EMS firm announced.

Entech, a contract manufacturer offering PCB assembly, turnkey assembly, prototyping, and bare PCB supply, has begun construction of a new Adelaide factory and HQ, with an anticipated move-in date of April 2024. The factory is being built on a 10,000 sq. m. site, with 4,500 sq. m. under cover, said Wayne Hoffman, CEO, Entech Group.

"It is a significant factory here in Adelaide … with the capability to take our factory floor space to double what it is at the moment," he said.

The company said that continuous improvement, growth, and a focus on the global supply chain of electronics components and materials has also set the stage for its third manufacturing location and further expansion into Southeast Asia.

The company has a factory in Shenzhen, and has operated a Singapore supply hub for the past three years, reaching out to businesses in Malaysia in preparation for its latest overseas expansion.

Hoffman said the new Malaysian operation would feature "glue and screw operations" but also the full supply chain of plastics, metalwork, hardware, wiring and harnessing through to finished product.

Critical Manufacturing Expands Operations into Mexico

PORTO, PORTUGAL – Critical Manufacturing has announced an expansion into Mexico to help meet the growing demands of American manufacturing systems. The new facility will serve as a strategic hub, fostering collaboration and innovation within the local manufacturing ecosystem, the company said.

As part of the expansion, the company named Juan Ledezma, an industry professional with a deep understanding of the Latin American market, general manager of Mexico.

“Our expansion into Mexico marks a significant milestone for Critical Manufacturing,” said Francisco Almada Lobo, CEO and cofounder. “With our strong foundation and a visionary leader like Juan Ledezma at the helm, we are poised to provide unparalleled support to our customers in Latin America and nearshore projects. We are excited to embark on this new chapter and contribute to the region’s manufacturing excellence.”

The ASMPT subsidiary provides a fully integrated, modular MES. The company said its decision to invest in Mexico aligns with its broader strategy of expanding its global footprint and fostering digitalization across international markets, and its commitment to providing localized support and expertise will enable Mexican manufacturers to accelerate their digital transformation journeys and achieve operational excellence.

“I am honored to lead the Mexico operations of Critical Manufacturing and contribute to the growth of the Latin American manufacturing industry,” Ledezma said. “Our mission is to empower organizations to embrace digital transformation and realize the full potential of their manufacturing processes. We look forward to partnering with local businesses, driving innovation, and supporting our customers’ success in this dynamic and evolving business environment.”

CMS Electronics Establishes Prototype-Focused Subsidiary

KLAGENFURT, AUSTRIA – CMS Electronics announced the expansion of its product portfolio with the establishment of a new subsidiary, PCBWhiz.

PCBWhiz utilizes an AI-assisted platform that provides instant quoting for prototype production. The software automatically analyzes specifications and extracts key technical parameters through its advanced algorithm. This enables immediate matching with the technical capabilities of production, as well as real-time checks on material availability and automated pricing of prototypes. Customers are presented with technical queries or alternative suggestions for components if material availability is insufficient, ensuring a seamless order process and timely initiation of production, and the price remains unchanged after the order is placed.

With the option to choose production locations in Europe or Asia (soon expanding to South America and Southeast Asia), PCBWhiz said it prioritizes data security and protection. All customer

data generated through the platform is securely stored in Frankfurt, Germany, ensuring compliance with ISO27001 (Information Security Management System) and GDPR regulations.

“Our aim is to revolutionize prototype production through flexibility and applied technology/system in processing,” said director Markus Quendler. “Our platform empowers customers to perform design for manufacturability (DfM) checks on their PCBs and analyze the bill of materials (BoM) for material availability and lifecycle status online 24/7 before placing an order.”

CMS Electronics said the new subsidiary allows customers to benefit from the combined strengths of both companies and gain access to world-class prototyping solutions. The company said the move underscores its commitment to innovation and ensuring customers have access to the latest and most efficient technologies.

Katek Completes Acquisition of Nextek

MUNICH – Katek SE announced that it has finalized the acquisition of Madison, AL-based electronics supplier Nextek. The acquisition, which was first announced last November, expands Katek’s presence in North America and strengthens its industry presence in the fast-growing areas of homeland security and defense, medical technology, energy, high-end industrial, and aerospace, which is new for Katek, the company said in a release.

With around 160 employees and annual sales of more than $43 million in 2022, Nextek is a developer of highly complex products for critical application areas, especially in the areas of prototyping and production of small to medium quantities and complements Katek Canada (formerly SigmaPoint) as a high-volume provider of complex electronics. Both companies benefit from the reshoring trend in North America, which is progressing massively due to the current economic and geopolitical tensions, Katek said.

In addition to quickturn prototype manufacturing, Nextek offers sophisticated PCBA and complete device construction (box-build) as well as analytical engineering, product engineering and extensive test services for its customers. Nextek is ISO 9001 certified and has obtained certifications and approvals in the field of aviation (AS 9100D), medical technology (ISO 13485) and military technology (ITAR registered), and has laboratory facilities for material testing and ensuring the required quality in critical application areas.

“The acquisition of Nextek is already our second pillar in North America. It not only enables us to serve our European customers local-to-local directly in the USA, but also opens up the opportunity for Katek to benefit from the generally strong growth trend in North America,” said Katek CEO Rainer Koppitz. “With the relocation from Asia and the high investments in North America as well as in connection with the ‘Inflation Reduction Act’ of the American government, we are well positioned to achieve success. Nextek ideally complements our existing location in Canada in the field of high-value electronics and is already very profitable.”

“Nextek is thrilled to be part of the Katek Group. We anticipate a successful integration and a bright future with great growth opportunities as part of Katek,” said Nextek CEO John Roberts. “We look forward with excitement to tapping into the anticipated additional business potential on both sides of the Atlantic. Combined with the strength and capabilities of Katek Canada, we at Nextek see a very promising future for Katek in North America. The entire Nextek team can’t wait to take the next steps together with Katek as part of ‘TeamBlue.’”

Kurtz Ersa Breaks Ground on Mexico Facility

JUÁREZ, MEXICO – Kurtz Ersa has broken ground on a new production facility here to meet the growing demands of the North America market.

The new plant will play a pivotal role in the production of Ersa soldering machines and will also serve as a preproduction center for Kurtz´s US factory, the company said in a release. The expansion will create Kurtz Ersa´s third-largest manufacturing site after Germany and China and will initially focus on manufacturing Ersa Hotflow reflow soldering systems.

“Mexico was chosen as the ideal location for this expansion due to its strategic advantages,” said Albrecht Beck, Kurtz Ersa president and COO. “Its central location on the border provides excellent access and facilitates access to strong local markets in the Americas. Additionally, Mexico boasts a wealth of highly educated and motivated workforce to maintain our high German quality standards at a modern state-of-the-art factory.”

With Kurtz Ersa’s rapid growth in the Americas, the new production facility in Chihuahua will better serve local customers, minimize its CO_2 footprint, shorten delivery times and reduce freight

costs, the company said.

The new production plant is expected to commence operations by spring 2024, and will join the company's existing service and logistics hubs in Plymouth, WI, and Guadalajara as its third major service and logistics hub in the region.

Otis Worldwide Opens PCB Production Center

BERLIN – Otis Worldwide has opened a new €8 million ($9 million) PCB production facility dedicated to advanced and complex PCB designs, as well as rapid prototyping and industrialization.

With the new production center, located in its SSI1 Electronics Berlin factory, Otis said it is building on the expertise of its Berlin-based teams in the design and production of PCBs, a field of growing strategic importance for many industries.

Otis' PCBs are used in elevators and escalators around the world, and around 75% of the equipment manufactured in Berlin is destined for European construction projects, as well as the modernization market. The remaining 25% is exported overseas.

SIA Calls for Halt on China Chip Restrictions

WASHINGTON – The Semiconductor Industry Association has called on the US government to refrain from any more restrictions on chip sales to China, saying additional measures against the country could disrupt supply chains and prompt continued retaliation from China.

"Recognizing that strong economic and national security require a strong U.S. semiconductor industry, leaders in Washington took bold and historic action last year to enact the CHIPS and Science Act to strengthen our industry's global competitiveness and de-risk supply chains," the SIA said in a statement released in mid-July. "Allowing the industry to have continued access to the China market, the world's largest commercial market for commodity semiconductors, is important to avoid undermining the positive impact of this effort. Repeated steps, however, to impose overly

broad, ambiguous, and at times unilateral restrictions risk diminishing the U.S. semiconductor industry's competitiveness, disrupting supply chains, causing significant market uncertainty, and prompting continued escalatory retaliation by China.

"We call on both governments to ease tensions and seek solutions through dialogue, not further escalation. And we urge the administration to refrain from further restrictions until it engages more extensively with industry and experts to assess the impact of current and potential restrictions to determine whether they are narrow and clearly defined, consistently applied, and fully coordinated with allies."

Tempo Automation Lays Off Nearly All Employees

SAN FRANCISCO – Tempo Automation in late July laid off 62 of its employees, leaving only seven employees on its payroll in an effort to reduce overhead and keep the company operational, according to an SEC filing.

CEO Joy Weiss and Ralph Richart, Tempo Automation's chief technology and manufacturing officer, are remaining with the company but will cut their base salaries by 50% for the foreseeable future. The company's chief financial officer, Ryan Benton, has resigned.

The company is trying to reduce overhead to better position the company to fund its planned operations while meeting obligations as they come due. Tempo has "experienced negative cash flows since inception that raise substantial doubt about the company's ability to continue," the filing said. The company lost $7.4 million in the first quarter on revenue of $2.8 million.

The company said it is working to identify alternative sources of capital and means of reducing expenses that may permit it to continue, including raising debt or equity capital and other alternatives, but there is no guarantee that it will be able to raise additional capital, or that the plan of termination and related workforce reduction will be sufficient to permit the company to continue operations.

Tempo Automation went public in November through a special-purpose acquisition company deal with South Korean firm Ace Convergence Equity Partners that was worth around $100 million.

Earlier in the month, the firm Tempo Automation executed a $7 million promissory note with Asia-IO Advanced Manufacturing Partners to finalize the previously announced acquisition of Optimum Design Associates.

PCD&F

Aohong Electronics plans to spend up to 600 million yuan ($84 million) on a new plant in Thailand that will build PCBs for export.

DuPont and **JetCool Technologies** announced a collaboration to increase adoption of advanced liquid cooling technology and introduce a new sales channel that brings JetCool's advanced cooling solutions to semiconductor companies in Taiwan and Singapore.

Eltek will receive an additional $2 million from its insurance carrier to cover costs and damages from a fire at its PCB plant in June 2022. The fabricator has repaid the balance of its $1.7 million bank debt and is accelerating investments in production equipment.

FTG Circuits Toronto earned qualification for IPC-1791, Qualified Manufacturers Listing.

Huatong chairman Jiang Peikun said operations are expected to gradually improve in the latter half of the year, primarily driven by AI and electric vehicles.

Insulectro will become exclusive distributor of **Arlon** copper-clad laminates for North America.

Meiko will reportedly develop the rigid and flex PCBs required for **Samsung's** Galaxy Ring.

Nan Ya will invest up to 700 million yuan to build a new copper-clad laminate and adhesive sheet production base in Thailand.

Nano Dimension sold a DragonFly IV system to the **University of Stuttgart** and signed an agreement with a large multinational electronics company to leverage DeepCube's deep learning-based AI technology.

Renesas Electronics has standardized on **Altium** 365 PCB design software.

Rostelecom launched a new production line of PCBs and telecommunications equipment in St. Petersburg, Russia, as part of its JV with **Russian Telecommunications Technologies.**

Samsung Electro-Mechanics is finalizing preparations for the commissioning of its FC-BGA substrate factory in Vietnam.

Siemens Digital Industries Software will expand its collaboration with **Amazon Web Services** to help IC and electronics design customers leverage AWS's advanced cloud services.

TSMC has seen its capacity utilization rates for advanced processes below 7nm rebound slowly since June and is poised to embrace a new wave of chip demand growth in 2024.

Ventec announced a cooperative agreement with **Giga Solutions** to offer full workflow solutions to its global PCB and related industry customer base.

Yijia, a Taiwanese manufacturer of flexible boards for vehicles, plans to establish a new subsidiary in Vietnam.

CA

Adco Circuits purchased a **Hänel** Lean-Lift vertical storage system and **Scienscope** Reel

Smart incoming material station, installed a new robotic thermal adhesive dispenser, and launched ADCOproto.com – an online tool that provides instant component availability for uploaded BoMs.

Advantest and **Arizona State University** announced a collaboration with **NXP Semiconductors** to create a new test engineering course at ASU.

Assembly Solutions purchased two **Inovaxe** Smart Racks.

Avary Holding implemented **Blue Yonder's** supply planning solution.

Benchmark Electronics celebrated the grand reopening of its facility in Almelo, Netherlands.

BTU International signed a strategic partnership with **ANS-answer elektronik** as its reflow oven distributor in Germany.

Compal Electronics purchased a $30 million plot of land in Vietnam to build a new plant and expand production capacity.

Creation Technologies moved into a new 150,000 sq. ft. facility in Changzhou, China.

Dorigo Systems chose **CalcuQuote's** QuoteCQ RFQ Management System to upgrade its quote process.

Emerald EMS purchased an **Identco** ILP-45 label feeder.

Elista is investing Rs 350 crore ($42.7 million) in setting up two electronics goods and appliances manufacturing facilities in Kopparthi, India.

Foxconn called off a joint venture with **Stellantis** to design and sell high-end automotive chips. Its Texas-based subsidiary, **S&B Industries,** laid off 115 employees in late July.

Hentec Industries/RPS Automation expanded its distribution agreement with **BTU International** to include the Vector series of selective soldering systems.

Heraeus Electronics announced its participation in the EU-funded research project "ALL2GaN" (affordable smart GaN IC solutions for greener applications).

Hisense Middle East signed an MoU with **Condor Electronics** to manufacture and assemble consumer electronics in the Middle East and North Africa region.

Incap Slovakia expanded its production area by 1,200 sq. m. due to increasing volumes of customers.

Jabil and **Napatech** have collaborated on a server platform for high-bandwidth, low-latency, financial technology applications.

MacDermid Alpha announced a partnership with **Amza** for distribution and sales across Israel, Gaza, and the West Bank area.

NeoTech installed new automated production and inspection robots to enable a higher level of performance and improve efficiency.

Orbit International's Simulator Product Solutions subsidiary received a new contract valued at more than $2.5 million.

Scanfil expanded its Malmö, Sweden, factory by 2,000 sq. ft.

Seho North America named **Lean Stream** technical sales representative across northern California and Nevada.

Segue Manufacturing Services expanded its Boston manufacturing facility.

STP Group will install a **Hentec Industries/RPS Automation** Pulsar solderability testing system in France.

Surf-Tech purchased a **PVA** Delta 8 selective conformal coating machine.

USI is expanding its expertise and capabilities in the EV industry by integrating production of powertrain systems.

Weller Tools is now offering its Weller Web Communication Platform in EMEA (Europe, Middle East, and Africa) and rest of world.

White Horse Labs purchased a **Yxlon** Cougar Evo x-ray machine.

Wistron will aggressively advance its worldwide manufacturing deployments in response to geopolitical shifts, according to the company's chairman.

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PCD&F

ASC Sunstone Circuits promoted **Kevin Beattie** to production manager and **Matt Stevenson** to vice president and general manager.

Elec & Eltek (Thailand) named **Johnny Lye** senior manager.

Landis & Gyr named **Russ Pringle** ECAD admin/librarian.

Peters named **Britta and Benjamin Alfes** to its management team.

CA

August Electronics appointed **Tanya Korenda** CEO and **Paul Crawford** VP of business.

Benchmark Electronics appointed **David Valkanoff** executive vice president and chief operating officer.

Bentec hired **Gareth O'Flattery** as a technical sales engineer.

Brooks Automation appointed **Andrew Balderson** senior director, sales & marketing.

Data I/O appointed **Gerald Ng** vice president of finance.

Deswell Industries announced the passing of chairman **Richard P.H. Lau.**

East West Manufacturing promoted **Ray Cottrell** to vice president of business development.

Icape Group announced the resignation of CEO **Cyril Calvignac** and the appointment of chief marketing officer **Yann Duigou** as successor.

Incap appointed **David Spehar** managing director of US operations.

Kimball Electronics promoted **Steven Korn** to chief operating officer and appointed **Kathy Thomson** chief commercial officer.

Libra Industries promoted **Andrew Williams** to president and CEO.

MicroCare appointed **Venesia Hurtubise** VP of technology & compliance.

RED Semiconductor named **David Harold** head of business development.

STI Electronics hired **Tammy Bailey** as SMT material handler.

Tompkins Robotics named **Tony Villanova** vice president, PickPal Solutions.

ViTrox appointed **Carlos Ponce** business development director in Mexico.

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National News

PCB West to Feature Free Expert Advice Sessions

PEACHTREE CITY, GA – Experts in printed circuit design and manufacturing will be on hand at PCB West 2023 to answer attendee questions during the exhibition on Sept. 20, the Printed Circuit Engineering Association announced.

Among the industry experts who will be available are Rick Hartley (signal integrity and noise control), Susy Webb (design layout and routing), Nick Koop (flexible circuits), Stephen Chavez (PCB design), and Keven Coates (design for assembly).

PCB West will take place Sept. 19-22, 2023, at the Santa Clara (CA) Convention Center.

The experts will be available at scheduled times at the PCEA booth during the show hours of 10 a.m. to 6 p.m. Visit pcbwest.com to see the schedule and to register.

"Past attendees have asked for more time to network and get help, and our 'Ask the Experts' series with gurus in signal integrity, high-speed design, EMI, DfM, flex circuits and more is intended to do just that," said Mike Buetow, conference director, PCB West.

The help sessions are free to all expo attendees. Those who register for the exhibition will also have

access to more than 100 leading suppliers to the electronics design and manufacturing industry.

Booth Sales Open for PCB East 2024

PEACHTREE CITY, GA – The show floor is now open to all exhibitors for next year's PCB East conference and exhibition.

Exhibitors at PCB East 2023 were given a three-week window to reserve for the 2024 event. That exclusive registration ended Jul. 31. Starting Aug. 1, any company may register to exhibit.

The one-day exhibition takes place Jun. 5 at the Boxboro Regency in Boxborough, MA, while the four-day technical conference takes place Jun. 4-7.

"The show floor will be open for three weeks to the 2023 show exhibitors," said Frances Stewart, vice president of marketing and sales, PCEA. "Then we will open it to any companies that want access to the only event for the New England electronics design and manufacturing industry."

In its second year, PCB East 2023 exhibits registration rose 63% from 2022. In all, more than 60 leading suppliers of electronics design tools, manufacturers of bare boards and assemblies, and suppliers of fabrication and assembly equipment and materials exhibited at the show.

Companies interested in exhibiting may visit pcbeast.com or contact Stewart at frances@pcea.net for details.

Chapter News

Education committee. PCD&F is undertaking its annual salary survey of printed circuit board designers, design engineers and other layout specialists. Designers for years have taken advantage of the results to benchmark their salaries, benefits and credentials against their peers.

The survey link is https://www.surveymonkey.com/r/2023designersalary.

Results will be published in an upcoming issue. All data collected are revealed only in the aggregate. No individual data are revealed.

Because this is a survey, not a poll, the audience being surveyed is not selected or controlled.

PCD&F has conducted the annual survey of design engineers and printed circuit designers for more than 20 years.

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MARKET **WATCH**

Apple Still Sweet for Taiwanese Flex Makers

TAIPEI – The success of Taiwanese PCB flex circuit manufacturers this year will come down to the new iPhone. The Taiwanese Printed Circuit Association (TPCA) says there's a strong correlation between iPhone sales performance and the overall output value of the Taiwan PCB market.

Looking at the third quarter, major flex makers Zhen Ding and Taijun are optimistic about the latest generation of smartphone. Taijun has focused on LCP technology R&D and the development of LCP laminates for high-frequency flexible circuits. The fabricator is also looking at FPC41.11 next-generation technology of Neuro Circuit, which can provide high-speed and low-latency transmission solutions for huge data computing, which will boost AI capabilities.

Industry insiders expect Apple to upgrade its motherboard, which is expected to drive new PCB materials. The market also thinks that the two major features of future iPhones will be the introduction of periscope lenses, which use a prism or mirror to shine light at an angle and enable extremely long zoom ranges, on high-end models, and the migration to USB-C.

Tuned In

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	MAR.	APR.[r]	MAY[p]	YTD
Computers and electronics products	-0.6	-0.4	0.3	3.0
Computers	-1.6	2.4	3.9	9.4

Storage devices	5.6	11.1	3.6	13.3
Other peripheral equipment	8.1	-0.1	-8.0	47.8
Nondefense communications equipment	-2.3	-1.8	-2.3	0.0
Defense communications equipment	-1.0	1.5	1.0	4.7
A/V equipment	2.4	0.3	27.0	-13.0
Components[1]	-3.3	-3.1	2.1	2.2
Nondefense search and navigation equipment	0.1	1.4	0.4	2.3
Defense search and navigation equipment	-0.3	1.7	1.3	2.9
Electromedical, measurement and control	1.4	0.4	-0.5	1.7

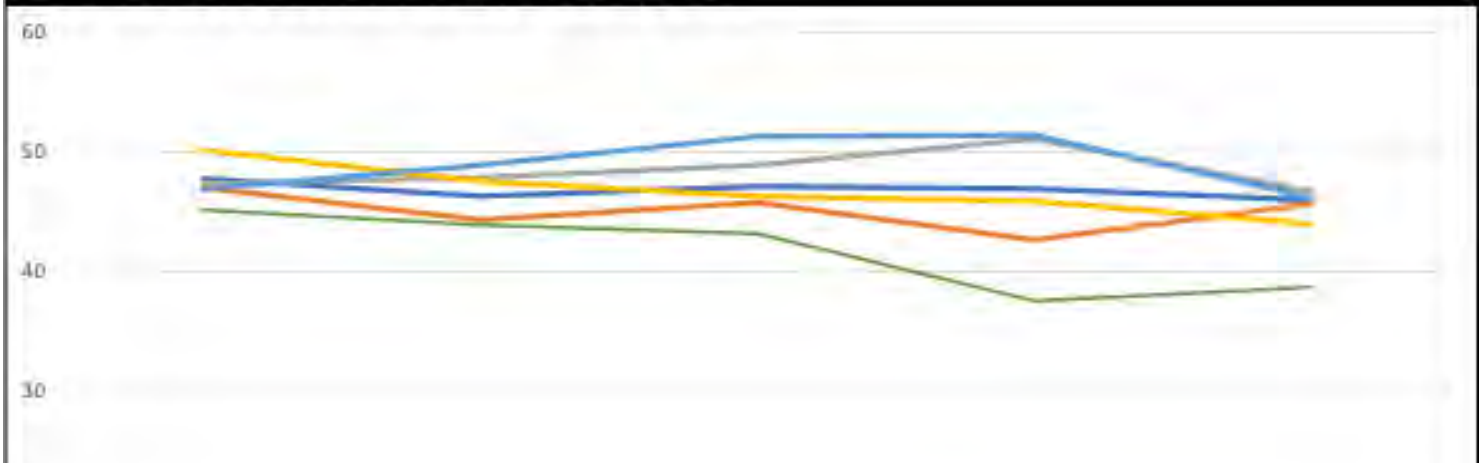
[r]Revised. [P]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, July 5, 2023

Key Components

	FEB.	MAR.	APR.	MAY	JUN.
EMS book-to-bill[1,3]	1.30	1.28	1.21	1.24	1.24
Semiconductors[2,3]	-20.7%	-21.3%	-21.4%	-21.1%	TBA
PCB book-to-bill[1,3]	0.99	0.91	0.88	0.89	0.98
Component sales sentiment[4]	82.2%	90.6%	88.7%	72.2%	76.3%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA

US MANUFACTURING INDICES



Source: Institute for Supply Management, July 3, 2023

Hot Takes

Printed circuit board and multichip module design software revenue increased 25.6% to $368.4 million in the first quarter. The four-quarter moving average, which compares the most recent four quarters to the prior four, rose 15.7%. (ESD Alliance)

Japan's PCB production fell 19.8% year-over-year in April, hitting a two-year low. (JPCA)

Consumers are expected to spend a record $41.5 billion on **back-to-school shopping** this year, up from $36.9 billion in 2022 as well as the previous high of $37.1 billion in 2021. (National Retail Federation)

Worldwide **PC shipments** totaled 59.7 million units in the second quarter, a 16.6% decrease from the second quarter of 2022, according to preliminary results by Gartner.

North American **EMS shipments** in June rose 0.9% over May and 4.3% from the previous year. Bookings fell 11.5% year-over-year and increased 0.6% sequentially. (IPC)

Global **TV shipments** for the second quarter will reach 46.63 million units, a 7.5% quarter-on-quarter increase and a year-on-year rise of 2%. (TrendForce)

Global **PC shipments** declined 13.4% year-on-year during the second quarter. (IDC)

The **DRAM market** is expected to attain equilibrium between supply and demand in the fourth quarter of 2023. (DigiTimes)

The **semiconductor market** declined for the fifth straight quarter, marking the longest recorded period of decline in more than two decades. (Omdia)

Global shipments of **smart home devices** declined 5.6% year-over-year to 186 million units in the first quarter. (IDC)

North American **PCB shipments** in June fell 15.8% from a year ago and fell 0.8% from May. Bookings fell 7.7% from 2022 and rose 0.2% sequentially. (IPC)

Worldwide **silicon wafer shipments** increased 2% sequentially and fell 10.1% from last year during the second quarter. (SEMI)

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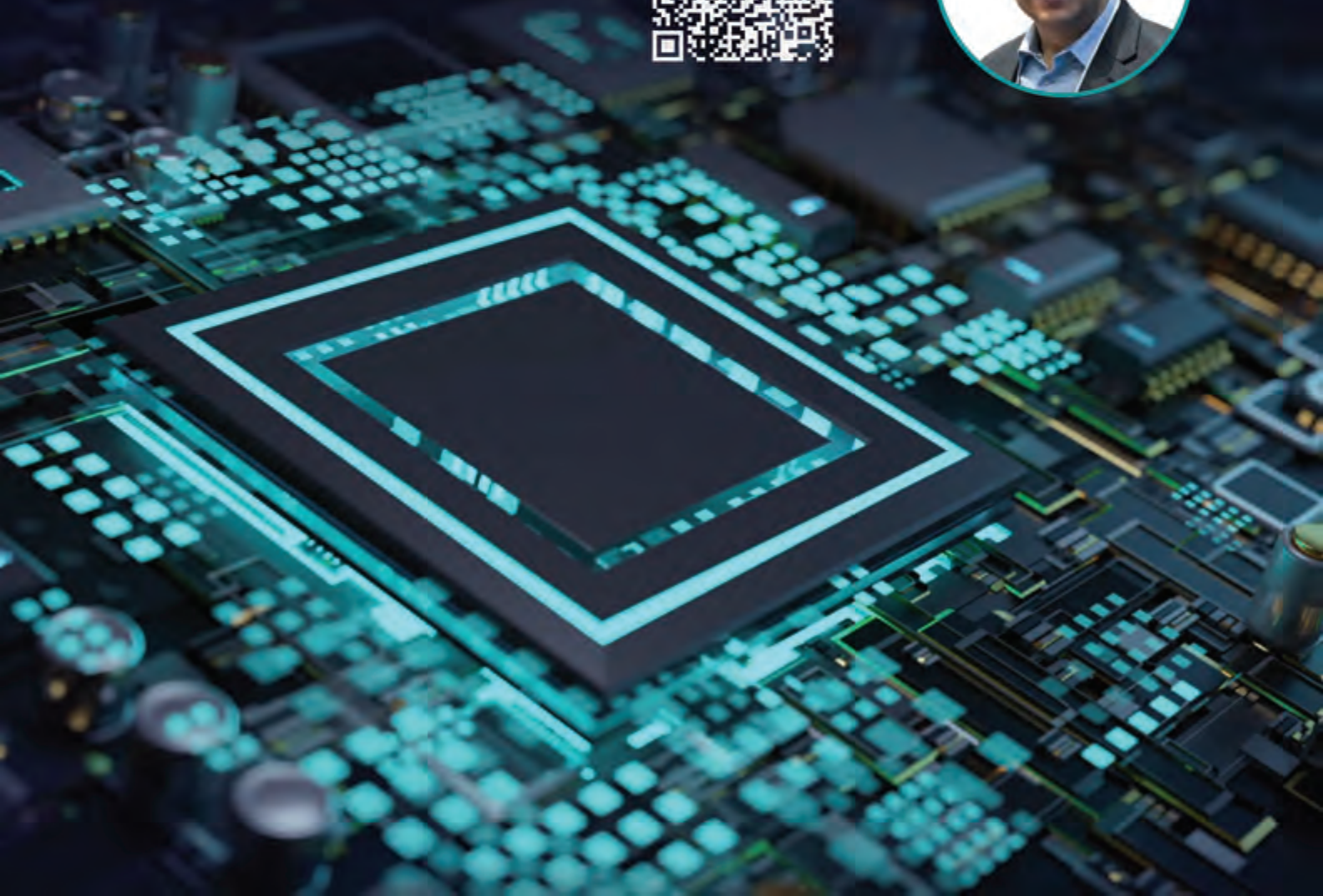

ROI

Sorting Through the Information Noise

Data for the sake of data can do more harm than good.

DATA CAN BE very useful, in moderation! Over what seems like a very long career I have seen data used and have used data for a great number of purposes. But "data," of course, can mean different things.

Early in my career during the 1970s, data were what I would consider "flat" numbers. If a machine had a counter, if you could measure or quantify a dimension via some type of gauge, that was considered best-in-class "data." During the 1980s, computers became more powerful and programmers were more adept at identifying information that previously could not be easily obtained. The power of large computing combined with the evolving skills of computer programmers ushered in new, never doable concepts such as logistics to be able to smartly schedule the entire manufacturing process from procurement to shipping.

Late in the 1980s, personal computers had evolved, and user-friendly software programs such as Lotus 1-2-3, Excel, Word, etc., enabled an expanded group of employees to collect information and create far more usable "data." These users of PCs were often not professional programmers, but the actual shop floor operator or supervisor who needed the data output but also understood the source of all the inputs. In many ways, the late 1980s through 1990s was a period of quantum expansion of data use. Both the user and generator of information could write programs where the information could be input and sliced and diced through pivot tables to generate far more usable "data." Of course, this worked only as well as the quality of both the inputs and formulas utilized.

More recently, thanks in large part to the ever more powerful computing that is readily available –

combined with technological advances in sensors and software – almost any transaction, product, process or even idea can have thousands of data points to support or disprove quality, performance or viability. This progression at times may make what is considered "data" inaccurate, unhelpful or even detrimental to decision making.

As data evolution moves forward, one cannot help but think about if and when artificial intelligence (AI) takes hold in a significant way. When a human becomes overwhelmed with data input, they can tap into their experiences of what they did and why that worked (or didn't) to regain focus or clarity. Data for the sake of data, with layers and layers of it, may just exacerbate the problem and result in a logical but very unsuccessful solution.

Which raises the question, "When is there too much data?" Early in my career when anyone was swamped with too much information or other input, they were said to be experiencing analysis paralysis. In this mental state, you begin to question everything, and bad and good inputs are treated equally because they all look the same to the overwhelmed person analyzing it. In that environment, any time saved by good data is more than neutralized by the time wasted interpreting and validating mounds of bad data. All too often, this leads to bad decisions despite having tons of data.

Often less is more. Just because something *can* be measured or collected does not mean that it *should* be.

Experience and prioritizing are the linchpins to separating what's noise from what's usable. Experience tells us when we would benefit from more information. Equally, experience tells us what type of information is critical for the task at hand versus what might be interesting but of no value, or worse, confusing and distracting.

More importantly, experience is the accumulation of data compiled over years or decades of successes and failures. Seeing how data can make tasks easier, faster or less costly comes from the experience gained both when things go well and when they do not. Experience is commonsense knowledge that enables a person to realize what is helpful and what is not.

Prioritizing, on the other hand, is realizing the inefficiency of too much data and then consciously focusing on identifying the most important information followed by the next important, etc., and reviewing it over and again so only the top few truly important data inputs are mined. Prioritizing,

enhanced by experience, makes it more probable that only usable information will be compiled, and that input will become the valued data needed to move a product or process forward. Experience and prioritizing enables users to minimize the noise that distracts effort and wastes critical time.

Throughout my career, the collection of data has been pursued to provide clarity and enable an individual, team or an entire corporation to achieve success faster and more efficiently. Data analysis enables more rapid problem-solving while providing the building blocks to potentially prevent the same problem occurring in the future. Managing that data and not letting the magnitude of all available data inputs manage you is imperative. Include the more critically important input of experience, together with the discipline of prioritization, to avoid data noise and instead harness only the signal needed for the moment.

PETER BIGELOW is president of FTG Circuits Haverhill; (imipcb.com); pbigelow@imipcb.com. His column appears monthly.

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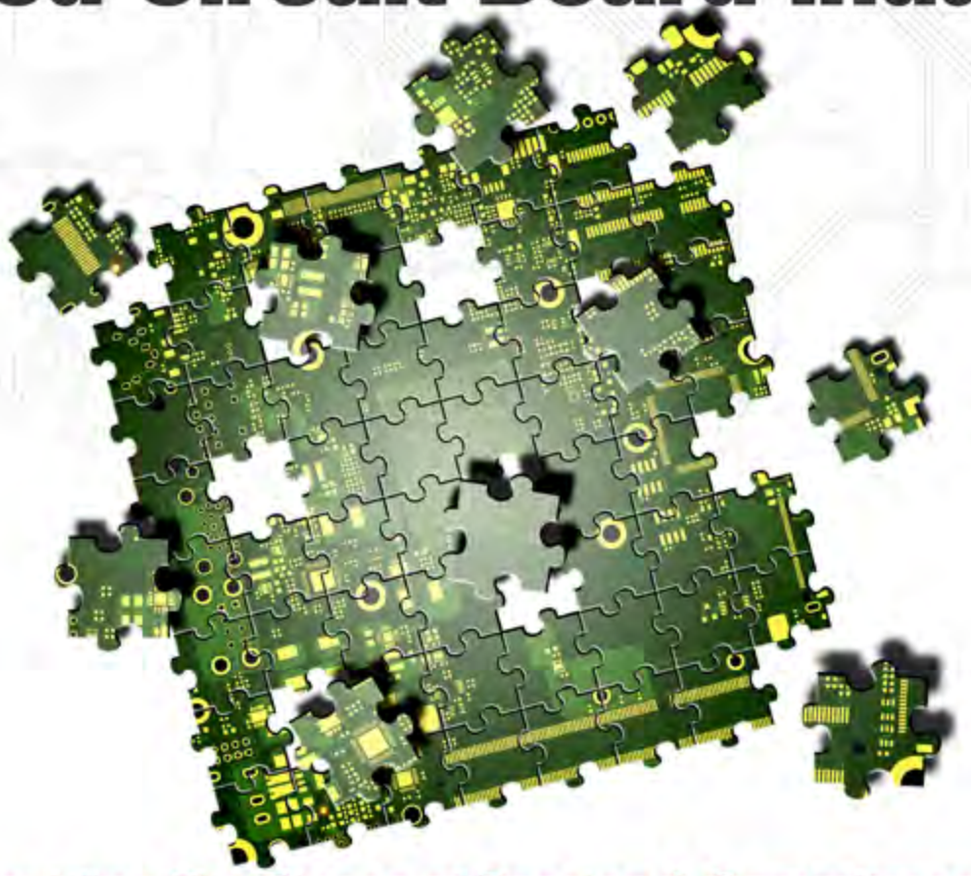

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EMS On the Move

As material supplies loosen, the winners and losers will change.

THE BIGGEST TREND I've seen in the electronics manufacturing services (EMS) industry this year is that OEM customers are starting to move. Materials availability has improved enough that OEMs are starting to move from EMS companies or regions they consider problematic, plus source new projects. The dynamics of this type of market are different from a normal EMS account acquisition cycle for two reasons. First, the past three years represented the worst material constraints that this market has ever experienced. Second, the labor shortages driven by Covid have created service issues on top of the material availability issues.

If past is prologue (and in the EMS industry it usually is), OEMs will change their sourcing behavior. They will be more secretive about intent to change suppliers and they will make decisions faster. EMS companies that adapt to this situation will have a banner year in acquiring new customers. EMS companies that have been underperforming or fail to speed up their responsiveness on inquiries and quotes will lose existing business and opportunities for new business.

While this situation provides the opportunity to close accounts in as few as six months versus the typical nine-to-12 month sales cycle, it also carries more risk. Given that OEMs don't want to tell an existing supplier they are moving until they move, the probability is high that the documentation used in the initial bid-for-bid quote is outdated. Be sure that any quotes reference the documentation revision number used for the quote and include terms that permit requote and price adjustment if the purchase order reflects a later documentation revision.

The next area of risk involves inventory. Every EMS company is carrying above-average inventory

levels right now. Some of that inventory may have been procured through brokers. It is likely that OEMs that are moving projects to a new EMS provider will want that EMS provider to purchase their inventory, and it may not be possible to inspect that inventory until the business has been awarded. The EMS provider losing the business will likely want to transfer any material it considers a liability, either in terms of excess or questionable age/handling. This makes it very important to have internal discussions about risk to ensure your company is contractually protected. Questions that need to be addressed in that discussion include:

- Is your company willing to buy that inventory from the existing supplier or do you expect your customer to purchase and consign it?
- If inventory is consigned, what markup and shrinkage factor terms will you apply?
- What method will be used to verify the count of components being transferred?
- What method will be used to preserve the provenance of broker parts?
- What contractual protections will you have relative to rejecting poorly stored parts?
- What contractual protections will you have for material-related defects arising from transferred inventory?
- What level of inventory versus forecast are you willing to carry? How will you contractually ensure that transferred inventory will be consumed in the time period represented by the agreed-upon forecast?

Understanding the answers to those questions can ensure expectations can be set early in an unusually short sales process. Waiting until the deal is about to close to have the conversation often creates a situation where the OEM buyer is upset because the material resolution they planned is different from the risk the EMS provider is ready to accept. Conversely, initiating the conversation early in the sales process from the perspective of how you handle existing inventory transfer is a less stressful way to discuss the risks and reach an acceptable agreement.

EMS providers at risk of losing business also need to internally develop a plan.

- What customers are at highest risk of loss?
- Are any customers acting in unexpected ways relative to forecasts or commitments?

- Have any buyers become difficult to contact or reluctant to discuss new projects?
- Are there "new faces" at a vulnerable customer and are adequate relationships being built with them?
- Are there options for keeping vulnerable business that have not yet been explored?
- What contractual protections are in place for customer termination for convenience?
- Is there uncovered material liability risk in any vulnerable customer?
- What contractual protections are in place for customer-approved purchases of broker parts that may be unattractive for transfer?
- What financial impact will loss of vulnerable customers have internally?

It can be difficult to talk about projected customer losses. No one wants to admit a service failure has created a vulnerability. However, internally discussing likely vulnerable customers, the possible ways to improve service to decrease vulnerability and the revised budget scenario if vulnerable customers are lost can help mitigate impact. You can't correct vulnerabilities if you aren't assessing them.

This is shaping up to be the year of transition to normal industry patterns. Similar cycles in the past have always included a period of fast project transfers, however. Preparation will open the door to more opportunity.

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Service.*; smucha@powell-muchaconsulting.com.

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DESIGNER'S **NOTEBOOK**

Where Are We Going with PCB Design?

Components drive circuit layout, but PCB designers are here to stay.

LIKE ALMOST EVERYTHING these days, the art of PCB design has its underpinnings in data. We're data driven – and swamped in a sea of information. Some of my favorite info is found on the literature offered up by the printed circuit fabricators. We get what's called a technology roadmap. While maps usually refer to geography, these roadmaps show the way into the future.

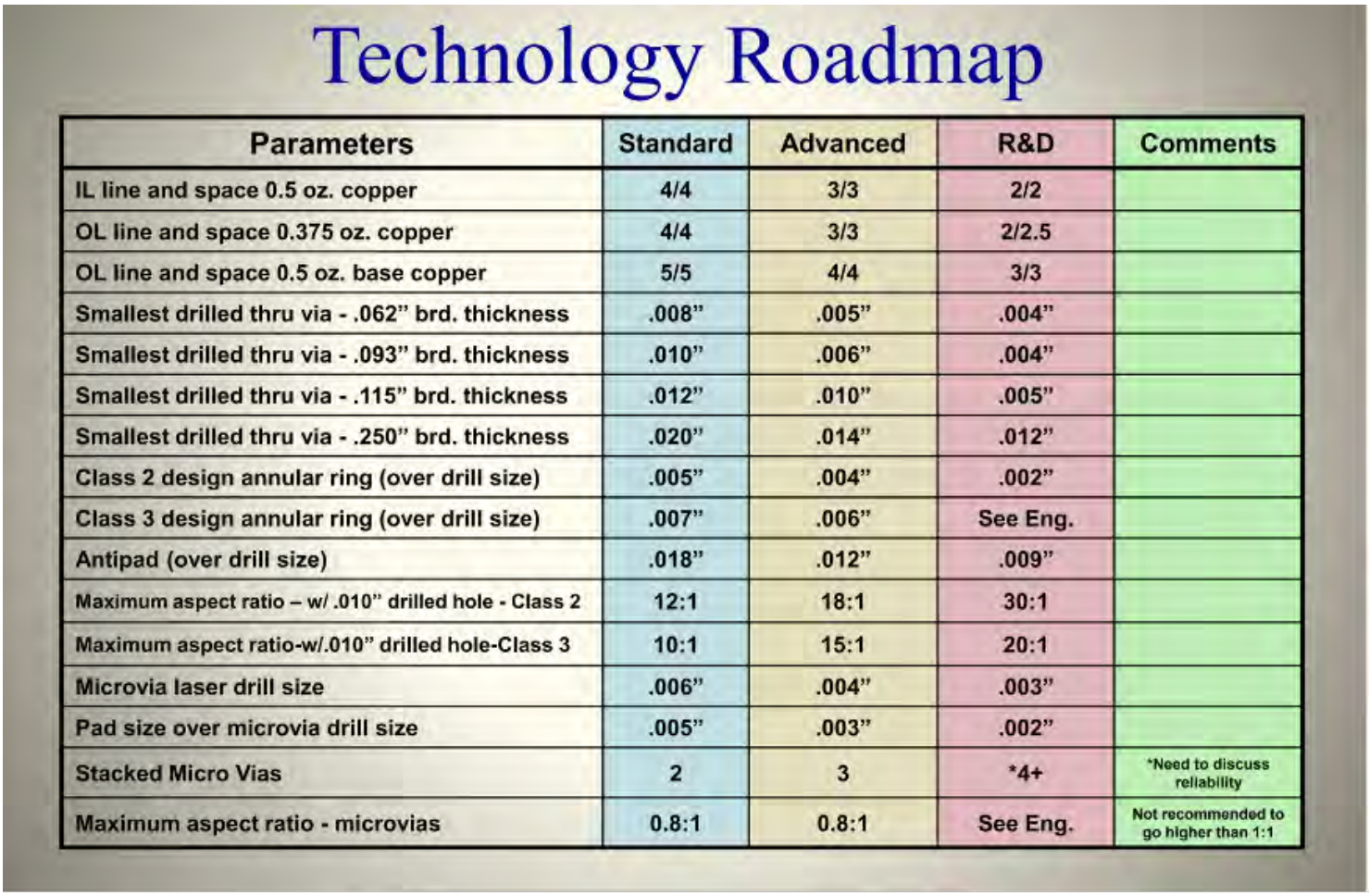
Open one up and it looks like a spreadsheet with physical attributes on the y-axis and calendar years filling up the rows. The numbers are sorted into columns with the values decreasing over time. The left column of data provides today's mainstream values for important characteristics of the circuit board.

We focus on minimum air gaps and line widths for inner and outer layers. Machining tolerances, dielectric thickness numbers, and so on are at their highest in the first column. Mass production boards should have technology that is aligned with standard processes.

When Google launched the first Chromecast dongle, Flextronics was the ODM. It owned Multek back then, which had five fabrication plants. Each site had different equipment and cost structures. To use its bottom-tier factory, we couldn't stack microvias, so I had to spin the board to stair step the 1-2 and 2-3 vias. The more price-conscious you are, the more you go for older factories.

Beyond the standard service, the next column lays out the shop's best practices as it leans into fine lines and tight pitches. Tooling charges and lead times increase and the number of qualified vendors diminishes. This represents their current prototyping capabilities.

Of course, the envelope is relative as each fabricator has a unique factory or collection of factories. This space is the home of the smartphone. The players in this market are already designing the phones for 2025 and beyond with the expectation that the technology in their prototypes will be mainstream by the time of the rollout.



Technology Roadmap

Parameters	Standard	Advanced	R&D	Comments
IL line and space 0.5 oz. copper	4/4	3/3	2/2	
OL line and space 0.375 oz. copper	4/4	3/3	2/2.5	
OL line and space 0.5 oz. base copper	5/5	4/4	3/3	
Smallest drilled thru via - .062" brd. thickness	.008"	.005"	.004"	
Smallest drilled thru via - .093" brd. thickness	.010"	.006"	.004"	
Smallest drilled thru via - .115" brd. thickness	.012"	.010"	.005"	
Smallest drilled thru via - .250" brd. thickness	.020"	.014"	.012"	
Class 2 design annular ring (over drill size)	.005"	.004"	.002"	
Class 3 design annular ring (over drill size)	.007"	.006"	See Eng.	
Antipad (over drill size)	.018"	.012"	.009"	
Maximum aspect ratio – w/ .010" drilled hole - Class 2	12:1	18:1	30:1	
Maximum aspect ratio-w/.010" drilled hole-Class 3	10:1	15:1	20:1	
Microvia laser drill size	.006"	.004"	.003"	
Pad size over microvia drill size	.005"	.003"	.002"	
Stacked Micro Vias	2	3	*4+	*Need to discuss reliability
Maximum aspect ratio - microvias	0.8:1	0.8:1	See Eng.	Not recommended to go higher than 1:1

Figure 1. A current technology snapshot broken down by relative cost. A roadmap would include what to expect in the future. (Source: MEI)

Low-volume, quickturn fabricators are the ones pushing the boundaries between the emerging technology and the next generation. The third column of the technology roadmap is the wish list of values for the future. Marketing hype replaces actual results in this forward-looking vision.

The leading-edge features MSAP, as in modified semi-additive process, where copper is sputtered onto certain layers of the stackup. Let's say you have an HDI (high-density interconnect) board with a 2-6-2 stackup. The board starts with a six-layer core and has two more lamination stages to wind up with a 10-layer board. The layers where MSAP can be applied are 4, 5, 6 and 7. The innerlayers of the core are the ones where this is doable. Other layers have a plate-up operation for the

microvias, and that's not an option with MSAP.

Of course, it is rare to find a fabricator that is up to this level of technology right now, but give it time and it should become available wherever you build your little streaming devices. All along, the driver for new PCB technology has been our partners in the component world. The pitch of the first BGA device was measured in miles, or at least fractions of an inch. So 1.27mm became 1.0 and then 0.8 to 0.65, 0.50, 0.40, 0.35, and now 0.30mm pitch BGAs in the market.

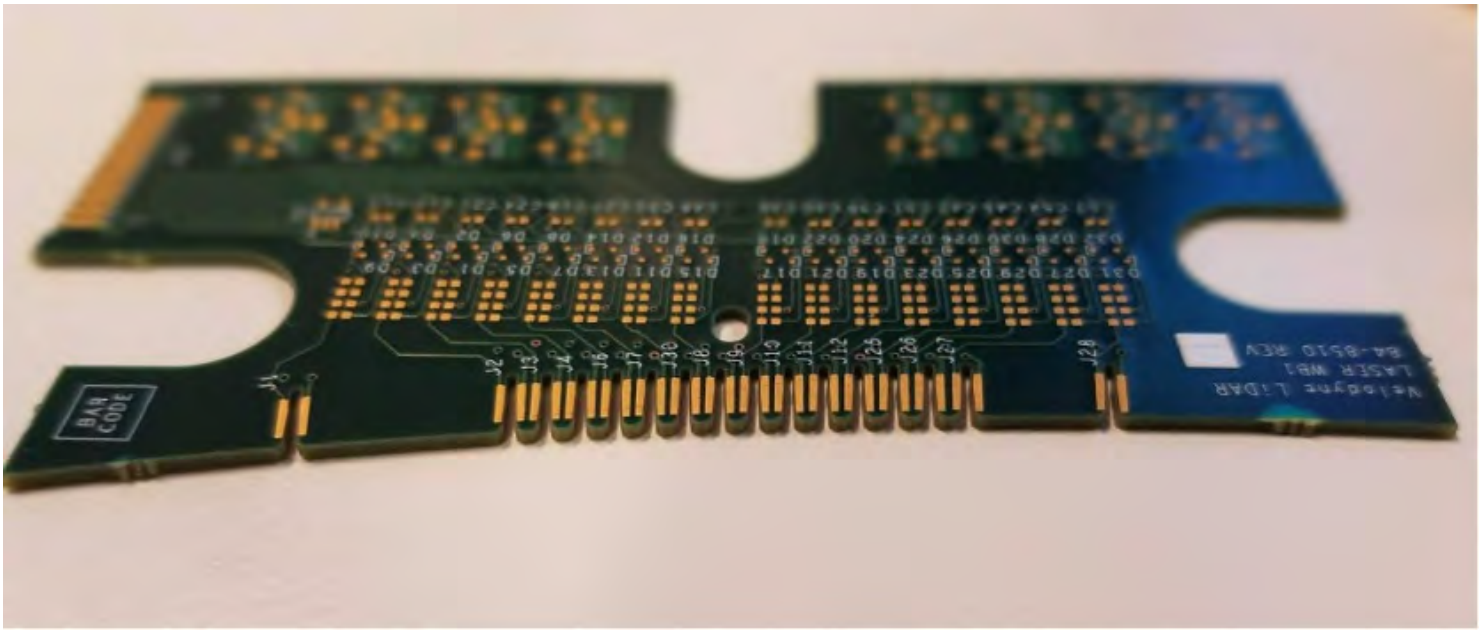


Figure 2. Laser-cut board edges with plating closer to the edge than thought possible could change the way PCBs are connected.

By condensing the circuit from perimeter pins of a quad flatpack (QFP) to an ever-decreasing geometry on a grid, the chip companies are handing off more of the workload to the printed circuit board. The marketing team calls it wafer-level chip-scale packaging, or WLCSP. In practice, the chip and substrate are essentially the same size. There are flip-chip pads on the die with matching pads on the substrate. The substrate has a via-in pad that passes the signal right down to the other side just as though it was a chip-on-board situation.

In this way, the PCB designer is doing the traditional task of the substrate where there were traces that spread out from the die to a more reasonable pin pitch that supported through-hole via technology. The chip companies could still be building them that way, but all our gadgets would be larger and more power hungry. The race to the bottom isn't going to relax if the marketing team has any say in the matter. Board designers are going to take on more of the load once carried by the chip

team and substrate.

The trends will continue with multiple passive components in the spirit of the old resistor packs. I can imagine capacitors ganged around integrated circuits while ESD diodes are clustered around connectors in monolithic packaging. This would reduce the bill-of-materials and process time in assembly. The tradeoff being that a discrete package can be replaced more economically than a gang package.

Figure 3. An insane Rubik's cube may be the forebearer of tomorrow's chip packaging technology.

On a software front, I think we will continue to see incremental improvements in design verification being handed down to the PCB community from the chip development ecosystem. The ability to lock in an IPC class or even a specific vendor's mainstream capability should help us tailor the data for high confidence in the initial iteration. This is happening one vendor at a time. (Dear Cadence: It sure would be nice to press a key and get a heat map of the board.)

The existential question for the layout engineer is “Will I be replaced by a machine?” My guess is that the simplest layouts could be thrown into the machine with usable results. The vast majority would get a more streamlined user interface but still craft the board. Out on the cutting edge, designers will be granted greater assistance from the machine learning component of AI.

Maybe that line between human and machine creeps down, but for now, most R&D is performed in secret. Machine learning counts on existing models while being part of something like ChatGPT has the potential to expose intellectual property. This in mind, I can imagine walled gardens of data held close to the vest by companies and institutions that can accumulate and leverage that much relevant information. Even with all that, someone will still be in the driver’s seat.

The job pool that seems to be shrinking is that of the librarian, which has become more of a service as time passes. The growth – as far as the deluge of offers I’m getting – is in the startup sector doing onsite or hybrid work. The jobs range from simple flexes to career boards that will consume you for months. The board designer’s job will evolve over time but it’s here to stay.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he’s not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

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DESIGN **BEST PRACTICES**

Library and Design Data Management

Automating data maintenance and revision control.

IN CONTINUATION OF the PCB Design Best Practices series, this month we'll dive a bit deeper into library and design data management. To be more specific, we'll address controlling and managing company data and intellectual property.

In general, most companies function in the same manner when it comes to electronic systems design, at least from an outsider's perspective, and PCB design is the same no matter what company you work for, what culture you belong to, what tool(s) you use, and what, if any, product lifecycle management (PLM) system you use. The difference from company to company is how people internally operate when it comes to library and design data management.

Today, we have engineering teams that work at the same location, interacting in person, and those that work remotely, sometimes spread across the globe. And of course there are combinations of these collaboration scenarios. Throughout my career I have worked in all of these environments. So, I've a good deal of experience when it comes to the different ways companies address library and design data management.

The library is the foundation of every PCB design. Accuracy, correctness and data integrity are key to long-term success. The industry best practice for library management is to utilize a type of electronic data management (EDM) system. From part creation through end-of-life, library data can be managed, maintained and controlled utilizing a tool with this type of automation.

Why is this best practice? The best designer in the world can design the simplest PCB possible, but if a library part is designed incorrectly and then implemented in a design, the outcome can be catastrophic. I have firsthand experience in powering up a very complex printed circuit assembly (PCBA) that contained a high pin-count BGA, where that BGA library part was created with the incorrect pin numbering scheme, which was not caught during the part creation process. Talk about instant overheating, resulting in catastrophic circuit burn/blow up!

A great deal of time was lost due to this error because the project was not able to move forward as planned. Then, additional engineering design time was required to fix and update the library part and redo the actual PCB design layout. To make matters worse, this bad BGA part was being used in another design. Luckily it was caught in the early stages of that design, so no major re-routing was necessary. These issues happened because manual efforts introduced human error.

The industry best practice is to use an EDM solution along with a tool capable of utilizing automation and design-for-manufacturing (DfM) checks to create, verify, and validate complex parts before they are released into a system. I have experienced similar issues, like library part updates, as well as an incorrect part number listed on a bill of materials that did not match what was in the layout of the PCB. I have heard many similar, if not worse, stories from industry colleagues regarding poor library data management, library parts being created incorrectly and not caught until after the fact, or someone ordering and purchasing the wrong parts, causing assembly issues and project delays downstream.

When it comes to managing design data, the industry best practice is to utilize a PLM system. This methodology has the highest potential for long-term success in managing your design data. Implementing and utilizing a true PLM system typically comes at financial cost, with more overhead to maintain the PLM system versus a manual approach. However, the latter provides very little or no control when it comes to maintaining the integrity of design data and no way to restrict or control who can access and or modify it. I've also experienced my fair share of the legacy approach of placing design data on an internal, open server where anyone can access and modify data, as well as having to manually conduct "where used" inquiries for individual components and specific PCB and PCBA versions. Talk about time consuming and all the potential for things to go wrong!

Although I have had success with this manual methodology, I've also had bad experiences. Like when an incorrect version of a PCB was fabricated due to incorrect versions of design data being

sent to fabrication. Another issue I have experienced was when the engineering team started on a project with a particular version of a design that was thought to be the latest, but it wasn't, because someone accidently deleted the final released production version of the design from the server. Then, later, someone replaced the released design with a previous older version, not realizing or knowing that there was a small, yet critical difference in that newer production version of the design. Sadly, these types of issues still happen today with this legacy approach.

The return on investment of a true PLM system is very high and significantly increases the ability to manage and maintain the integrity of design data and control access to it. Utilizing a PLM system along with integrated tools increases the potential for an optimized digital thread during the PCB design process. But it's more than that. It's having the ability to control and maintain the integrity of your design data, specify who can access or modify the design data, and view and make inquiries regarding revisions and "where used," from PCBs to PCBAs down to individual components and the respective suppliers.

When it comes to industry best practices for library and design data management, the legacy manual approach is not good enough anymore. Using an EDM solution and a PLM system is the best practice for managing library and design data.

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Pushing the Limits

Adaptability in all aspects is the PCB industry's greatest strength.

"Change is inevitable – except from a vending machine." – Robert C. Gallagher

IT'S AN AMUSING quip (although perhaps increasingly incongruous given the rapid adoption of contactless payments) that lets me comment on some of the transformations we have experienced in the PCB industry over recent years. Some challenges, such as thermal management, had receded for a time but are now back and more urgent than ever. Others, like the constant demand to support faster and faster signal speeds, demand that we continue to extend the limits of performance from the materials and techniques at our disposal.

The PCB's role has become hugely more significant and influential as electronic systems have gotten more complex, more performance hungry, and more mission critical. It has extended from providing basic mechanical support and connectivity to becoming a comprehensively engineered part of the system.

The electronics industry of today is vastly different from the way things were as recently as the 1980s. Thermal management was a great challenge, largely due to the inefficiency of circuits such as linear power converters and power amplifiers. The adoption of much more efficient switched techniques, as well as exponentially smaller chip fabrication processes, solved that challenge for a while.

But thermal management is back on the agenda today, particularly in lighting and power conversion. With the adoption of solid-state lighting in buildings, outdoors and automotive

applications, controlling the LED die temperature is essential when engineering light engines to ensure consistent chromaticity and the desired reliability. In power conversion, while efficiency continues to increase courtesy of new topologies and component technologies, our relentless desire to make all things smarter and more connected, wherever we live, work and travel, is raising the overall demand for electrical energy and power. But the overall size of the system is important too, to meet legacy form factors in markets such as residential lighting and to satisfy user demands for the smallest, slimmest product outline.

All this has moved designers to rely increasingly on technologies such as insulated metal substrates (IMS) as an elegant solution that can be included in designs from the beginning and not added as an afterthought – as is so often the case with a heat sink. IMS is a relatively new innovation in the PCB world and manufacturers' product ranges have quickly become diverse and differentiated to help designers find the right balance of parameters such as thermal performance, cost, size, weight and reliability for their applications.

On the other hand, the perennial demand for increased high-speed signal capability continues to challenge board designers. The PCB industry has responded with advanced, low-loss substrate materials and innovations such as ultra-thin copper foils that minimize skin effects. The critical point to consider here is, perhaps, not so much the physics of skin effect, but the processes that must be developed to produce such ultra-thin materials with consistent parameters and at affordable cost.

More challenges come from the general trend toward higher voltages in key applications such as electric vehicles and the conversion, distribution and storage of energy from renewable sources. The push toward higher system voltages enables lower I2R losses and thinner conductors. However, as voltages used push beyond 600V, there is increased demand for substrate materials that provide a high comparative tracking index (CTI > 600V) to maintain electrical insulation in environments of electrical stress, humidity and contamination.

Also to consider is the adoption of wide-bandgap power semiconductor technologies like gallium nitride (GaN) and silicon carbide (SiC). SiC, in particular, can withstand higher die temperature – typically up to 200°C – and operate from higher rail voltages than their silicon predecessors, and so demands improved PCB properties to ensure the best system performance.

In addition, the smart revolution is driving complex electronic systems, such as industrial controls,

vehicle trackers, smart meters and power systems, into harsher environments that contain natural humidity. Accordingly, conductive anodic filament (CAF) formation between conductors has become a major concern that has drawn response from the PCB industry. Closely spaced PCB interconnects and other design parameters, substrate choice and process are all factors that can promote CAF failure.

Revolutions in the PCB industry today are few, although evolution is continuous. While the underlying recipe is mainly the same today as it has always been, combining glass weave, copper foil and epoxy resin, substrate performance has changed beyond recognition. Material chemistries continue to advance, offering improved properties, and new processes such as 3-D printing are absorbed.

As well as being adaptable from an engineering perspective, the industry has shown adaptability and resilience in the supply chain. Market demands have led to China becoming the world's largest PCB manufacturing nation. Now, geopolitical changes and new cost pressures are reshaping the landscape again as material production and board manufacturing moves toward southeast Asia and Thailand and Vietnam in particular. It's reckoned that about one-third of production could migrate into this region in the coming years.

Change is inevitable and growth is prolific. The global PCB market has already grown to exceed $80 billion, through its ability to adapt and meet customers' changing needs. Endowed with that flexibility, it's expected to rise above $120 billion in the next few years.

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THE FLEXPERTS

Copper vs. CuNi for Flexible Heater Elements

Voltage, heater size and material costs all factor into the decision process.

> *I would like to use a flexible heater in a product I am designing, but I am concerned about cost. Flexible heaters typically seem a lot more expensive than regular (copper) flexible circuits. What is the advantage to using a resistive metal? Why not just use copper for all flexible heaters?*

COPPER CAN CERTAINLY be used for the heating element material in a flexible heater in many applications. When a design permits copper to be used for the heater, that will usually be the most cost-effective way to go. But how do you know if copper is a good choice for an application?

Cost impacts of copper heating element. The first hurdle to clear to ensure copper is a good cost-effective solution for a heater is the electrical resistance requirement. The biggest problem with using copper as the heating element is that it has *very* low coefficient of resistance. To get any appreciable resistance in the heating area, very thin copper must be used and element traces made very narrow in order to pack as many lineal inches into the heating area as possible. Both these will work against your goal of reducing costs. Also, base laminates that are clad with less than 0.5oz copper thickness are typically more expensive due to their fragile nature, and industry use of materials this thin is far less than use of 0.5oz or 1oz copper thicknesses. Another drawback of narrow traces is that the manufacturer's yields will be less optimal, which in turn equates to a higher selling price of the end-product. Another downside to incorporating very narrow traces that many

designers fail to take into account is the trace width variations from part to part due to etch tolerances.

The amount of trace width variation is based on the metal thickness, printing variations, etch strength variations, etc., but typically runs +/-0.001″ to +/-0.002″ on thinner foils (0.5oz or less). This trace width variation has a direct impact on the resistance of the heater. As an example, if the design trace width is 0.020″ and the trace width tolerance is +/-0.001″, the resistance tolerance based on *only that variable* would be +/-5%. Unfortunately, unless the heater is *really* big, the copper traces will most likely be in the 0.005″-0.006″ range (or less). In that case, the same trace width tolerance equates to +/-17-20%. Additional processing variables will impact resistance tolerance, so most manufacturers want +/-20-25% on the drawing to have respectable yields. Can your system tolerate and function with that amount of variation?

Another drawback to using copper for the heating element is that the resistance changes with temperature. If operating over a very small temperature range, the change in resistance due to temperature may be inconsequential. Over a large temperature range, however, the TCR can make it much more difficult to control the heater. The additional electronics necessary to accurately monitor the temperature and then drive a changing resistance load to maintain desired temp will drive up controller cost.

Cost impacts of using a copper-nickel alloy heating element. While several common resistive foils are used to make flexible heaters, I will only discuss copper nickel alloys such as Constantan or CuNi 715. Due to their moderate coefficient of resistances, these are really the only alternatives that could potentially be built using either copper or a CuNi alloy. The biggest drawback to using a CuNi alloy for a flexible heater is raw material cost. The cost of the bare metal foil can be two to three times that of a copper-clad laminate, and will require the fabricator to then laminate a dielectric film to one side of the foil prior to the photoetching processes. All said and done, the cost to get the material to the metal-clad laminate stage will be three to four times more expensive than just purchasing a copper-clad laminate. Projects with a CuNi alloy will unequivocally start in the hole cost-wise, but paybacks can offset some – if not all – of the additional cost of the raw materials. The higher resistivity of CuNi alloys will permit much wider traces to achieve elevated resistance values. Additionally, the wider traces will result in much better etch yields and much tighter resistance tolerances. These mean better overall yields for the fabricator, which will lower the

selling cost. As a bonus, CuNi alloys have a very flat TCR, making the heaters easier to control.

How do you decide? As a rule of thumb, the smaller the heater, the closer the prices will be between copper and CuNi. Very large heaters (one to four pieces per processing panel) will be significantly more expensive when built using CuNi. On smaller parts where there are 15 to 20 pieces or more per panel, the material cost has a much smaller impact and CuNi becomes very attractive for the reasons stated above. For heaters that fall between these limits, CuNi will still probably be a little more expensive, but the tighter tolerances and the improved performance of CuNi may well override the added expense.

Due to the greater resistance of CuNi alloys, a lot more resistance can be packed into a much smaller area than with copper. If the heater is very small, or has higher voltage, you may have to go this direction out of necessity **(FIGURE 1)**.

Figure 1. Thin resistive CuNi alloys permit much higher resistance density than copper.

Still in doubt about which way to go with your specific application? Have a chat with your fabricator. Having seen hundreds of different flexible heater designs, they should be able to quantify the cost versus value tradeoff to help make the best-informed decision.

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THERMAL MANAGEMENT

The Heat is On

Claire Wemp is hot on the trail of better thermal interface materials and more engineering roles for women.

by MIKE BUETOW

Thermal interface materials (TIM) are used between components to help with heat dissipation. Claire Wemp, Ph.D., is a thermal applications engineer at DuPont, with a doctorate in mechanical engineering, where her research was on heat transfer enhancement for metal surfaces. While an undergraduate, Wemp also became involved in the Society of Women Engineers, and continues to work with the nonprofit professional organization today. Wemp joined PCD&F/CIRCUITS ASSEMBLY on the PCB Chat podcast, where she discussed the use of TIMs and her work with SWE. What follows is a lightly edited transcript.

Mike Buetow: We're going to talk about TIM 1 materials, and it might be confusing for those who don't know about the TIM 1 and TIM 2 classifications. Do you want to take a moment to explain the difference?

Claire Wemp: Yes, absolutely, Mike. For TIM materials or thermal interface materials, you can think of it like a soft or pliable material that's placed between the two hard materials to help assist with heat flow going from the heat source out to some sort of heat sink. If we think about a typical computer chip, you'll have a GPU on your laptop, you've got your PCB, you have some sort of silicon wafer that's attached on, maybe your flip chip design, and then usually there's some sort of lid that fits over top of that. And at most, if you're the kind of person that tinkers around with computers, you're going to be seeing that lid. You might pop off the heat sink or hinge device of some sort, you're going to see that lid there. And you might actually see a TIM material between the

lid and heat sink itself. So when we say TIM 1, we are actually referring to the thermal interface material that is below the lid. So it's the TIM material that goes between – if it's a flip chip – the backside of the die – it's actually touching the silicon – and the lid, which is usually some sort of metal material. It's kind of a first line of defense direct from the source out to that lid material.

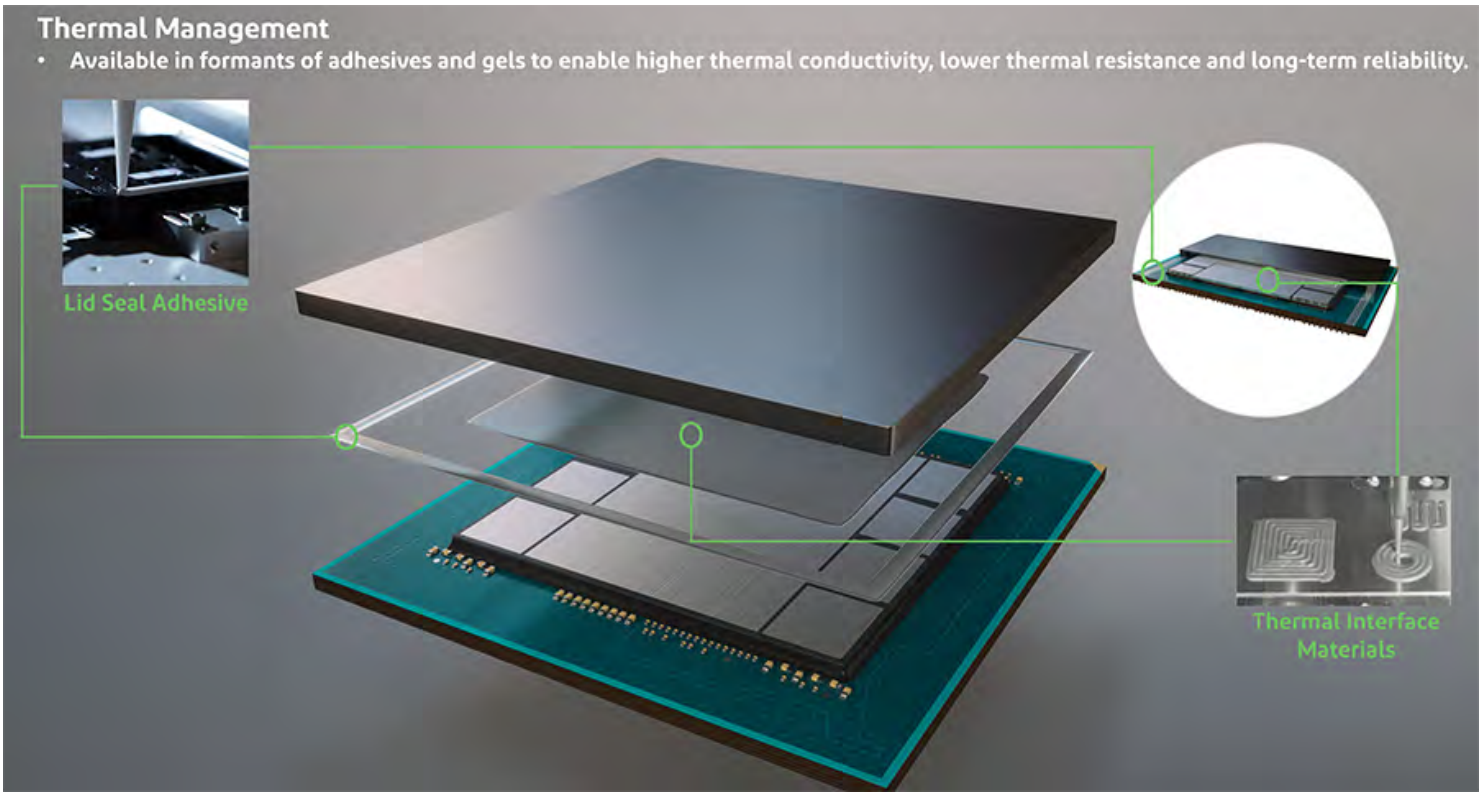

Figure 1. TIM materials are like a soft or pliable material placed between two hard materials to help transfer heat from the source to a heat sink.

MB: There's obviously a trend toward reducing heat in electronics by means of lower power devices. I think of Intel's Atom line of processors, for example, or AMD with the new Zen 4 chips. Can you tell us a bit more about where TIMs fit in? If device manufacturers are trying to take care of some of that simply by introducing lower power devices, what are some of the other hurdles that you have to go through or reasons why you might use TIM in order to get some of that heat transfer or dissipation?

CW: That's a great question. Lower power devices or just the power in general coming from the device is really only one factor that you would use in selecting the type of TIM or for that matter, as an application engineer, one of my main roles is qualifying TIM materials and understanding

whether that particular sample will actually work in a given application. Heat flow or heat flux is one of those.

Another factor is the size of the chip itself. Larger die sizes will result in more warpage. There is a CTE mismatch, or a coefficient of thermal expansion mismatch, just being a property of the material between that silicon wafer and the lid, which means that your TIM 1 material is going to experience the stress and the strain of any kind of flexing or mismatch between those as the temperature changes, maybe through power cycling or temperature cycling. A larger-size chip, particularly the corners and the edges, is going to experience longer stress and strain, so you might need to choose, for example, a TIM 1 material that has a softer, maybe lower modulus, to be able to accommodate and move with that without actually delaminating from either the wafer or the lid. In addition, you might want a TIM that has more adhesive properties that's going to adhere better to the chip to accommodate that, so die size in addition to heat flow is part of that. The last one I'm thinking off the top of my head is the temperature: What are the extremes that this particular material is going to experience, both on the cold side and the hot side, and this will depend on the application. So generally speaking, for reliability testing to qualify a TIM material in a consumer electronics application, you're going to need to pass reliability thermal cycling that will go from -40°C up to about 125°C. If it is a chip that is not going into a consumer electronics, but rather into maybe an automotive application – "computers on wheels," as they're essentially becoming – those chips now have to cycle from -40°C, and sometimes even lower than that, up to 150°C. So rather than 125°C on the high end, now it needs to go to 150°C. And as it happens, with certain types of materials, that variation between 125°C and 150°C makes things change in the polymer on a molecular level that could adjust or change the modulus or the adhesive properties.

There's a lot of clever chemists at DuPont and Laird who work to develop formulations that can go from 125°C to 150°C without maybe experiencing those changes. That's certainly a challenge in the industry now: Understanding the temperature extremes and how any given material is responding and its modulus and its adhesive properties, and then of course, its thermal properties.

MB: When we're talking about those temperatures, my understanding is that the TIM 1s are mostly silicon-based, correct?

CW: The ones offered by DuPont are currently silicon-based TIM materials, and that means that they're dispensed in an uncured state and then they go through the curing cycle once they're in the

package. That will help to cross-link the material, to make sure it's going to be adhering better on either end. Also, it slightly increases the modulus just to make it less "flowy" and stay in place nicely during those reliability tests.

MB: Let's talk a little bit about the processing. Are they always dispensed, or could you apply these to the board or in general through any other mean?

CW: Generally speaking, the silicon-based materials that go through here are dispensed onto the chip either in a pattern of some sort and then the lid is pressed on, and that's an automated process. The types of dispensers vary a little bit depending on the material or depending on the OEM manufacturing it. There are a couple of exceptions, ones that I'm maybe slightly less familiar with because they come from other companies, but there's some solder pad materials that would be solid in room temperature states. We place them in a solid-state and then burn it in or melt in, and that will melt into place, but those are for very niche applications and sometimes don't meet the same kinds of reliability requirements that polymer TIM applications are used for.

MB: And this might be diving a little bit too far into the weeds, but is the nature of these materials thixotropic or pseudoplastic?

CW: You're talking to a mechanical engineer here, not a chemist. [Laughs] I honestly don't know the answer to that. I know that there are people that DuPont that would, but being someone who works more on the application side rather than the formulation side, I can tell you that in their uncured state, when I have run tests with them, they're gooey, kind of like melted cheese, and stretchy, very good adhesion. And then once they go through the curing process, we like to refer to them as more of a gel material. They have a little more springiness, a little more elasticity.

MB: OK, so this might be more up your alley. In your experience who makes the call on TIM use? Are they designed in, or are they added afterwards because testing is showing that there's unacceptable thermal gradients or some other heat problem?

CW: Oh, it varies so widely. I've been working specifically in this TIM area for about five years, after doing a lot of academic research in this space. And when I first joined [DuPont] five years ago, most of it was kind of what you described. Later in development stage where they're like, "Oh my goodness! The electronics engineers have designed this thing that's producing a ton of heat. And

now we have to respond and try to find a thermal interface material that will meet whatever scenario has been thrown at us." Some of the higher-end electronic device manufacturers are starting to incorporate thermal management earlier in the design phase, which in my opinion is fantastic because it means, rather than having someone come at you and say, "Here's our PCB, and here's the spacing of all our components, deal with the thermal," you can come back and say, "Well, gosh, it would be really great if we could separate out the memory and GPU just a little bit more so that we can have a more even distribution of heat. Or maybe we'll incorporate some heat spreaders or something like that." And there can be more of a conversation back and forth. Designing, scaling up and manufacturing PCBs is expensive and it takes a lot of effort to figure out the placement of everything. If you don't consider the thermal, oftentimes, by the time thermal is incorporated, you've already got a design, you've already done scale up, you put in all of that early funding. You don't really want to go back and start from ground zero moving things around. The earlier the better. It varies so much. We work with a lot of different customers and I think many of them have their own approach to it.

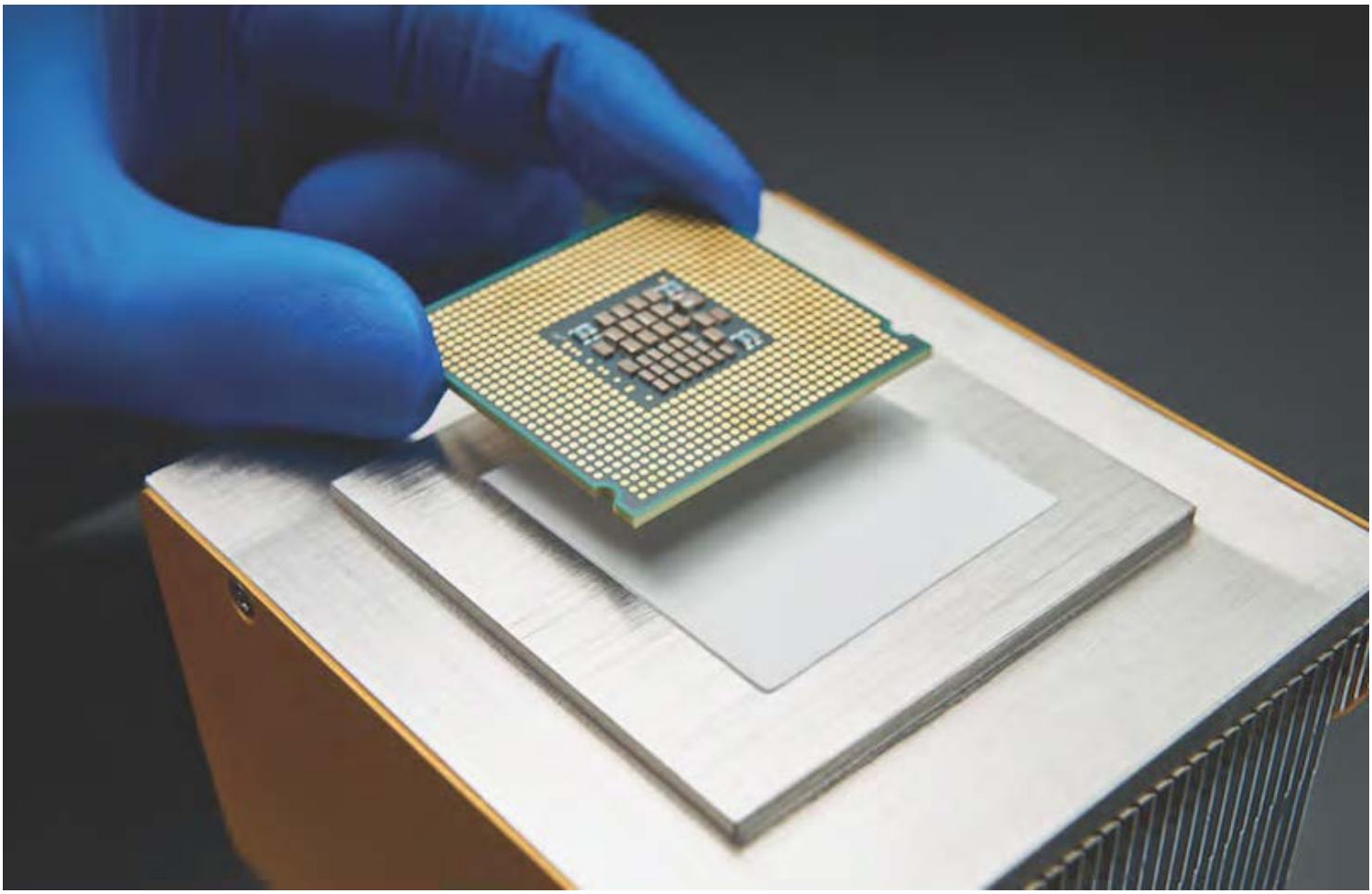

Figure 2. Higher-end electronics manufacturers are starting to incorporate thermal management in the design phase.

MB: Are you seeing TIMs used as a possible replacement for heat sinks, or are they typically going to be used simply because there's no other solution, but the heat sink is still going to be there to resolve some subsequent issues?

CW: The thermal interface material doesn't act as a heat sink. It's merely the means to get heat from one place to another. If you were to literally stick the heat sink, which is usually metal, directly on top of the lid, you're going to have metal on metal and, on a micro scale, that has a lot of air gaps. Air is a thermal insulator. You don't want that. So really the TIM is just serving to fill all those little crevices. So no, I don't see the heat sink going away. However, what exactly the heat sink is varies a lot. Historically you would see finned heat sinks, just metal fins. Sometimes you see pin fins, which are more like individual rods sticking up, and you have air flow. So for any mechanical engineers [reading this], those heat transfer classes, conduction cooling, just got air flowing over it. And the different kind of controls that we can address with that or the temperature of the air, the speed of the air. And that's about it. And it takes a lot more HVAC cooling if you need to lower the temperature of the air, or if you need to turn the fans higher to blow the air faster, that takes energy.

And it's also loud. I don't know how recently you walked through a data center, but oh my goodness, when fans are running at 100% duty cycles or 80% duty cycles it is loud. Ideally you want to try to reduce that as much as possible. And people have designed all sorts of cool, cute things to do this. Now we start seeing heat sinks that have heat pipes incorporated inside of them. It's usually copper, kind of vertical heat pipes, and horizontal fins. You still have air blowing over it, but the heat pipes introduce an evaporative cooling component which is pretty nifty. Then you have both convection cooling and evaporative cooling happening inside the heat pipe. But in essence you're still just blowing air over it. When we get to a really high end, especially in data center applications, we're starting to see liquid cooling. You might have a cold plate with an inlet and an outlet for liquid coming in and even in many of those cases, you still need to have thermal interface material because that block of metal that is the cold plate has to attach somehow to your lid, or in some cases to the die itself. Some designs will actually remove the lid and in that case we call the thermal interface material TIM 1.5, kind of a hybrid. Essentially, you've got the backside of the die, the TIM 1.5, and then some sort of heat sink sitting on top. But in any case, the heat sink can come in many, many forms. I probably haven't even talked about half of them but it's a great place for a designer to get creative and also think really critically about the space you have to operate with.

MB: For companies that are really thinking this through, who all is in the room at the outset?

CW: It's going to be a really great cross-section of engineers: electrical, mechanical. You would probably have PCB designers in there. Probably have some budget people thinking about how much things are going to cost. You might even have some general designers as we know working in the electronics industry, everything gets ripped apart on iFixit or one of these online websites. So you want to make it look pretty from the inside. So yeah, honestly, those that would be my guess off the top of my head since as a supplier of raw materials I'm never sitting in that room. But that would be my guess. Folks in there are going to range from electrical to mechanical and design.

MB: Let's switch gears for a moment. You've been involved in the Society of Women Engineers since your undergrad days and continued that effort while working on your doctorate. What drove you to get involved?

Wemp continues to help the next generation through her work with Society of Women Engineers.

CW: When I started my undergrad at Santa Clara University, I was in a class of mechanical engineers, about 90 of us, and I think there were maybe six, possibly seven mechanical engineers who were women. In high school I never really thought too much about the breakdown of gender

because most classes were split 50:50. But I'll tell you, it's pretty shocking to walk into one of your morning seminar classes and be one of two women in a 100-person class. And it really hit me in a way that I didn't expect. And I did actively seek out ways to engage with other women that were sort of going through the same process as me, a little bit solidarity, a little bit social, and also really working to make sure that future generations were not going to experience that same thing that I had just being sort of one of the lone wolves in the room. Society of Women Engineers is an international organization. They have sections that are at the collegiate level. They have sections that are professional sections. I'm now part of the Santa Clara Valley section of the Society of Women Engineers on a professional level. But the undergrad sections just do a fantastic job of engaging and creating a space for young women who are desiring to pursue engineering, to really share their joys and their struggles, but also to connect with professionals in the area that have gone through that and seen the other side of it. I think it's a fantastic organization I've been involved in. Like you said, ever since undergrad and continuing through grad school and now, as a professional member.

MB: Per the National Science Foundation, if we look at all science and engineering degrees, women accounted for half of them in 2018. But if we look a little closer, the NSF goes on to note just 22% of engineering degrees in 2018 were awarded to women, which is up only four points in 20 years. Now, the percentage of doctoral degrees has almost doubled in that time. Women aren't just switching to coding either. I want to point out that percentage has actually declined seven points in 20 years. I'm going to guess that awareness and recruitment were really big topics of conversations in some of your SWE chapter meetings.

CW: Huge, huge, Mike. Absolutely. So the studies done by Society of Women Engineers, NSF and then I believe the American Association of University Women (AAUW) have shown that women and young girls typically start self-selecting out of STEM classes whenever they can, where they start telling themselves that "I'm bad at it" and that kind of perpetuates the desire not to pursue it, between 5th and 7th grade. And if someone starts telling you at that age, "Well, you're just not good at it," then you're not going to have a desire to do it. And when I read that data, I thought back to my 4th grade teacher who told me the opposite. He told me "You're good at math," and had me start doing some advanced stuff with a couple other students. I'm sure at the time I didn't think too much of it, but for all I know that has been the linchpin that got me excited about it and continuing.

For outreach efforts, that's a big part of SWE, where we have SWE Next, which is sort of like an elementary to high school club to try to engage even younger students as much as possible, we would do a lot of outreach activities trying to bring hands-on engineering to students at young schools and again, not just women. We'll bring these activities to classrooms that are of all genders, so that's the part of it, but one of the things I really want to highlight is something that often gets overlooked. Many times, when people say, "What are the key skills that you need to be an engineer?" [the response is], "Oh, you need to be good at math and science." But the conversation ends after that. So you could imagine a young girl hearing that thinking, "Well gosh, I don't like my math and science classes," or "I'm not good at it," and they'll just figure out I won't be a good engineer. What I like to say to that is, "If you're an engineer that's really, really good at math and science but you have no creativity whatsoever, you're not a good engineer." You could be so good at these, but we really need people who are thinking outside the box, thinking creatively, and part of thinking outside the box is having people from different backgrounds who just naturally think differently because they've experienced different things in their life, and that could be gender, it could also be cultural, it could be socioeconomic status … there's so many different things. I had a design engineer tell me when I was an undergrad that when they were originally setting the building code standards for kitchens, they set the countertop height to be appropriate for the average male, because all the people sitting on the standards board were men. But at that time most of the people that cooked in the kitchen every day were women. And so they spent all this time and money, and they built all these standards and they started doing testing, they brought women in, and the woman said, "These counters are way too high!" I think that's a very funny kind of practical example. But you know the reality is, is that most of the things that engineers design and build are being used by men and women. And so if we don't have a diversity of people sitting at the table we will end up with a counter that's too tall, metaphorically speaking. I really do feel strongly about getting that pipeline going and trying to remind young girls that creativity is as much a part of it, if not more so. than just being good at math and science. I did not like physics when I was in high school, and I became a mechanical engineer, so what do you know!

MB: I totally get the creativity part. We had a panelist at our PCB West conference last year who is the director of engineering for Collins Aerospace. She talked about how kids who play Minecraft think in 3-D, they think in abstract ways. And she felt that the next generation of engineers, or rather the folks who want to find those people, should be focused dead center on that group of kids because their brains are already wired

that way.

CW: Yep.

MB: Are there specific things along those lines that we in the industry can do to help encourage this and to help, not just young people – because I agree with you, it's got to start in elementary school – and not just educate them as to what the possibilities are, but then also help them walk through a path so that they could see where the things that they're doing today might actually translate into the really cool products of tomorrow?

CW: Oh boy, that's a great question. What are the things that we can do? It really comes down to how are we educating young minds. I don't have children myself, so I'm not really as familiar with what the school system looks like if I were to hop into a classroom right now. But I hear a lot about teaching to the tests and having a lot of these kind of closed-formed questions where there is only one answer. I think that if we want people to start thinking outside the box and being more creative in their approach, we need to give them challenges that have more than one solution. Almost all the activities that Society of Women Engineers brings into the classroom are these sort of open book options. We give you a bunch of tools and we tell you, "This is the goal that you're trying to shoot for, but however you want to do it, go ahead and do it." The simplest thing was one where we give a bunch of paper and tape and twist ties and a few other things that everyone has exactly the same amount of it, and a marble. We say, "You have to start at table height and design some sort of something" – we don't have to call it a ramp, although most of them end up doing a ramp of some sort – "that will allow this marble to travel to the ground as slowly as possible, and whoever's marble takes the longest to get from top to bottom is the winner." And people will do spirals, kind of the swirly slide of some sort or different things, but once in a while we get a kid who designs a full lever system. It's like, "Wow! You were not taking the easy route." They didn't look at what other people around them were doing. I just get so excited when I see that and, to me, that maybe those are the kids doing Minecraft, essentially because Minecraft is a giant open-source game where you get to do whatever you want to reach your goal. That's exactly the kind of stuff that we can and should be doing more of in schools.

MB: What are some of the things that DuPont is doing to help move the needle in terms

of attracting more women to engineering in general and perhaps specifically to electronics?

CW: I think there's some practical things from the benefit side, and this is not just DuPont, but DuPont is on the corporate board for SWE, so certainly they help playing their role in any kind of lobbying efforts or different logistical things that SWE is trying to do on a more national level. But as a company, I would say some of the big recruitment tools and again, bearing in mind they're usually recruiting people in their 20s and 30s who are coming out of undergrad or Ph.D. programs, they recently increased their paternity and maternity leave. So if you're someone who's looking for a company and thinking of starting a family, that's kind of a big deal. Not all companies have really generous policies. Or more importantly, they have a policy that people might not use it or the culture doesn't encourage people to use it. And I have absolutely seen both men and women taking full advantage of that at DuPont. I see that as a really positive thing, because it creates a culture of welcomeness and inclusivity and when people then come back from maternity or paternity leave, I've seen people get promotions a couple weeks afterwards. There isn't a negative downside to that, and I think that is a cultural thing that probably takes years to build. DuPont, I believe, has done a really excellent job of that. We have an internal DuPont women's network, or a DWN, and we bring in external speakers as well as internal speakers talking about different topics that are relevant to women. So that could be, how we can bring our whole selves to the workplace, or create a culture where we don't feel like we need to hide a certain part of our personality or background when we come to the workplace? That might sound really foreign to some, but I was really surprised there's certain factors of people's culture or personality or whatever they just never share. And then because of that, they feel like they're hiding something, and that can ultimately be detrimental to their presence in the workplace. One thing we really try to be more open about is talking about wage equality and fighting for promotions and knowing how to promote yourself, how to speak up in a room which oftentimes can be very male-dominated. We create spaces to have those conversations. DuPont's Woman Network is one of those. Beyond internal workplace organizations, we have been doing work for recruiting externally to try to increase our physical recruitment pool of women engineers. That includes recruiting at the National Conference for Society of Women Engineers. It includes reaching out not just to Society of Women Engineers, but any kind of other chemistry, women organizations or clubs or campuses, when we do campus recruiting, to make sure that those clubs are advertising to their constituents to come out when we recruit. There's a couple different avenues we are going. Those are the ones I'm taking off the top of

my head, but it's certainly something that is in our thought process as we go through recruitment.

MB: And how would someone in industry get involved in Society of Women Engineers?

CW: You can go on to the Society of Women Engineers website (www.swe.org) and search for a section near you. If you live near a big city, odds are there probably is a big section. If you live more rural then you might have to join virtually. We're kind of all slowly transitioning out of the Covid era and maybe just beginning to offer some more in-person events. My local section has been doing coffee hours roughly once a month where they choose a local coffee shop and have a range of a couple hours one morning and people can come out and grab a cup of coffee and chat, and that has surprisingly been a really successful avenue to get people connected. That would be my first thing; just start seeking out a local group and go to an event, get involved, meet people and you'll be really surprised. Everyone's so friendly and so eager to help out. I work in the Bay Area and we've had some layoffs from various tech companies in the area, so there's been some women in our section who are now seeking new jobs. We're having these wonderful conversations about, "How do I update my resume for the first time in five to 10 years?" and "Making sure that I'm getting the salary I'm worth, and how do I negotiate that?" These are all extremely valuable conversations, some of which might be considered taboo in certain circles, but we're trying to break that down and really be transparent about it among the women in the group. I think these sections are great. I encourage any women or for that matter, men who are allies and interested in, especially ones who might be responsible for hiring and trying to figure out well, "I put out this job offer and the only people that applied are men. What do I do?" Join SWE. Talk to some of us. We've got lots of different suggestions to help folks that are trying to diversify their hiring pool.

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PACKAGING

A Plethora of Pitches

The unstructured evolution of integrated circuit package technology (and its consequences).

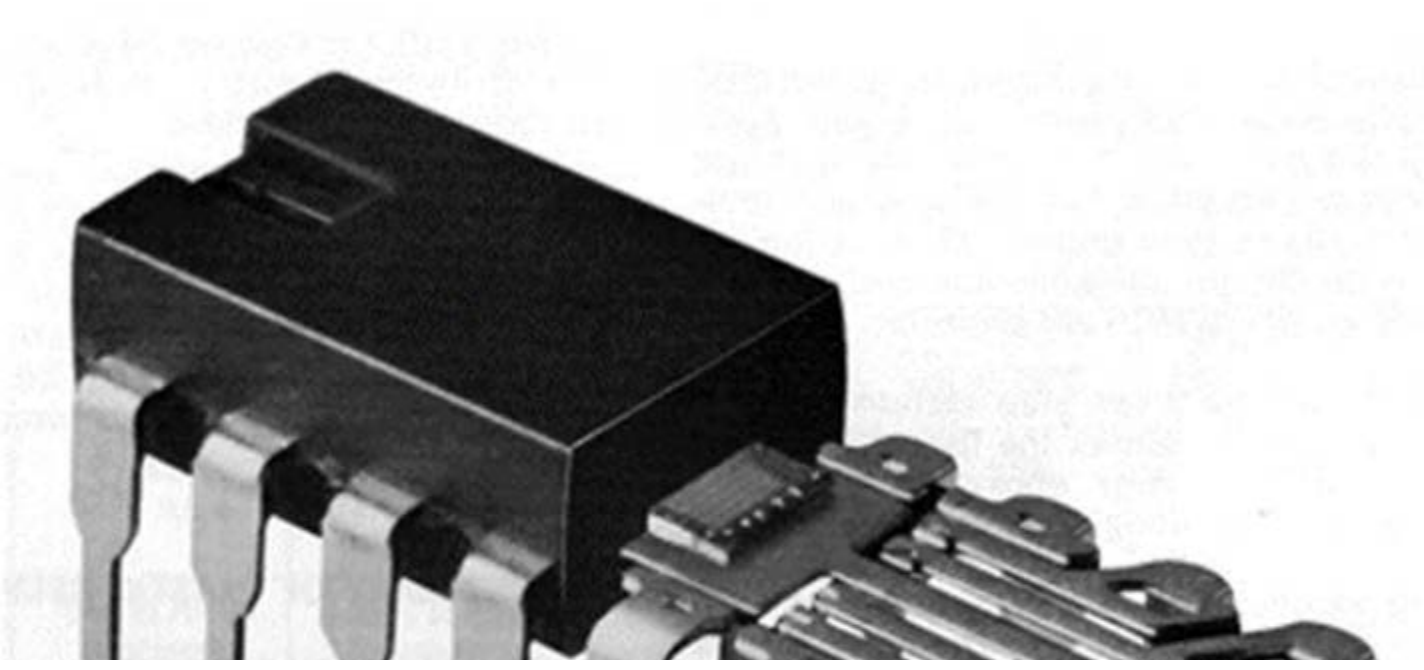
by JOSEPH FJELSTAD

I purchased my first "integrated circuit" around 1957, which was roughly a year before Jack Kilby is credited with inventing the IC. In appearance, it was a paper phenolic PCB with six discrete transistors in TO-cans and a few axial-leaded resistors and capacitors soldered on one side. If one can stretch their thinking just a bit, however, one can see the truth of the suggestion that it was arguably an "integrated circuit." The fact that Kilby was working at Centralab in Milwaukee, a ceramic circuit maker, immediately before heading to Texas Instruments for his new job was fortuitous. I have long assumed it influenced his invention. Around the same time, the IC's recognized co-inventor, Robert Noyce, took the idea a step further and showed how transistors and interconnections could be built on silicon wafer, which remains the primary method used today – featuring sizes a few orders of magnitude smaller and significantly increased material sets to embrace many new semiconductor materials in addition to silicon.

Handling delicate pieces of silicon, was not going to "cut it," however, so IC manufacturers invented IC packages to protect the silicon chip in the assembly process. TI came up with a robust ceramic package that used microscopic gold wires to connect the I/O on the chip edges to the metal leads affixed to the ceramic, and a lid was soldered on top to protect the structure. The leads at the periphery extended straight out and were soldered to the copper metal circuits supported by a ceramic or organic base material **(FIGURE 1)**. These were the first surface mount packages, and they flew to the moon with the crew of Apollo 11 in the navigation, control and monitoring computers on board. Another format was proposed around roughly the same time that made assembly easier, however, which was the iconic dual in-line package **(FIGURE 2)** invented by Bryant "Buck" Rodgers

at competitor IC maker Fairchild.

Figure 1. Many of the earliest IC packages, notably those from TI, were flat leaded and surface mounted. This carrier contains 10 ceramic ICs having 10 leads each with soldered lids.



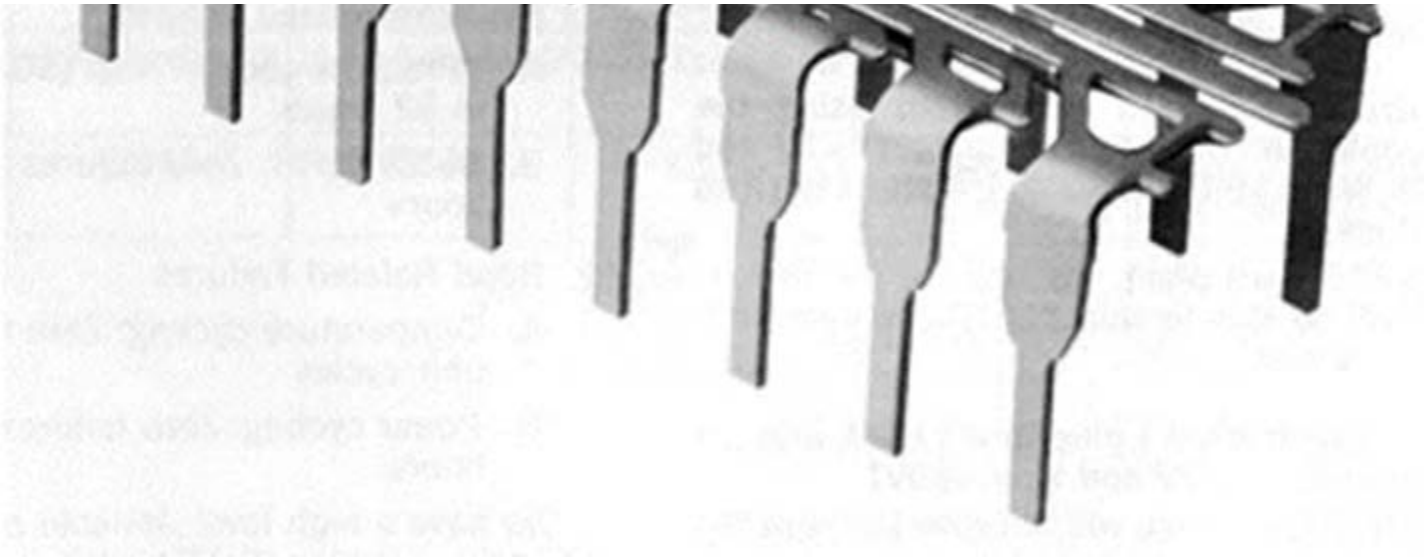


Figure 2. Structure of a DIP with die attached to metal lead frame and wire-bonded to leads to redistribute chip I/O to a standardized and more useful structure and pitch for assembly. (Source: Intel).

The DIP reigned supreme throughout the 1970s as the electronics industry exploded around the world, and the DIP format is still in use today. Among the features that made it so attractive was the pins of the lead frame carrier made hand assembly easy while being robust enough to be automatically machine inserted at high speed, plus the leads were all on 100-mil (2.54mm) centers. The former served the needs of mass assembly, and the latter eased the designing and prototyping of assemblies, with prototyping typically using "breadboards," carrier substrates fully perforated with drilled holes on 100-mil centers which could accept all common components and subsequently be interconnected using wire wrapping or direct soldering of the interconnecting wires. This technique is also still used by electronics hobbyists today to try out new ideas without having to purchase a PCB. For production, laying out a PCB on a common grid substrate could be easily done – usually without the need for a computer.

Surface Mount "Rediscovered"

The disadvantages of such "pin-in-hole" components became apparent as pin counts climbed. One was the realization that the holes required for the lead pins consumed a significant amount of printed board real estate. Another was that electrical/electronic parasitics of the long leads required to get from chip to board were significantly limiting performance in a time when PC developers were trying to squeeze greater performance from their offerings for market advantage.

In the 1980s, surface mount technology was "rediscovered." It was quickly and virtually universally recognized by the electronics industry as the answer to size, weight, cost and performance challenges faced by the industry, and a host of new components were created to address the need. First, the small outline package (SOP), then the thin small outline package (TSOP), both with leads on two sides only, followed soon after by the quad flat package (QFP) with leads on all four sides and others. With the doubling of chip transistors approximately every 24 months (in accord with the observations Intel cofounder Gordon Moore made in a 1995 update[1] of his seminal 1965 paper[2] projecting the trajectory of the technology) the need for more I/O and the problem of peripherally leaded components grew rapidly, thus attention shifted to area array packaging.

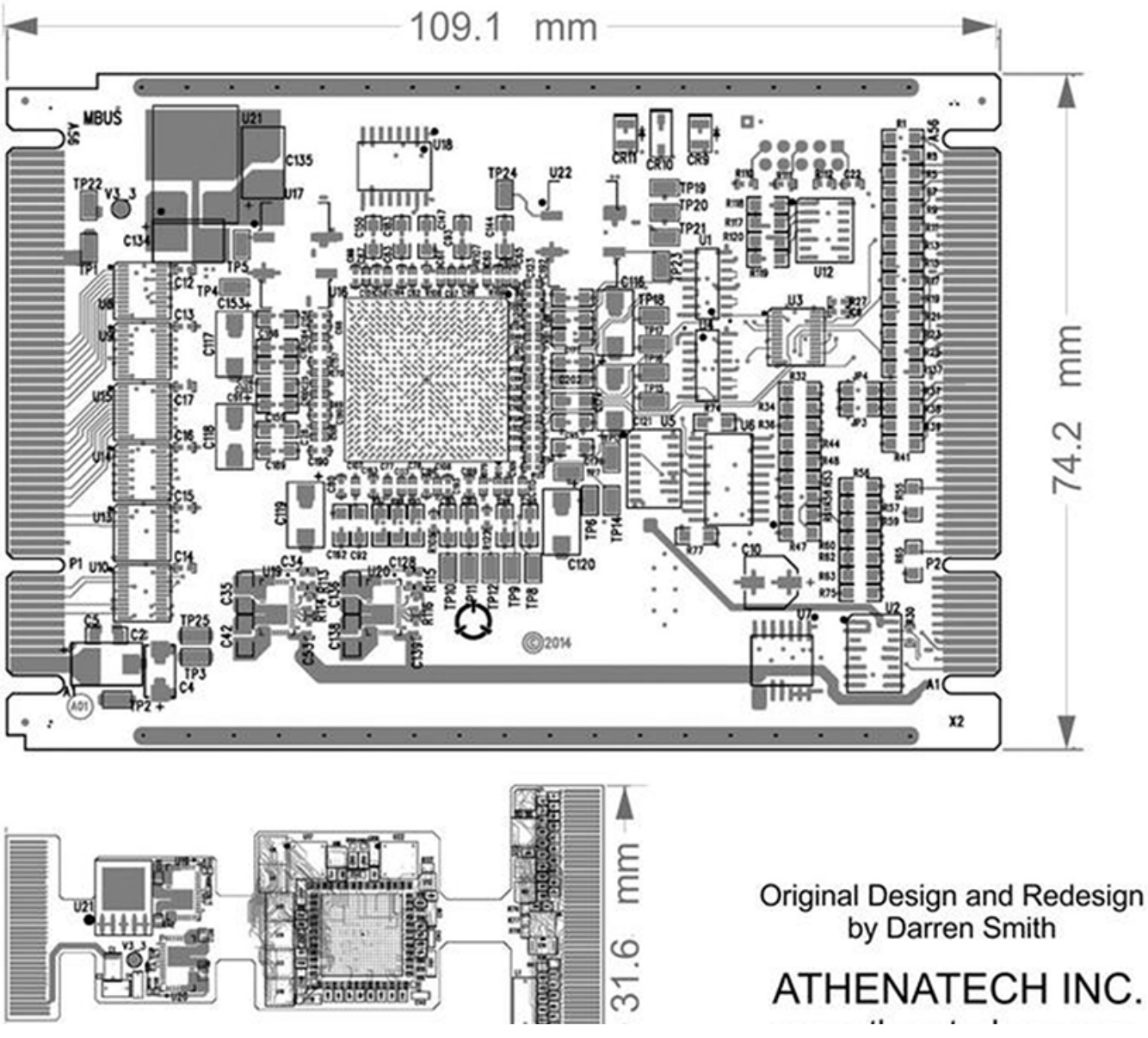
The advantages of area array terminations were quickly and easily understood by engineers, and the pin grid array (PGA) was quickly adopted for microprocessors because they could be socketed for testing and in use. It also allowed the user to easily upgrade to next-generation processors. Direct attachment of processors to motherboards was deemed necessary for cost and performance reasons and the ball grid array was introduced. It was beset by the challenge of inspecting the solder joint. If one cannot see a solder joint, how does one know that it is good?

The '80% Rule' Problem

Thus, peripherally leaded packages continued to be designed and used. However, to overcome the size challenge and give planners a predictive tool for future generations of products, the so-called "80% Rule" was adopted. The rule value was clearly arbitrary, resulting in "standard" I/O pitches of 2.54", 2.5mm, 1.27", 1.25mm, 1mm, 0.8mm, 0.65mm, 0.5mm, 0.4mm, 0.3mm, 0.25mm and 0.2mm. When one steps back and thinks over the problem of such a plethora of lead pitches, one might be reminded of the tale of "The Emperor's New Clothes." Yet the industry has held fast to the concept of the 80% rule, even though on closer inspection, the apparent absence of logical thinking has resulted in significant ongoing problems for electronics designers as each lead pitch has specific requirements in terms of solder stencil design.

The problem is also often manifested as a need to increase layer counts in PCBs to deal with the redistribution wiring required to accommodate several different lead pitches of a mix of area array and peripherally leaded components. It would have made more sense to choose a fundamental base pitch and depopulate to the desired pin count. While not a perfect solution for peripherally leaded

components, it arguably makes perfect sense for area array components. This solution allows the designer to predictably lay out an assembly, reducing its size and layer count. In **FIGURE 3** are shown two identical electronics assemblies designed by the same person. The first is a design completed by the designer for a work project. It was done choosing components that met functional requirements, but without concern as to the package termination, so it included a variety to area array and peripherally leaded components along with various and sundry discrete components. The second is a design completed by the same designer using the same fundamental components except that all the components are theoretically envisioned to have their I/O terminations on a common fundamental grid pitch of 0.5mm. No attempt was made to verify that all components were available with termination on such a pitch, as it was only to demonstrate the potential of using a common pitch to build what look like Lego assemblies. It illustrated the benefits that were enjoyed by the 1970s designer when 100-mil lead pitch was the de facto standard.



DETAILED COMPARISON SUMMARY

Design Feature Value	Original Design	Occam Redesign	Occam Advantage
Board Area	11,900 sq. mm	3400 sq. mm	**28% of original**
Component lead pitches	2.54,1.25,1.0, 0.8, 0.65mm	0.5mm	**5x less**
Minimum Line/Space	100 µm /200 µm	50 µm /50 µm	**50% of original**
Land size vs termination target	Numerous	100 µm	**Single value**
Nominal Via Pad Size	610 µm	100 µm	**16% of original**
Nominal Via Hole/Via Size	305 µm	50 µm	**16% of original**
Layer Count`	12	6	**50% of original**
Circuit construction	Rigid FR4 PCB	Rigid Flex Circuit	**Foldable circuit**

Figure 3. The comparison of designs generated by the same senior PCB designer, Darren Smith, using traditional methods versus the Occam design process, which advocates more attention to components selection (when possible). More recent thinking on the approach has suggested using packaged silicon IP blocks to allow products to be designed with the least number of transistors required.

Summary

It is evident in hindsight that the electronics industry missed opportunities to create a more coherent set of basic IC package requirements to limit the explosion of IC package types. Presently, JEDEC lists 318 registered mechanical outlines for IC packages, each with a number of lead counts and configurations. The result is thousands of choices when the fundamental requirement could well be a fraction of that number. We cannot undo the past, but we can collectively choose to use logic as a foundation for future choices to improve design efficacy and product performance and reliability.

JOSEPH FJELSTAD has been active in electronics manufacturing since 1972 in various roles, including chemist, process engineer, and R&D manager. He holds nearly 190 US patents and numerous foreign ones. He is an internationally recognized expert, inventor and lecturer in the field of electronics interconnection technology and a veteran of several startup companies, including: Beta Phase, ELF Technologies, MetaRAM, Silicon Pipe, and Tessera (now Xperi). Some of Fjelstad's innovative devices and novel reliability improving IC packaging structural features are

found in nearly every electronic device made today. He is also an author, coauthor or editor of several books on interconnection technology, including *Flexible Circuit Technology 4th Edition, Chip Scale Packaging for Modern Electronics, and Solderless Assembly For Electronics – The SAFE Approac*h (the Occam Process); joseph9000@aol.com.

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INSPECTION

Selectively Assembling High-Value Components Based on Warpage in Order to Improve Reliability

Can predicting board and part flatness at critical points in the reflow/reliability profile reduce failures?

by NEIL HUBBLE and CHANCE RABUN

Surface warpage, or flatness, is an established source of reliability issues in surface mount devices (SMD), particularly when these surfaces are considered as they warp due to heat generated in production or real-world use.[1-6] Thermal warpage of surface mount components such as ball grid arrays (BGA) and line grid arrays (LGA) are subject to different industry standards from JEDEC, JEITA, and IPC, based on sample size, ball size and ball pitch.[7-9] Further SMD studies have proposed different methods of classifying and qualifying surface shape in hopes to improve the correlation in thermal warpage data and product reliability.[10] Meanwhile, printed circuit boards are less regulated for warpage in the area where an SMD may attach. Overall PCB warpage is referenced in some industry standards and technical papers, but specific warpage limits are lacking within documentation discussing warpage of SMD landing areas.[11-12] Finally, further studies have considered warpage of both SMD and PCB landing areas together.[13-14]

The approach of considering the shape of both sides of a surface mount interface is used as the basis for this study. To fully understand warpage gaps that create defects, both sides of the attaching interface are required. The trend for larger BGA packages in high-speed network applications is furthering the need for managing warpage on both the SMD and PCB sides of the assembly.[15] Larger package footprints permit more lateral space in which shape change can occur due to either

starting sample shape or thermal warpage.

While measuring samples for thermal warpage is a common practice, this study is proposing a much different approach to improve product reliability. This study presents a concept of measuring warpage on 100% of high-value SMD devices and 100% of the PCB landing areas where they would attach in assembly, then deciding which sample to place on which PCB. This study is very much a first step and does not provide a final approach or hardware configuration to accomplish such a quality control approach. Matching initial surface shape alone to minimize initial gaps between BGA and PCB landing sites may also be a value add and simpler approach. However, gaps at high temperature points in the reflow profile are more problematic for creation of surface mount defects.[16] Therefore, this study focuses on the ability to predict what shape will be during reflow, based on a sampling of thermal warpage data and 100% measurement of room temperature shape. Thermal warpage testing is often considered destructive, thus cannot be used for 100% inspection in production.

Experimental Methodology

Warpage metrology approach. Shadow moiré and digital fringe projection (DFP) warpage measurement techniques are discussed in this study. Both are referenced in industry standards related to warpage, though DFP is excluded from JEITA standards on package warpage.[7-10] Shadow moiré is exclusively used for the data of this study, focused on accurate thermal warpage behavior of SMDs and PCB local areas. This technique is best used for continuous surfaces and provides a highly accurate approach whose accuracy does not scale with larger areas of measurement.[17] Although shadow moiré may be viable for the production room temperature measurements, here DFP is hypothesized to be the preferred approach for 100% room temperature measurements, being the more portable of the two techniques.

Shadow moiré measures surface shape by shining a line light through a Ronchi rule grating, a piece of glass with alternating clear and opaque lines, having a common pitch from 50-500μm. This creates a contour map via an interference pattern generated between the lines and the shadow cast by the same lines. A phase-stepping technique is also applied for increased resolution. **FIGURE 1** shows the shadow moiré concept, and **FIGURE 2** shows a created contour pattern.

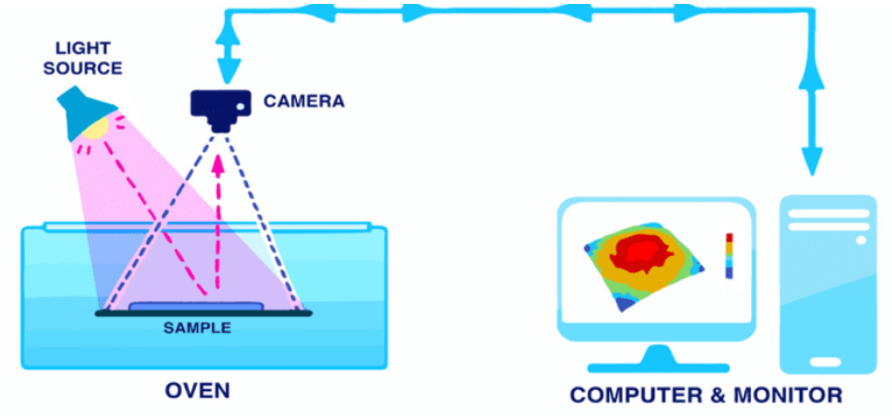


Figure 1. Shadow moiré visual concept.

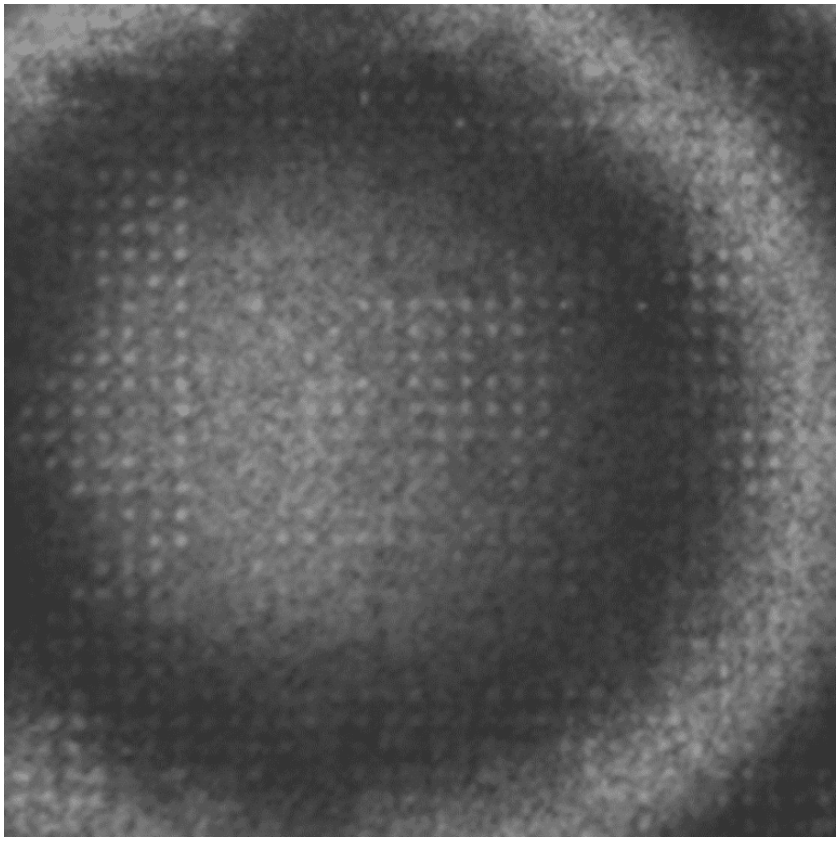


Figure 2. Shadow moiré pattern.

DFP also measures surface shape and uses a phase stepping approach to improve resolution. Calibration is achieved by measuring an optical flat at different heights. Here a pattern is projected instead of an interference pattern created. The calibration flat and measured sample are compared to show surface shape. Fringe density can be varied as well as shifted, limited by the projector resolution only. Varying fringe pitch helps in measuring sudden sample height changes. **FIGURE 3**

shows the DFP technique and **FIGURE 4** shows a surface with fringes projected on dome like contours on an overall flat surface.

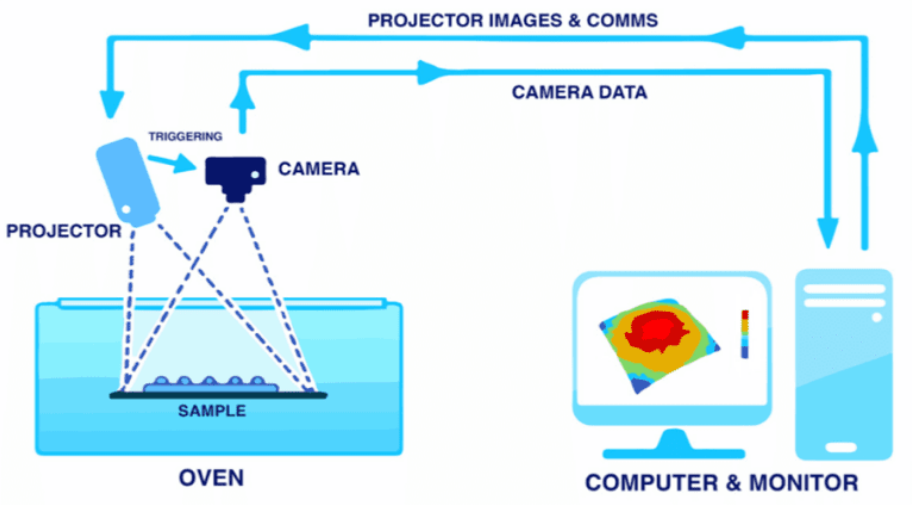


Figure 3. Digital fringe projection visual concept.

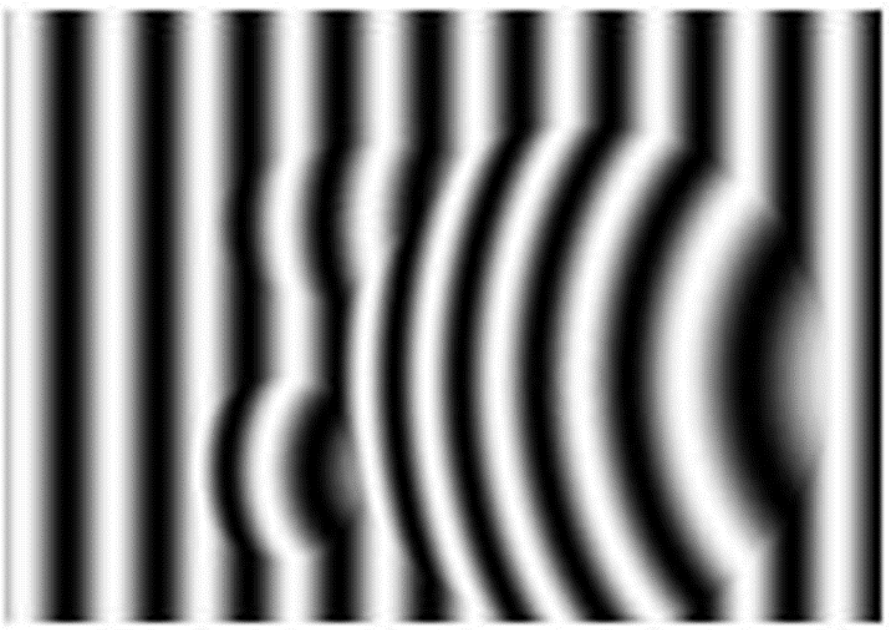


Figure 4. Digital fringe projection pattern.

Test samples. For the purposes of intellectual property protection, sample descriptions and details are left generic in this study. Here only a conceptual approach is presented and not details on specific samples and their warpage behavior. The purpose of testing these samples is to show how thermal warpage can be correlated to initial room temperature shape for the purposes of predicting

surface mount defects. This also addresses the specific functions, such as matrix subtraction and averaging, to implement such as approach.

Multiple samples of two package types are measured for warpage across reflow temperatures. Additionally, a couple of PCBs are measured for warpage. Local areas sized to match the footprint of the package sizes will be used for comparison of warpage between package and PCB area. Details of the test samples and quantities are shown in **TABLE 1**.

Table 1. Test Samples

Sample Type	Sample Dimensions	Quantity Tested
Larger BGAs	75 x 75 x 2mm	4.0
Smaller BGAs	32.5 x 32.5 x 2mm	6.0
PCBs	237 x 255 x 1.5mm	2 (with 2-3 local areas used)

Test setup. Samples were prebaked 24 hrs. at 125°C to reduce possible effects on warpage from moisture in the samples.[18] Oven setting were optimized around sample temperature uniformity, per standard operating procedures. All samples were subject to the same thermal profile, shown in **FIGURE 5**.

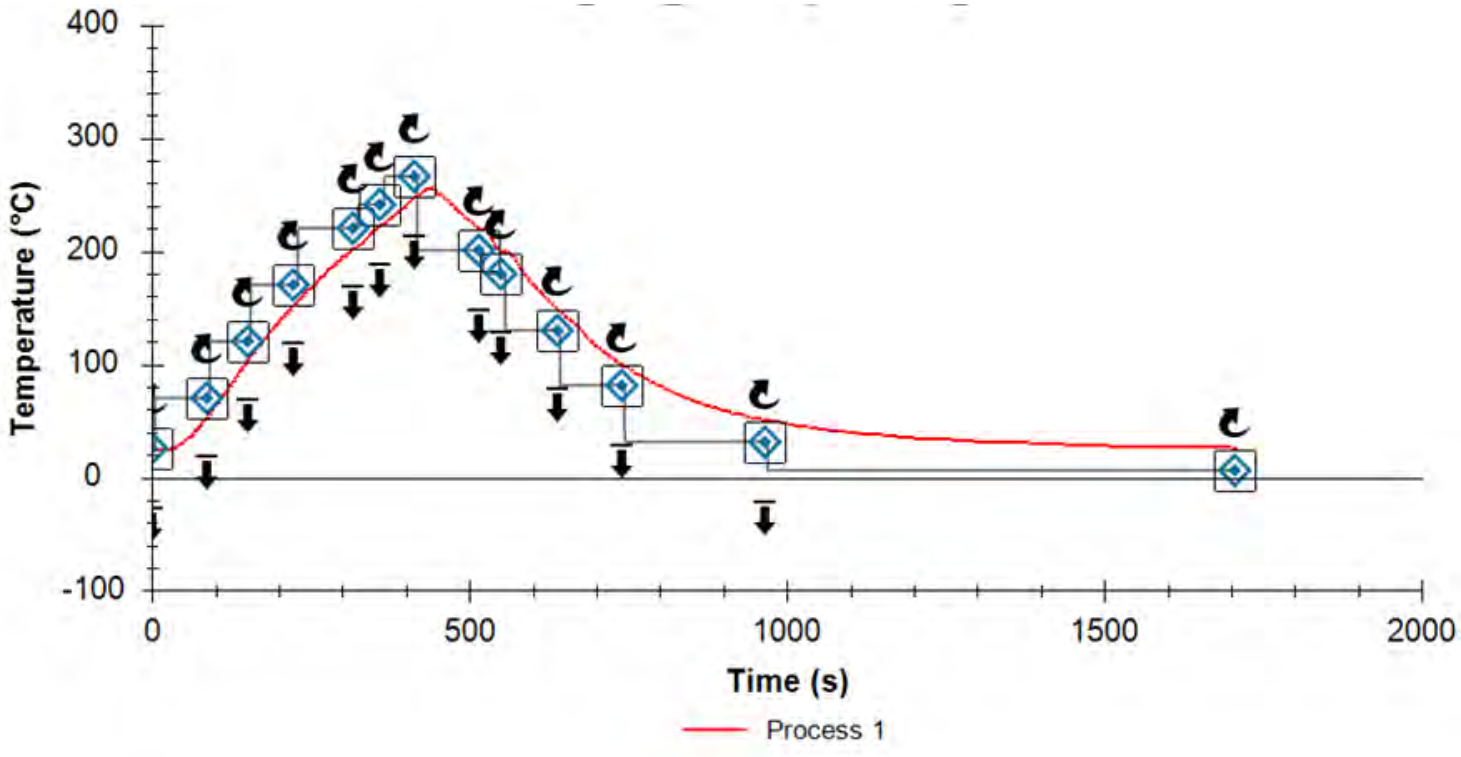


Figure 5. Thermal profile output.

Smaller package samples were supported on Robax glass with controlling thermocouple attached to the top surface of a dummy sample for testing. The larger package samples were supported by metal rails along the horizontal edges with a controlling thermocouple on the bottom surface. There were test setup samples with both top and bottom surface thermocouples run with the thermal profile used in all subsequent tests to optimize the oven time and temperature settings to ensure a top/bottom uniformity of +/-5°C or less. PCBs were tested on metal rails held from the edges with thermocouple attachment to the bottom surface. All other test setup variables were kept the same between sample measurements. Example setups of the package and PCB samples are shown in **FIGURE 6** and **FIGURE 7**.

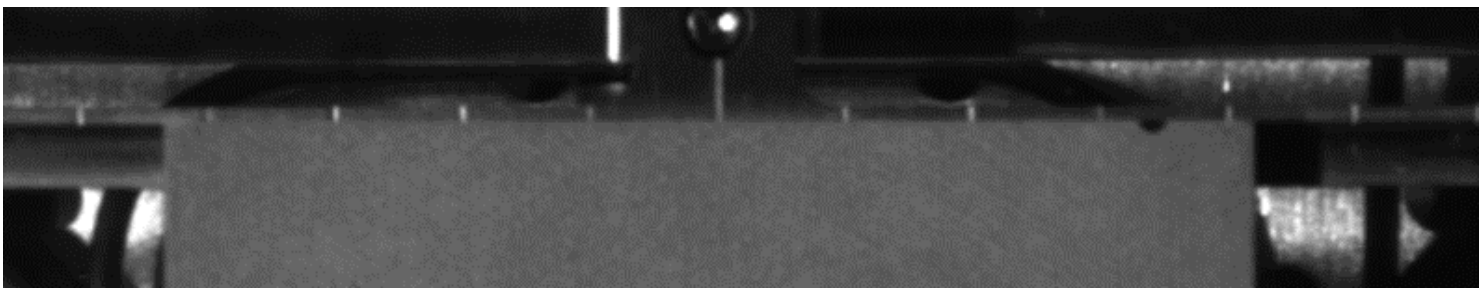


Figure 6. Package samples (top smaller BGAs, bottom larger BGAs) test setup in oven.

Figure 7. PCB sample test setup in oven (blurred to protect manufacturer).

Shape matching. Here only two PCBs are tested. Different local areas from the PCB are digitally extracted to match the specific size of the BGA land area. For the smaller BGA, three local areas are chosen around the PCB, thus two PCBs and three local areas are compared across temperature to the six smaller BGA samples. Similarly, two local areas are chosen with physical size matching the larger BGA, thus four regions of comparison are created across temperature. Note that the BGAs and PCBs are not specifically units that are assembled together in a real-world production scenario.

Offset methods and gauge choices to quantify 3-D shape are another critical decision. In this study, closest point touching is exclusively used as the offset method. This addresses how top and bottom surfaces are combined together for comparison. With all offset methods, sample Pin 1 location and measured surface, inner or outer, are tracked in sample metadata for use in software comparisons. For gauges, maximum gap will be the data focus. Other gauges such as average gap and compatibility, however, could be useful gauges to consider. These gauges are defined as follows:

- Closest point touching: offset method – The top and bottom surfaces are brought together with their LSF (least squares fit) planes parallel until the first point touches.
- Maximum gap: The maximum distance between the top and bottom surface out-of-plane.

- Average gap: The average distance between the top and bottom surface out-of-plane.
- Compatibility: The RMS (root mean square) deviation between the top and bottom surface out-of-plane.

Room temperature interface analysis. The most basic iteration of using shape matching to decide mating surfaces is purely to consider both shapes at room temperature only. In **FIGURE 8**, artificially created surfaces are used to demonstrate the concept.

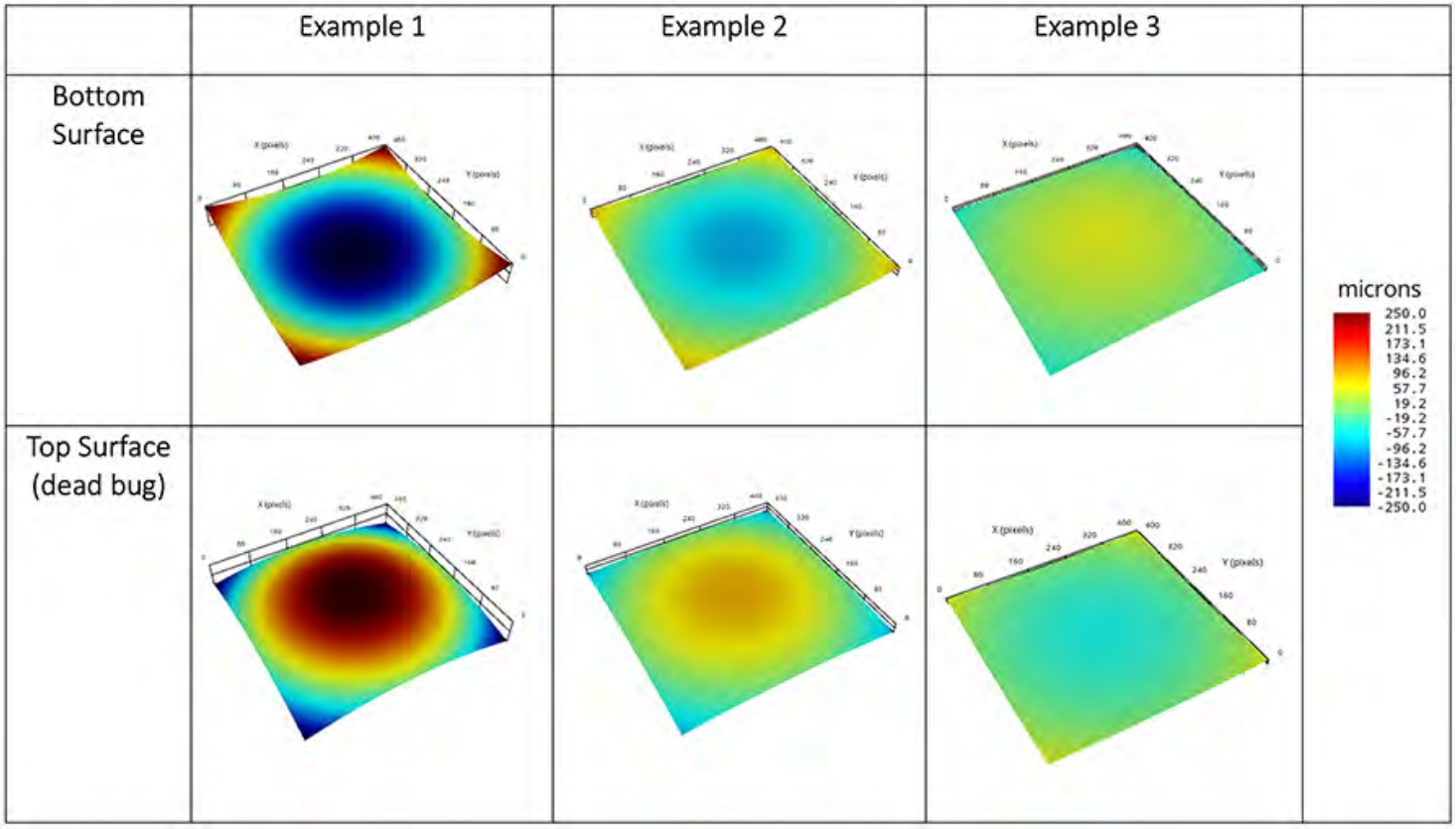
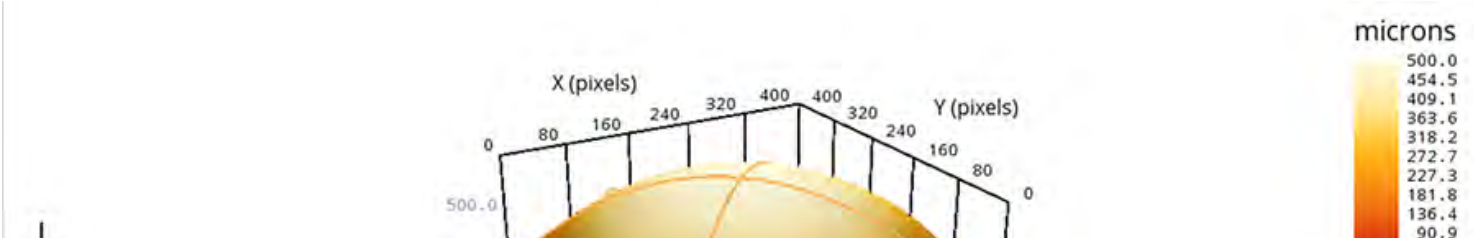


Figure 8. Surface matching example.

In Figure 8, flipping top surface 1 onto bottom surface 1 as they would be assembled creates a surface with no gap, a fully flat plane. The same is true for examples 2 and 3. However, assembling top surface 3 onto bottom surface 1 would create a surface with significant shape between the mating surfaces **(FIGURE 9)**.



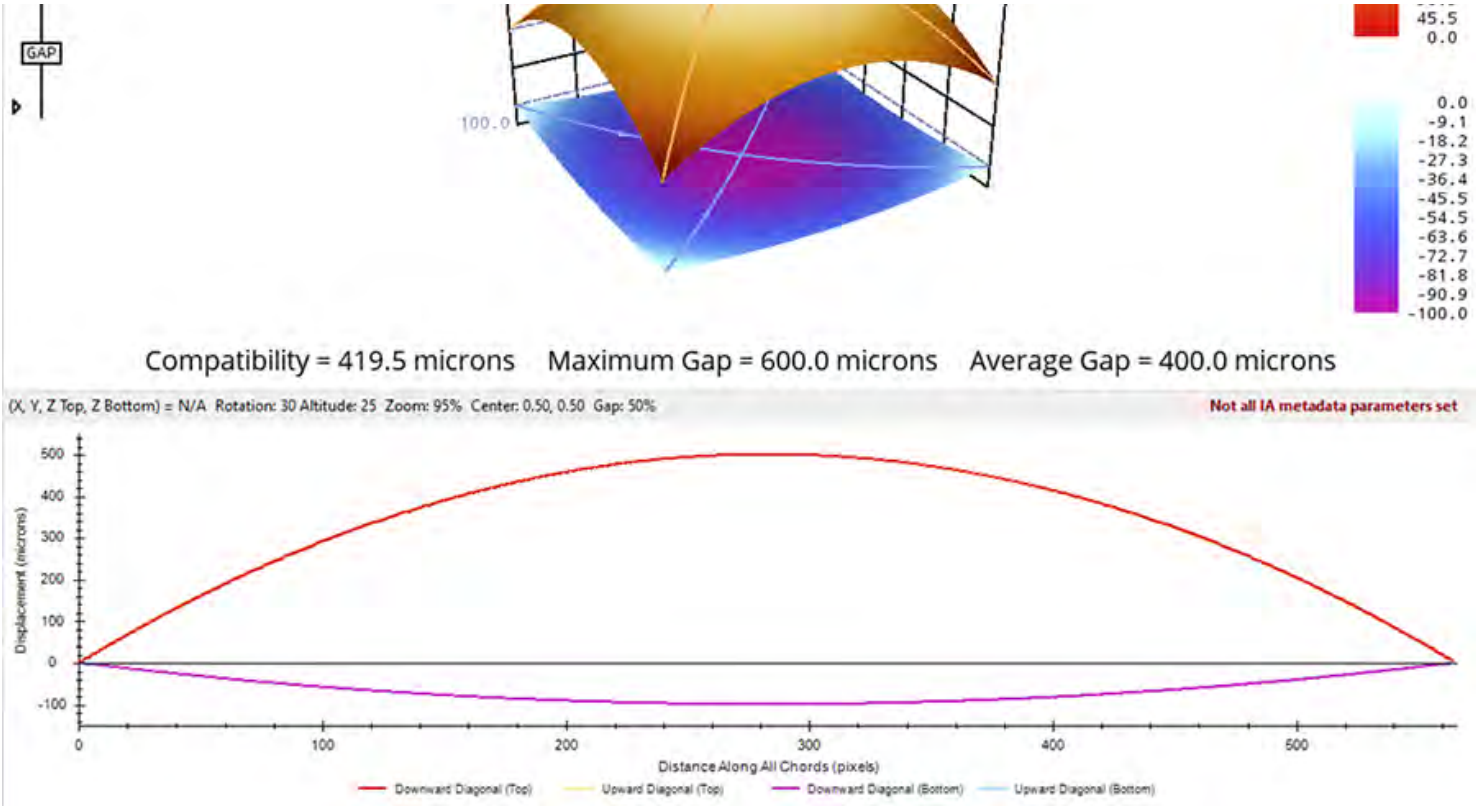


Figure 9. Interface analysis of poorly matched mating surfaces.

Figure 9 shows the potential importance of selectivity in which samples to mate. In a real-world scenario, the differences between samples are unlikely to be this extreme, but studies have shown that sample variation even at room temperature can affect product yield.[19]

Prediction of relative shape change in thermal warpage. While matching surfaces based on room temperature shape is a possible approach to improve yield, here the argument is made that a prediction of what surface shapes will be at a critical point during reflow is the more valuable data point. The area around solder liquidus is of particular interest for good solder joints. It is hypothesized here that a collection of thermal warpage data can be used to predict the relative shape change of a surface over temperature. To create this data set, relative shape change from room temperature to solder liquidus is rendered. These surface matrices are then averaged together to predict the relative shape change of the sample using only room temperature data. Examples of this process are shown in actual measurement results.

Results

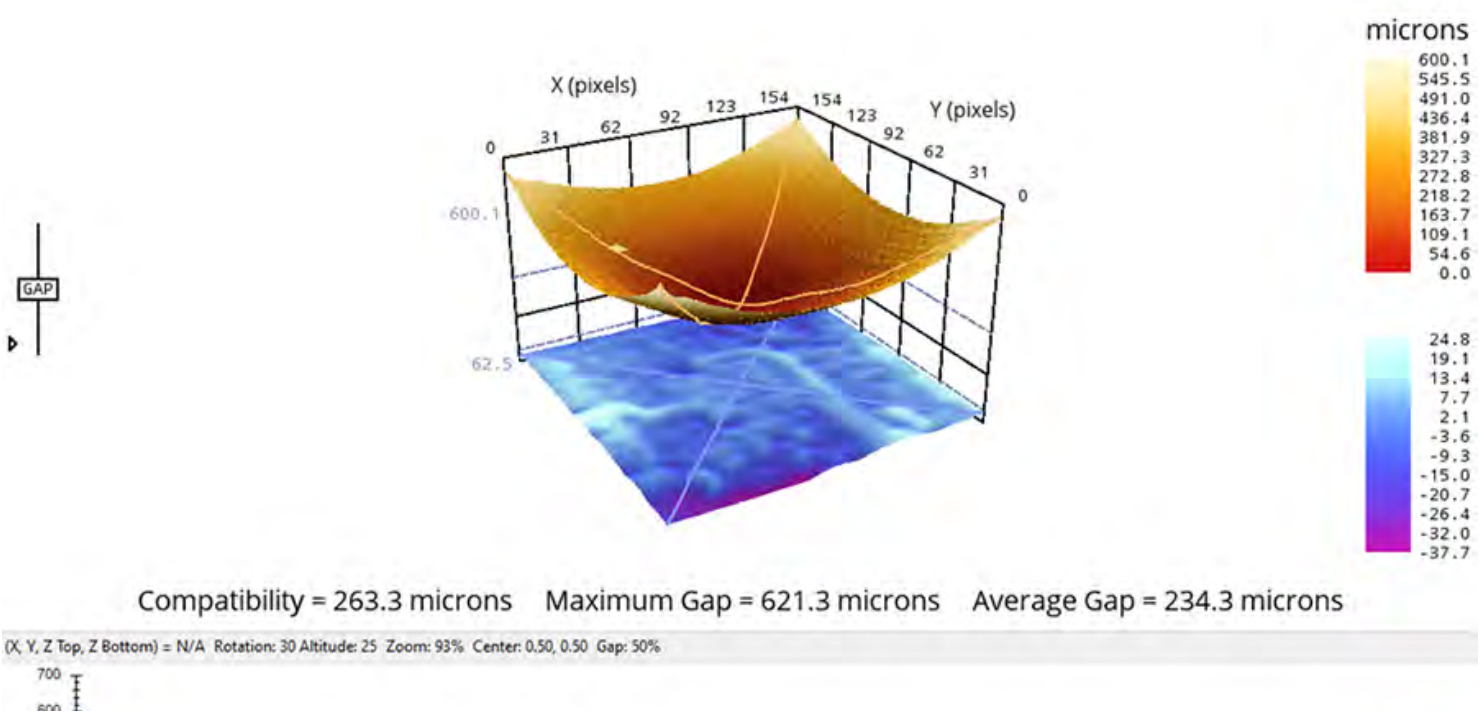
Data were taken through a full reflow profile as shown in Figure 5. However, only room

temperature shape and shape at 220°C on the cooling side of the profile is analyzed in this study. Warpage result gauges are presented in microns throughout.

Room temperature interface analysis. **TABLE 2** shows the maximum gap in microns at room temperature of the six smaller BGAs interfaced with PCB1 and two at all three ROI (regions of interest), considering every possible combination. **FIGURE 10** shows one example interface graphically.

Table 2. Room Temperature Maximum Gap of all Interface Combinations, Smaller BGA

	BGA1	BGA2	BGA3	BGA4	BGA5	BGA6
PCB1-ROI1	592.6	533.0	522.4	504.5	533.6	596.0
PCB1-ROI2	621.3	562.6	544.4	533.6	562.3	592.1
PCB1-ROI3	626.9	567.4	575.0	538.8	567.7	648.1
PCB2-ROI1	617.7	557.6	540.2	530.2	558.7	592.4
PCB2-ROI2	585.7	527.6	509.3	507.2	526.7	554.7
PCB2-ROI3	614.6	555.9	534.9	527.0	553.4	588.5



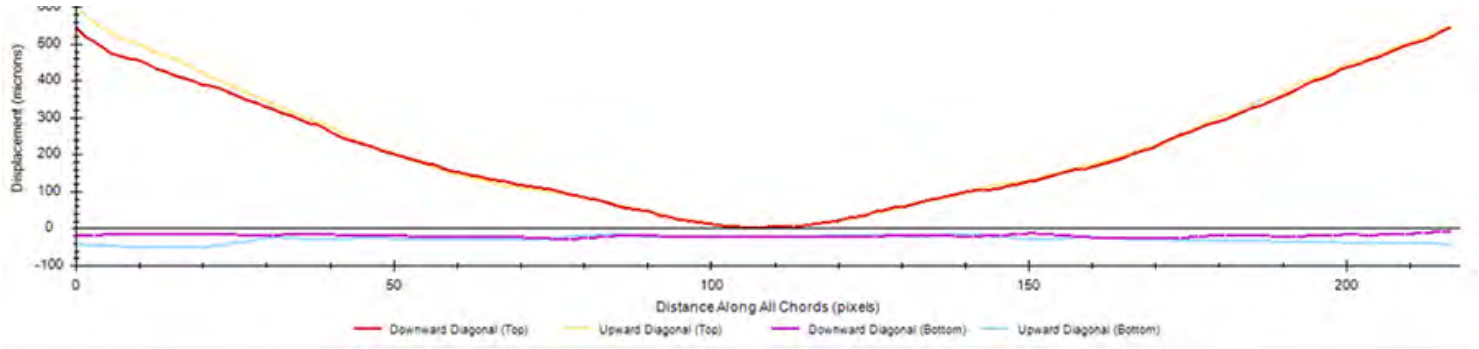
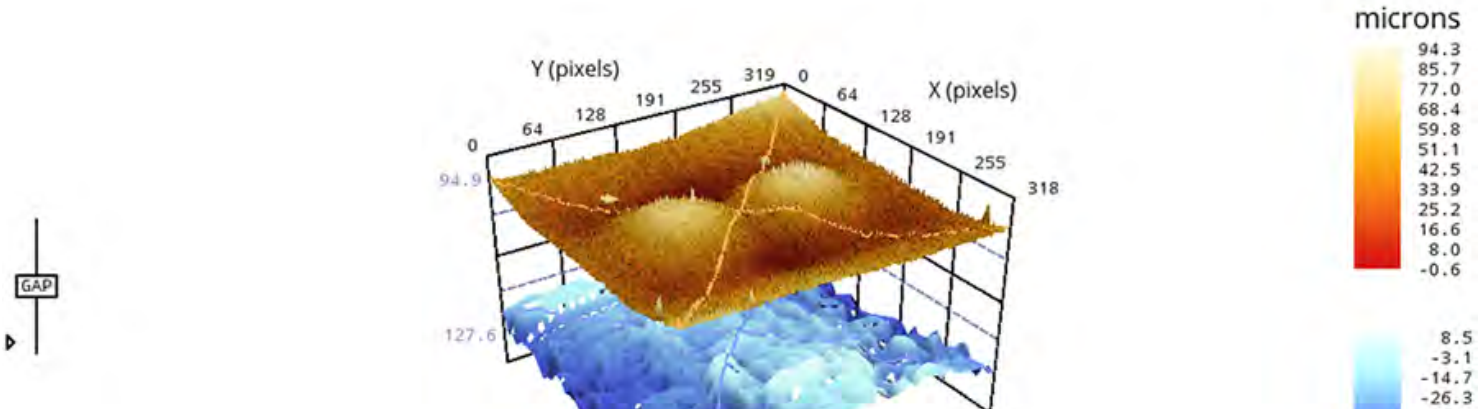


Figure 10. Room temperature interface analysis between smaller BGA 1 and PCB 1 – ROI 2.

TABLE 3 shows the maximum gap in microns at room temperature of the four larger BGAs interfaced with PCB1 and PCB2 at ROI 2, considering every possible combination. **FIGURE 11** shows one example interface graphically.

Table 3. Room Temperature Maximum Gap of all Interface Combinations, Larger BGA

	BGA 1	BGA 2	BGA 3	BGA 4
PCB1-ROI1	117.8	123.5	131.1	132.8
PCB1-ROI2	170.3	172.3	216.9	196.5
PCB2-ROI1	170.8	166.3	195.3	166.5
PCB2-ROI2	356.1	369.3	371.2	404.5
PCB2-ROI2	585.7	527.6	509.3	507.2
PCB2-ROI3	614.6	555.9	534.9	527.0



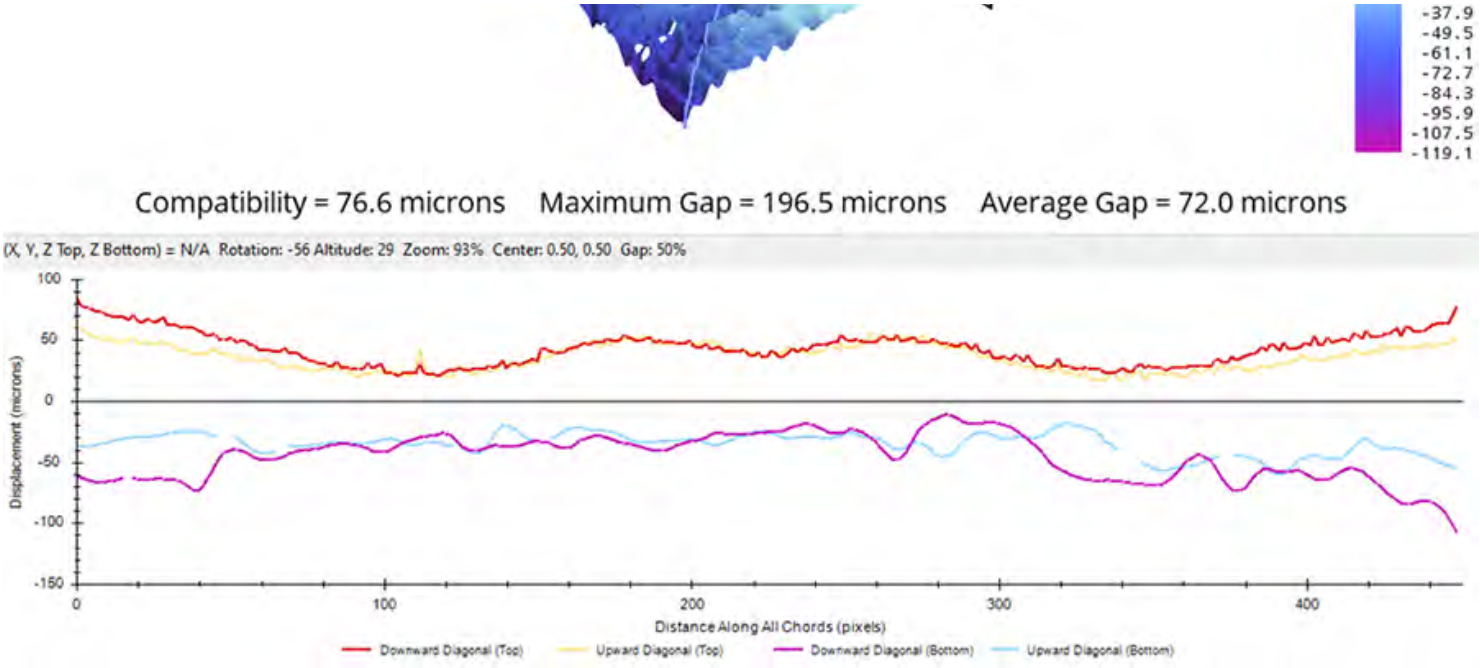


Figure 11. Room temperature interface analysis between larger BGA 4 and PCB 1 – ROI 2.

Interface analysis at actual solder liquidus. Since we have thermal data for all samples, here we analyze interface gaps at a solder liquidus of 220°C on the cooling side of the profile. Later this shape will be predicted using an average of relative shape change from room temperature to 220°C. **TABLE 4** shows the maximum gap in microns at 220°C of the six smaller BGAs interfaced with PCB1 and 2 at all three ROI, considering every possible combination. **FIGURE 12** shows one example interface graphically.

Table 4. Solder Liquidus (220°C) Maximum Gap of all Interface Combinations, Smaller BGA

	BGA 1	BGA 2	BGA 3	BGA 4	BGA 5	BGA 6
PCB1-ROI1	376.0	456.9	430.8	482.3	422.7	447.7
PCB1-ROI2	362.1	439.5	417.9	454.9	404.9	420.9
PCB1-ROI3	335.9	408.8	381.4	447.1	362.1	383.2
PCB2-ROI1	353.6	438.1	419.3	455.5	405.4	426.4
PCB2-ROI2	374.2	452.4	411.3	462.3	403.4	411.8
PCB2-ROI3	364.8	442.6	441.1	446.5	404.0	436.7

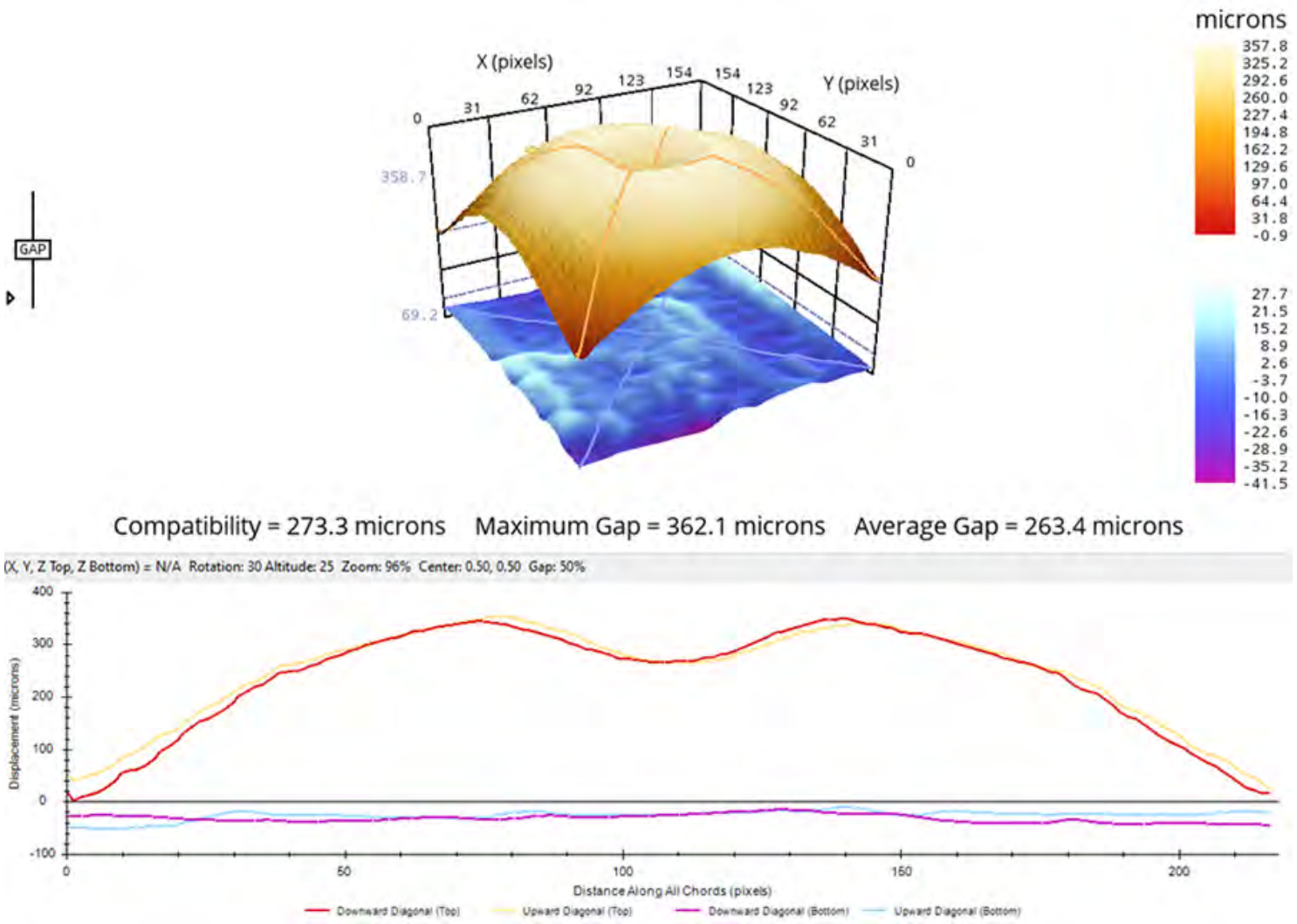


Figure 12. Solder liquidus (220°C) interface analysis between smaller BGA 1 and PCB 1 – ROI 2.

TABLE 5 shows the maximum gap in microns at solder liquidus of 220°C of the four larger BGAs interfaced with PCB1 and PCB2 at ROI 2, considering every possible combination. **FIGURE 13** shows one example interface graphically.

Table 5. Solder Liquidus (220°C) Maximum Gap of all Interface Combinations, Larger BGA

	BGA 1	BGA 2	BGA 3	BGA 4
PCB1-ROI1	151.2	145.0	158.7	149.2
PCB1-ROI2	246.5	249.5	250.7	280.7
PCB2-ROI1	208.4	208.6	239.7	210.8
PCB2-ROI2	237.6	229.9	253.8	260.1

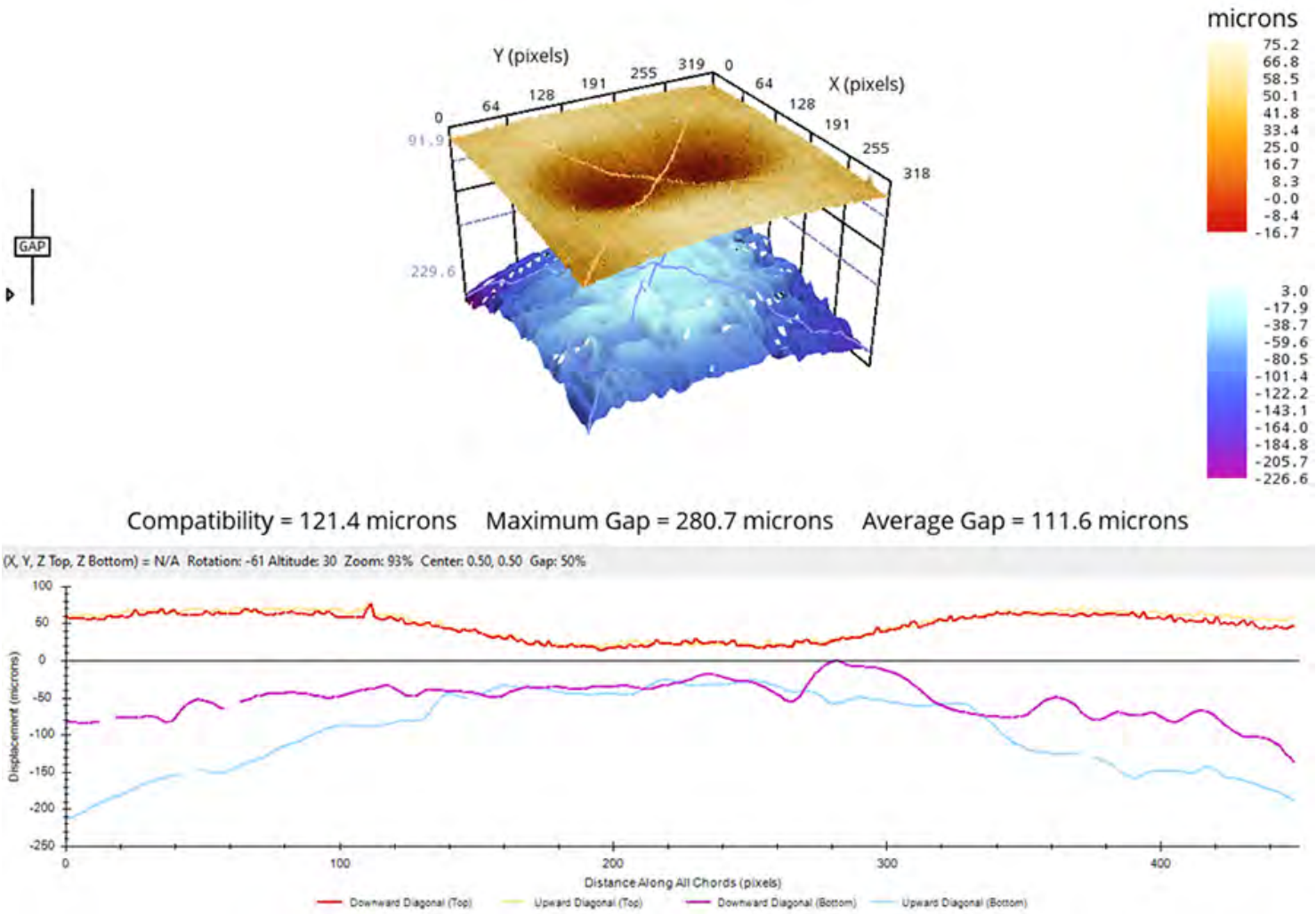
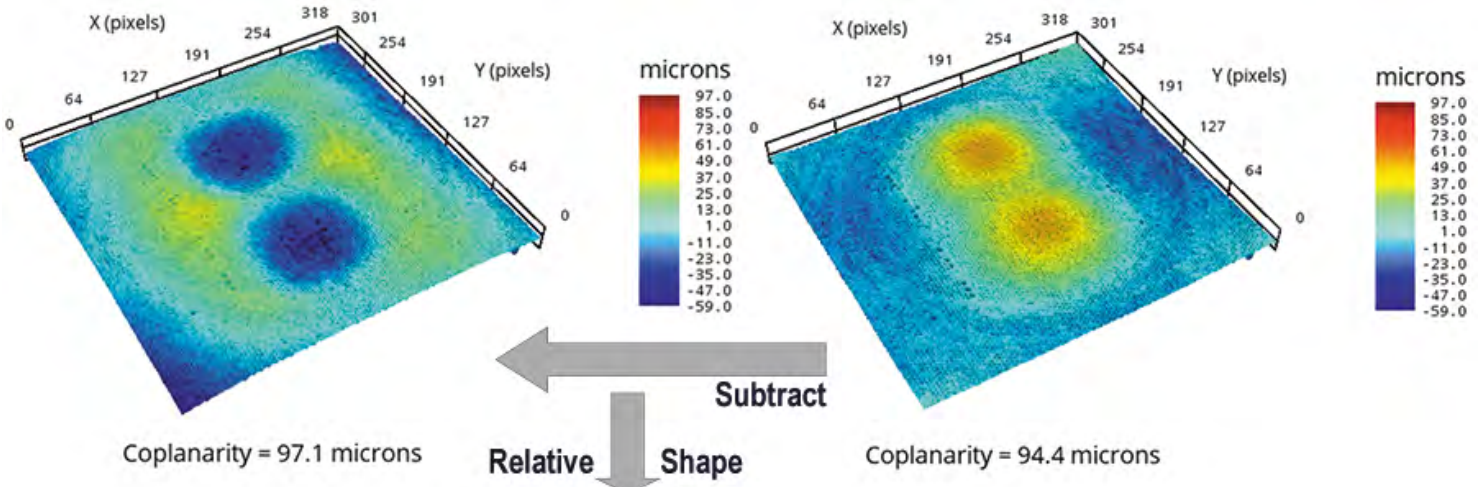


Figure 13. Solder liquidus (220°C) interface analysis between larger BGA 4 and PCB 1 – ROI 2.

Relative shape change room temperature to solder liquidus. For each measured surface, the relative shape change between room temperature and 220°C can be found by subtracting the room temperature surface from the 220°C surface as in **FIGURE 14**.



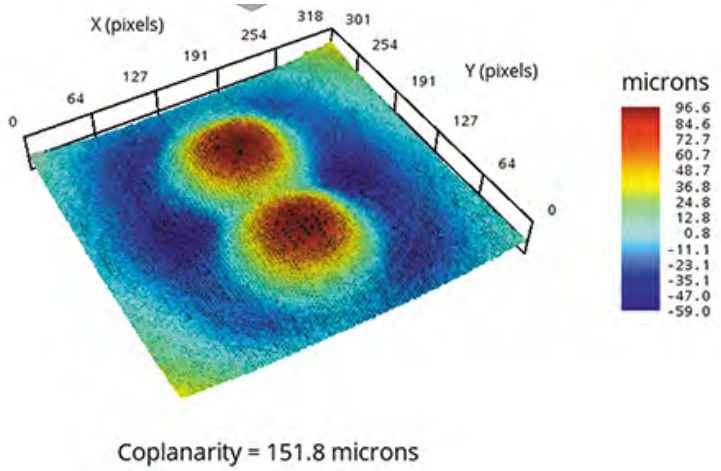


Figure 14. Relative shape change in BGA 4 from room temperature to 220°C.

This process is repeated for all surface data. Then relative surfaces for each ROI are averaged together. **FIGURE 15** shows the four average relative warpage change surfaces for the PCB and BGA in larger and smaller sizes between 220°C and room temperature.

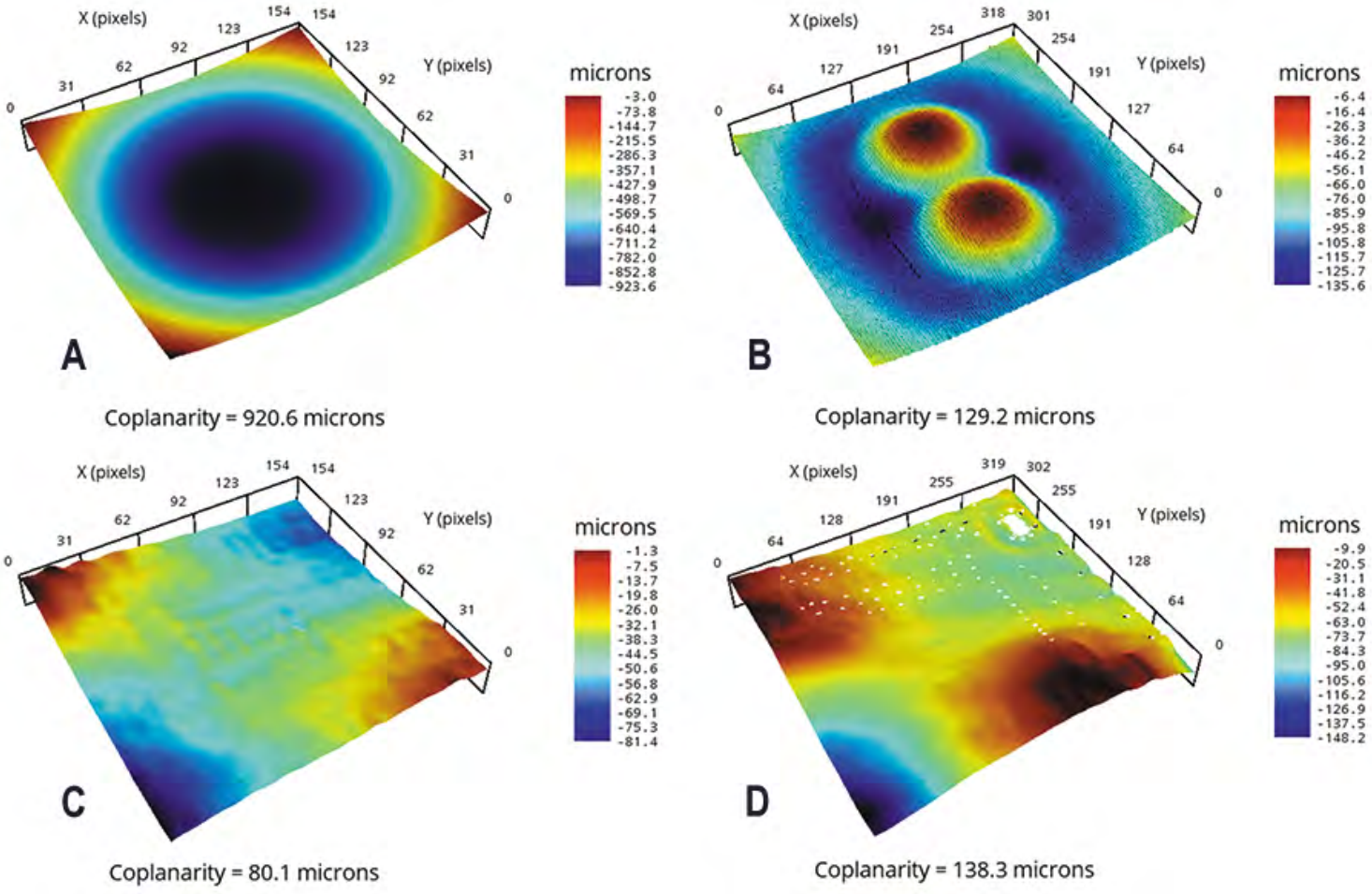


Figure 15. Average relative shape change from room temperature to 220°C; a) smaller BGA, b) larger BGA, c) smaller PCB all ROI, d) larger PCB all ROI.

Prediction of shape at solder liquidus based on average shape change. The final step is to use these averaged surfaces, applying the shape change to the room temperature surface to try and predict what the shape will be at the critical solder liquidus point in the reflow profile. The example from Figure 14 can be used again in **FIGURE 16**. The average relative shape change is inverted and then subtracted from room temperature data to predict the solder liquidus shape.

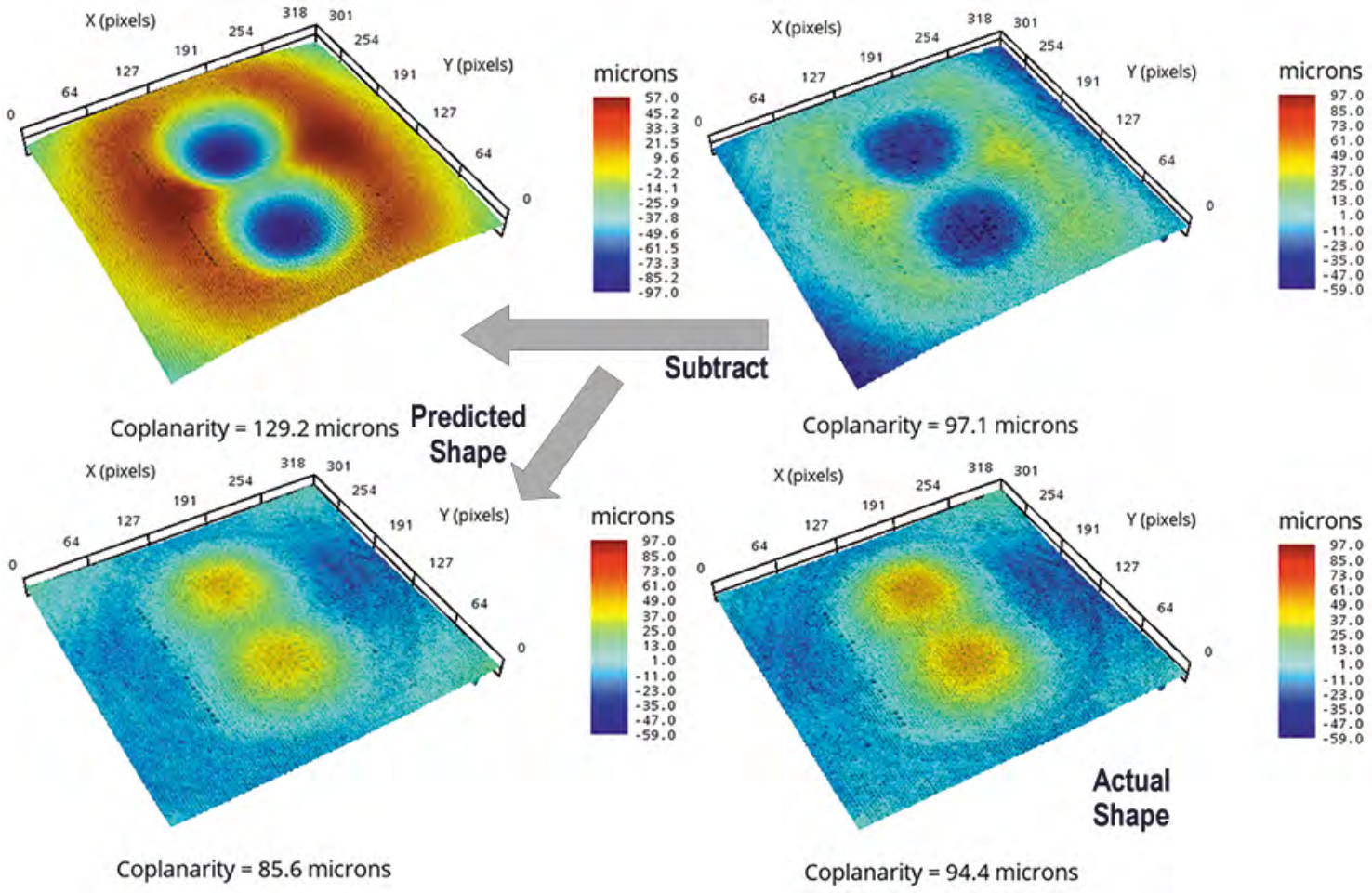


Figure 16. Predicted larger BGA shape at 220°C based on room temperature shape and average relative shape change.

This same process can be repeated for all surface to recreate max gap numbers using the relative shape change prediction and actual room temperature shape of both PCB and BGA surfaces. The hope is to find similar numbers found in Tables 4 and 5. Given the highly different shape changes of the multiple PCB regions, only ROI 1 from the PCB data is used in this process. The overall concept of this predictive method is that shape change over temperature is somewhat repeatable for samples of equal design and production conditions. **TABLES 6** and **7** show the results from the transformed room temperature data.

Table 6. Predicted Maximum Gap at Solder Liquidus of Interface Combinations, Smaller BGA

	BGA1	BGA2	BGA3	BGA4	BGA5	BGA6
PCB1-ROI1	455.4	597.0	486.0	534.0	490.9	424.2
PCB2-ROI1	454.5	593.8	461.3	529.9	486.7	395.2

Table 7. Predicted Maximum Gap at Solder Liquidus of Interface Combinations, Larger BGA

	BGA1	BGA2	BGA3	BGA4
PCB1-ROI1	154.8	167.4	204.4	190.2
PCB2-ROI1	179.1	197.7	214.5	200.5

Discussion

Shape prediction accuracy. Further data analysis starts with qualifying the accuracy of the predictive approach in using average relative change over temperature to predict sample shape at temperature. **TABLES 8** and **9** show the percentage error of actual maximum gap between interfaces at 220°C and the predicted gap.

Table 8. Prediction Error of Maximum Gap at Solder Liquidus of Interface Combinations, Smaller BGA

	BGA1	BGA2	BGA3	BGA4	BGA5	BGA6
PCB1-ROI1	28.50%	35.50%	10.00%	16.30%	20.10%	-7.30%
PCB2-ROI1	21.10%	30.70%	12.80%	10.70%	16.10%	-5.20%

Table 9. Prediction Error of Maximum Gap at Solder Liquidus of Interface Combinations, Larger BGA

	BGA1	BGA2	BGA3	BGA4
PCB1-ROI1	16.40%	5.50%	11.70%	5.10%
PCB2-ROI1	-2.30%	-13.40%	-22.40%	-21.60%

The error in the prediction is significant. This could be attributed to the age and unknown history of the samples used, however. The PCBs and small BGA were both older products with unknown thermal history. Realistic samples of the application may see different results under this presented model. Notably, the larger BGA was the more realistic and more modern package used in the study, and it showed more consistent change under reflow temperatures. While the error was significant in Table 9, predictions are consistently high for PCB1 and low for PCB2, suggesting variation in the PCB could be the larger inconsistency. Larger data sets may also aid in establishing a baseline relative thermal warpage change.

Practical production implementation. The approach proposed in this study assumes a percentage of destructive thermal warpage testing on samples in question. This is an industry practice used by many companies, with referenced standards.[7-9,11] It also assumes 100% flatness inspection of both bare PCB surface mount attach areas, however, as well as flatness measurement of designated high-value components. Flatness inspection of these items is not standard industry practice.

Physical space and methodology to take these measurements must be considered. PCBs would need to be measured prior to solder paste application. Measuring components within tape-and-reel is likely unrealistic. But, many high-value components will be presented to pick-and-place machinery in JEDEC trays, making automated flatness inspection during assembly more viable. Components in JEDEC trays would also typically be sitting live bug, such that the topside is visible for measurement instead of the attach side. Industry standards for thermal warpage instruct measurement of the attach side, but they also include removal of solder balls when present, which is not practical for production, given the destructive nature.[7-8] Therefore, correlation of the shape on top of the

sample may be needed, unless further complexity is added to inspect the attach side of the component. Even in this case, BGA components have the challenge of measuring substrate surfaces between the solder balls, which presents some metrology challenges for more densely populated components. With the availability of optical metrology techniques, measuring sample shapes can be done at high speeds relative to typical reflow production processes and are not expected to increase production times.

Communication with pick-and-place machinery would be required to implement such a solution. The level of communication required would be highly simple, however, only needing to indicate which samples should be picked up next. Additionally, possible physical integration between pick-and-place tools and JEDEC loading mechanisms may be required. Measuring samples as they are loaded into the pick-and-place tool would be a likely place to capture component shape, possibly taking multiple measurements per tray to improve measurement resolution, versus requiring motion systems for the metrology optics or multiple optical hardware setups.

The quantity of available data upon which to make decisions would depend on the timing of the assembly process. The discussed examples assume that a handful of data are available at the same time to place combinations of samples together. The criteria for making this decision could be numerous, including many different types of gauges, including the referenced average gap and compatibility gauges. This could potentially also include a level of criteria that would fail inspection and be removed from the assembly process. A failure level is not required for the approach.

The portability of the DFP technique may be a better fit for a production scenario. Studies have shown that DFP and shadow moiré techniques can be correlated with appropriate control of variables.[17] Thus, the shadow moiré technique could be used for thermal warpage data and establishing average relative change data, even if DFP is used for production flatness measurements.

Conclusions

A potential approach to improve yield in the reflow assembly process is presented. The approach and data presented here are only a first phase concept, rather than a fully established solution for implementation. Further studies, using more realistic mating samples, is the recommended next step. Further steps include establishing conditions for acceptable interface gaps, further studying

product warpage and production yield, communications with production equipment, and creation of production tools for warpage measurement of samples at room temperature.

Error in the prediction scheme is significant. The error here may come down with more realistic samples and larger product samplings. While the error is significant, the study also shows that the gaps between the samples at room temperature and at critical solder liquidus temperatures are noticeably different. Thus, using room temperature shape differences alone is not expected to provide the necessary information for selectively assembling component to board.

Strong control of product history and realistic reflow emulation in thermal warpage metrology will be essential to enable prediction of surface shapes at critical points in the reflow process.

Acknowledgments

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LEGISLATION

Public Sector Efforts 'Chip Away' at PCB Funding Deficit

The PCBAA is ramping up efforts to secure funding for R&D and capacity in the US.

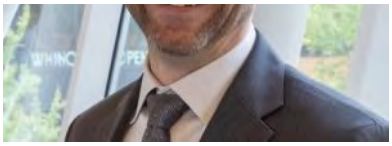
by MIKE BUETOW

What constitutes the printed circuit board industry? And how much, if any, investment should the US government allocate toward ensuring its technological and capacity capabilities?

These are among the questions David Schild is tackling every day. Schild is executive director of the Printed Circuit Board Association of America, which was founded in 2021 to advance US domestic production of PCBs and base materials. The organization is made up of corporate members of all sizes and includes fabricators, assemblers and suppliers.

Schild addressed questions about public and private investment, how governments can help create "demand signals," and the PCBAA's annual meeting with PCEA for the ~~PCB Chat podcast~~ in late July. The following transcript has been lightly edited for clarity and length.

Mike Buetow: You came to PCBAA in November after years spent serving the aerospace and defense industries. [In June] PCBAA had its annual meeting, which I believe was your first as executive director. Let's get your initial thoughts on that meeting and the priorities that came out of it.



David Schild, PCBAA
executive director

David Schild: This was our second annual meeting in Washington, DC. As you mentioned, we're a new association but growing rapidly. We doubled year-over-year from the 2022 to the 2023 annual meeting. And I was just thrilled that so many of our leaders gave their time and their talent for a couple of days in Washington, both to hear from the experts – officials from the Department of Commerce and from the Department of Defense, elected officials and staff from both the House and Senate – but also to do the hard work of lobbying, to go up to Capitol Hill and wear out the proverbial shoe leather so that we can advocate for our industry. Great meeting.

MB: Several industry leaders sent a letter in June to the Appropriations Committee and the Defense Appropriations Subcommittee in the US Congress. In it, they pushed for $100 million in the next budget to implement President Biden's designation of printed circuit board and IC substrates as technologies that are critical to US national security. What has to happen to make this a reality?

DS: I'm glad you brought this up. The invocation of the Defense Production Act was a long-time legislative priority for our group, and our coalition more broadly. It's great to see at the highest levels of government an official designation that printed circuit boards and IC substrates are critical national assets. We share that view completely now. We have to invest the money. The DPA is really a hunting license and, once it's granted, you sort of have to put some bullets in the gun, some arrows in the quiver, as it were, and what we're looking for is a $100 million appropriation that would go to the Department of Defense budget and that would allow investment in rapid prototyping, research and development, the kind of things that we're going to need to invent the next generation of technologies in this particular segment. The appropriations process is something that happens every year. Everybody and their brother is looking to add monies to that process, but certainly we're going to push hard for this $100 million as a down payment. It's not all that we need, but the Department of Defense recognizes that next-generation microelectronics are going to power everything that our war fighters use, and we need a strong domestic capacity to produce those

technologies.

MB: Would that $100 million be part of the National Defense Authorization Act?

DS: No, I'm glad you mentioned that. There's a distinction between the NDAA, which is an authorizing document, writing out policies, procedures, and guidelines for the Department of Defense. I'm oversimplifying, of course, [but] for the appropriations process, we have a bill for pretty much everything the government does, from agriculture to education to defense. We need the policy language that's in the NDAA, and I can talk about more specifically what hits printed circuit boards, and we need actual dollars appropriated through that annual appropriations process.

MB: OK. I want to circle back to the NDAA in a moment, but let's just say that $100 million appropriation happens. What does the roadmap look like insofar as where it's applied? In other words, why $100 million and how would it be spent? For instance, there's been a lot of focus on chiplets of late, but of course most US manufacturers have little to no experience building that technology. Would that be a focal point?

DS: I think anything that's an emerging technology is something the Department of Defense is looking at. I don't want to speculate too much on how that money would be specifically allocated because my sense is that the DoD is going to open the window, as it were, and they're going to say, "Hey, come to us with your ideas, with your proposals." [There are] several offices within the Department of Defense, in the acquisition technology and logistics space; you have an Executive Agent dedicated to printed circuit boards out of Crane in Indiana and these offices, I think, want to see companies stepping up with proposals to say, "This is the problem that you've designated, and this is our technology solution." That $100 million can get used up pretty fast on cutting-edge prototypes and research and development. But if we were to mirror the way it's been done in the past, I think you would see the Department of Defense saying specifically, "These are the problems that we need to solve, industry. What are your solutions and what do you need to make that happen?" And there would be a call-and-response there. That's what we've seen with other smaller allocations like this.

MB: So the expectation would be, then, companies would go to the US government and apply in the form of grants or other kind of funding for that money? Or would there be a

third party that would be responsible for allocating it?

DS: Typically the Department of Defense will make direct investments. Different government agencies do it differently. And again, I don't want to get too much in the weeds about the procurement process and how some of these grants would work. The Department of Defense does have a different process than, say, the Department of Commerce, which is administering the CHIPS program. But I think that they understand that all these future technologies are going to power everything from submarines to satellites, and there is a concern about the industrial base, right? What you see at the Department of Defense when they talk about these kind of investments is thinking not just six months, but six years or even 60 years ahead to say, "Hey, can we make the things that we need for future conflicts, future challenges that the department might face?" They're trying to get ahead of a problem right now.

Our industry does a tremendous job of meeting the need for secure and trusted microelectronics that go into everything that floats or flies, as we say. But I think there's a concern about the next-generation technology set. Are we going to invent it here in America? Because if it's not invented here, we become deployment-dependent on foreign sourcing. That obviously makes the DoD nervous. Hence, the desire to make some of these initial investments. And again, this is an industry push for the $100 million. This is our industry saying, DPA simply allows you to spend. Now let's put our money where our mouth is.

MB: Do you think the actions going on right now in Ukraine and Russia have created any kind of sense of urgency among the congressional members insofar as saying, "Wait a minute. If we're seeing how much supply we're using for something that we're not directly involved in, what do we need to do to ensure we have the capacity if we are directly involved?"

DS: Two things are happening simultaneously. I'm glad you brought this up. Number one, there's a greater recognition of the high-tech nature of modern weapon systems. The conflicts of today and into tomorrow are being fought with extremely high-tech systems that rely on, among other things, microelectronics. Certainly, we're not the only industry that has some light shining on it right now. You see critical minerals. You see specialty metals, alloys, even issues of workforce, labor concerns: Do we have enough people who can do these special skills? So one, I think everybody sees what's

going on in that particular conflict and says, “OK, high-technology munitions, high-technology defense systems, this is the way that battles are being fought.”

The second part of that, I think, is an understanding that we are burning through some of our stockpiles. We are making significant debits against some of our inventory and those are going to need to be replenished. Again, I’m not hearing any problems right now meeting the demand coming out of the Department of Defense. What I think we recognize is that defense-focused industries often need their commercial partnerships, their commercial side of the factories, to keep everything healthy. You see this with military engines, at companies like, let’s say, Pratt and Whitney, you see this with national space applications where if commercial launch is suffering, defense launches face challenges. I think there’s a similar analogy in our industry where we want to have a commercial space that is healthy, that is productive, that is profitable, because it enables the defense line, which is much smaller, much more bespoke, to be sustainable.

MB: Now I want to point out that of the 26 companies that signed that letter, a third of them are primarily in the assembly space. So you’re not just working to assist the fabrication side.

DS: No, absolutely not. PCBA has critical material suppliers, it has assemblers, it has PCB manufacturers and we’re hoping to welcome more substrate companies, an emerging area of growth in the United States, a place that we’ve got to do better, I think 99% of our IC substrates are made overseas because upstream and downstream of the boards themselves, there is a real impact here. The $3 billion that our PCBs Act calls for would be available to anybody who makes boards or substrates, but the 25% tax credit is really the game-changer because it would apply to anybody buying American printed boards or substrates. So now you’ve got any company using these technologies saying, “I want to reassure, I want to diversify my supply chain. I’d like to buy more things in America. But it’s not cost-competitive.” The tax credit gets you there.

MB: Changing gears for just a moment, the bipartisan HR3249, better known as the Protecting Printed Circuit Boards and Substrates Act of 2023, is seen as a necessary adjunct to the CHIPS Act. Its goal is to incentivize investment in the US PCB industry. It calls for, among other things, $3 billion to fund factory construction and modernization, workforce development and R&D. And it also calls for a 25% tax credit

for purchases of American made PCBs and substrates. I think it has five cosponsors so far. What can you tell us about the status of that bill?

DS: It's been referred to several committees of jurisdiction and we are building a strong base of support. I know that our coalition is meeting every week with lawmakers virtually and in person to appeal to them to support the bill. The more cosponsors we get, the more of a snowball effect that we build, of course. Congress has been consumed lately with spending bills, raising the debt ceiling, moving several critical bills like the NDAA forward. But I think what we are trying to do now is the educate part of our educate, advocate and legislate mission. One thing the semiconductor industry did very, very well was teach everybody how essential semiconductors are to modern life. We need to accomplish the same thing with printed circuit boards and substrates. We need to make people understand that there is a technology stack at work. That's one of the first conversations we have with members of the House and Senate: If I hold this green board up, do you understand its role in the ecosystem? Do you understand how critical this is? We used to make 30% of the world's supply here in America. Now we make 4%. That's an unhealthy contraction. That's a concerning dependence on foreign sourcing. And sometimes you see people's eyes light up and they're like, wow, I didn't know this. They of course know it about semiconductors. Our friends in the semiconductor industry did a tremendous job of getting the word out. We need to do the same thing. The PCBs Act will pick up more and more support, I'm convinced, once we explain to more and more elected officials our role in the ecosystem.

Figure 1. The success of the CHIPS Act is seen as a roadmap to the subsequent PCB bill.

MB: And that's 4% of the value of the output. It's not 4% of the total production output, which would be probably even less because that would be on a square foot basis. The volume of these boards being produced in Southeast Asia is so much greater than what we're doing here. They're just generally lower-cost boards.

DS: The President said something in the State of the Union last year that I really agreed with: "If we invent something in America, we should make it in America." We have been the leader in innovation in this space. One of the things that our chairman Travis Kelly talks about a lot is that research and development and design are often colocated with production. When you take a PCB or a substrate factory and you move it over, you can certainly produce a lower-cost good, but what happens is that the next-generation technology is being invented there colocated with production. We lose the capacity to build these things, but we also lose the know-how, the intellectual power that will design the next generation. That's why there's such an imperative to rebalance. No one is arguing that we should put up enormous walls and try to decouple from the world and undo a global economy that's 50 years in the making. I don't think anyone's making that argument. What we're saying is that 4% is simply not a healthy slice of the pie, and it presents real supply chain and security risks.

MB: I would agree 100% with what Travis is saying and in fact, if you look at companies like Apple, they have a huge number of manufacturing patents that they apply for every year, even though Apple doesn't "manufacture" anything. I think that there are companies that still recognize there's a strong tie between understanding how things are built and understanding what the next generation or a couple of generations down the road of design are going to look like.

I want to circle back to something you mentioned earlier about the industrial supply base. I would argue that in the great successes, the transcendent moments in American history, there's a very close tie between the government and industrial partnership. If you go down to the US Space & Rocket Center in Huntsville [AL], you can

see the first examples of surface mount boards. These are from 1964, and they are all built by IBM, not a defense contractor. Folks who were making computers had also figured out the manufacturing technology that was needed for the one-of-a-kind, at that time, space launches.

DS: We just passed the 54th anniversary of man landing on the moon, and it does give you an appreciation for the engineering challenges that had to be overcome, the technologies that had to be built to actually achieve that remarkable feat. And when you think about what's happening now with technology in general, where we need to have a decarbonization of the economy, we need to have a green tech revolution in this country, that's going to be very, very heavily dependent on microelectronics.

We want to go back to the moon. We want to go on to Mars. We want to explore the solar system. [This is] very, very dependent on cutting-edge microelectronics. I guess it's a long way of saying that we're not going to accomplish anything impressive here on Earth or out in space without the ability to invent and build these technologies, and I think that there's a sense of national pride and ownership and a desire to lead in that space, while at the same time being part of a global economic footprint. You're right. And I'm a nerd about the space program, we could talk about that all day. But when I see this tech and I realize my iPhone has more capacity now than the computer that took us to the moon, you just realize how far we've come, and it's on the backs of engineers and some of our member companies that have invented this technology and are poised to do even more in the future.

MB: Along the same lines, HR 7677, which was a similar bill to 3249 that was introduced in the last Congress, defined PCB as a circuit board on which a pattern of copper foil connects the components. The text of the current bill defines PCBs as a composite with electrically conductive and nonconductive materials, so that opens the door to, among other things, additively manufactured or electronics printed with conductive inks. Was that the reason for the change?

Rep. Blake Moore (R-UT)

DS: One of the things that we did at the end of the last Congress was our coalition circled the wagons and said when we see this bill reintroduced in the 118th, what are some improvements to the language that can be made? I'm not an engineer. We went to our member companies and said, "Are we casting the net wide enough? Is this the proper modern definition?" Because what gets written into the law is what gets applied out in the field. With the CHIPS Act, there are very specific phrases, nouns and adjectives and verbs that define where these billions of dollars go. This wasn't something at the sort of administrative level that was worked out. Our member companies said, "A more current and proper definition is really XYZ," and I give a lot of credit to Chris Mitchell and the team at IPC for assisting in that. We also added substrates because we realized in the last bill that we were falling a little bit short by limiting ourselves to printed circuit boards, that three layers of the stack – the semiconductor, the substrate and the board – are all part of the ecosystem. Many board manufacturers are beginning to get into that substrate space and they wanted that expanded definition as well. I think the language was greatly improved and I thank Representative Blake Moore and Representative Anna Eshoo for making adjustments to that bill with industry input that now I think brings it to the state-of-the-art.

Rep. Anna Eshoo (D-CA)

MB: If I'm reading it correctly, 3249 funds the factory updates for one year. Does that suggest manufacturers need to be ready to go right away if it passes?

DS: What I'm observing is that private money is following public action and here's what I mean by that. The $52 billion that the CHIPS Act allocated is starting to be dispersed. You're going to see this over probably a decade, the entirety of that money get handed out, but what's amazing is how private money is coming off the sidelines in response to public leadership. There's by some estimates $400 billion in private money going into semiconductor construction, production capacity. I think that a number of people in our industry are waiting to see where the government goes. They're prepared to act. The business case only exists if the demand signal is there. The government can help make that demand signal. Think of all these things as a down payment.

Everyone acknowledges that the CHIPS Act is a start. People believe, and I certainly believe, that the PCBs Act is a first. I think our industry is nimble. I think it's ready to invest, but of course without a demand signal, the business case isn't there. We're operating in a marketplace, so I'd like to see this bill passed. I'd like to see the tax credit create strong demand, $3 billion be available to our members immediately, but we're going to be back revisiting this issue whether this bill succeeds or fails for years to come. Travis likes to say, "We took 40 years to dig this hole for ourselves. We're not going to dig out in four months." This is a long slog, and we're ready for it.

MB: We mentioned the NDAA a bit ago. It's different from the standalone funding bills, as you noted, and it just passed the US House. Any specifics in that particular bill that the industry should be made aware of?

DS: I think one of the things that we have been around for two years pursuing aggressively is DoD policy that protects American microelectronics and secures and builds resilient supply chains, and Section 841 and Section 851 of the NDAA specifically call on the Department of Defense to come up with a plan to secure their entire microelectronic supply chain, including commercial off-the-shelf technology.

Figure 2. Joint NASA-industry collaboration led to the first SMT boards.

We're all familiar with ITAR. We understand the rules that say that certain defense systems have to have American-made, trusted microelectronics. That's nothing new to anybody in our industry. But when it comes to commercial off-the-shelf technology, the supply chain becomes a bit opaquer. The trust becomes a little bit weaker. One of the things that we're calling on DoD to do by 2027 – that's the implementation date – is say we are going to look at our COTS supply chains and we're going to make sure that from certain adversarial locations, we are not in fact supplying critical defense systems. We've got to keep that provision sold. We've got to fight to make sure that's there every day through January 1st of 2027, when DoD has to actually implement it.

This is the reason we came into existence in 2021, and we've got to fight for it every year in the NDAA, but that's really the policy bill. That's the rules of the road. How do you run the DoD bill? The appropriations bill is the money, as you mentioned. We've got to go fight for at least $100 million in that bill as well. But Congress looks at everything that our men and women in uniform depend on and says, "We've got to be able to trust this stuff. We've got to be able to trust where the critical materials come from, where the microelectrodes come from, where is it made." And I think we exposed a potential flaw, a potential liability, and this is a good step to deal with it.

MB: Finally, advocates for passage of the Chips Act were successful, in part because of their outreach to mainstream media. Do you see a need to go outside the industry media as well?

DS: Oh, absolutely. You and others who cover the industry in detail have been tremendous advocates for us. You're shedding a lot of light on this issue, and I think even within microelectronics, critical materials suppliers, assemblers, manufacturers, there's a growing awareness that advocacy in Washington is critical to what we do. But yes, I'm openly envious of the way that the *Wall Street Journal* and the *New York Times* cover the semiconductor industry. Some

of it has to do with size, of course. These are some of the biggest companies in the world and they're working in the "high B" billions, they're breaking ground on massive facilities and promising thousands of jobs in key political districts, I don't know that our impact politically or economically mirrors what they're doing, but they will tell you because I've sat with these that what we are doing is critical to the overall stack and supply chain. And I think we've had some very positive interactions, positive coverage in outlets like the *New York Times,* for example. I've spoken to Bloomberg a number of times about these issues. At the national level with tier one press and media, it's a competition to have your issue covered and to make sure that you're the shiny object of the day, but we are part of a broad story and as much as anybody wants to talk about there's always that question: "What's the rest of the story?" Well, *we* are the rest of the story, and I think we're beginning to get traction there. But we are eager to get the word out in any venue that will give us the time.

MIKE BUETOW is president of the PCEA (pcea.net); mike@pcea.net.

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SCREEN **PRINTING**

When Cleaning Isn't Helping

"Bargain" materials can result in subpar outputs.

WE'VE COVERED UNDERSTENCIL cleaning topics in this column many times. Admittedly, if the stencil printing process were perfect, understencil cleaning wouldn't be required. But it is not an ideal world; we have board stretch, interspace challenges, and the compromise of printing speeds versus pressures to achieve balanced aperture filling.

Here is the basis for some of these challenges: If all the apertures were identical, the filling process (print speed/print pressure) could be optimized around one architecture. But, with the reality of different aperture shapes and sizes, the filling process must have a middle ground. The larger apertures fill more efficiently; thus, the filling process can deliver slightly too much fill on certain apertures, causing excessive material which may lead to solder paste bridging.

Conversely, the smaller apertures have a lower filling efficiency and, under the same speed and pressure setting, can be starved of solder paste, causing an insufficient fill. Insufficient deposited material can also result from an aperture with a low/tight associated area ratio. A low area ratio aperture has a lower transfer efficiency, which means that some of the material may remain in the aperture after filling. Eventually, this unreleased material can block the aperture, requiring understencil cleaning.

PCB to stencil misalignment is another challenge that cleaning helps mitigate. Even though printing machines have exceptional alignment capabilities down to 12µm, current PCB fabrication methods cannot equal this precision. Observing board stretch in the tens of microns across a standard PCB of 200 x 200mm is not uncommon. This mismatch between the stencil and PCB causes bridging due

to the apertures not being presented directly in line with the component pads. Indeed, there are a host of other root causes that we have addressed in previous columns – from tooling to incorrect solder paste types to poorly manufactured stencils. That is why we must clean and expect that understencil cleaning will help alleviate potential defects.

Cleaning doesn't always offer the remedy that's intended, unfortunately. Recently, a customer experiencing bridging and insufficients told us, "I'm cleaning, but it's not helping." While the root cause of those issues may be one described above, the fact that the cleaning "fix" wasn't providing any correction is what we'll address here. Even with bridging and/or insufficients, understencil cleaning helps stabilize the process. This customer was not getting any stability post clean.

So, what does one do if the cleaner isn't delivering the desired result? There are some general pre-flight checks I would advise. First, verify the cleaner is calibrated and touching the stencil. It seems obvious, but if the fabric roll isn't parallel with the underside of the stencil or making complete edge-to-edge contact, there won't be any cleaning going on! Though rare, it does happen. Second, check the solvent levels in the tank and the solvent chemistry. Some stencil printing platforms have sophisticated software that alerts users if solvent or fabric requires replenishment. If your platform isn't equipped with this feature, ensure you are checking supply regularly. The cleaning chemistry is also critical. While IPA is used in lab settings frequently for manual cleaning, it is not recommended for automated understencil cleaning systems because it is fast drying. It can take a bite out of the flux chemistry as all cleaners do, but then it flashes off quickly and leaves a sticky mess that gets smeared on the stencil's underside. IPA also has a high flash point, which is not safe. Special chemistries are fit for that purpose, so use whatever the machine supplier recommends for its understencil cleaning tool.

Back to our customer. Upon inspection of the understencil cleaner, fabric and solvent, our team noticed that the fabric lacked pores for absorbency. Without a porous structure, the fabric cannot accept the solvent to present it to the underside of the stencil. Ideally, the amount of solvent sprayed on the fabric roll is tightly controlled, the fabric becomes damp, and there is enough material to break down the flux vehicles. This was not happening, and because the fabric was not absorbent, the cleaning solution was rolling off. Once the culprit had been identified, a few minor changes to the understencil cleaning process inputs resulted in a thorough and effective clean. The solder paste bridging and insufficient material deposit challenges were alleviated. There is more work to do to

help correct the root cause of those issues, but for now, this customer's stencil printing process is in spec.

Some advice for what it's worth: While it is tempting to try to reduce costs by sourcing perceived "bargain" consumables, stencils, and other materials, subpar printing outputs may be the result. Remember that everything that goes into sophisticated stencil printing equipment is an engineered product and should be evaluated just as diligently as the printing platform. You've invested in advanced machine technology that requires high-quality inputs. Make wise investments in the process support products, too.

CLIVE ASHMORE is global applied process engineering manager at ASMPT (asmpt.com); clive.ashmore@asmpt.com. His column appears bimonthly.

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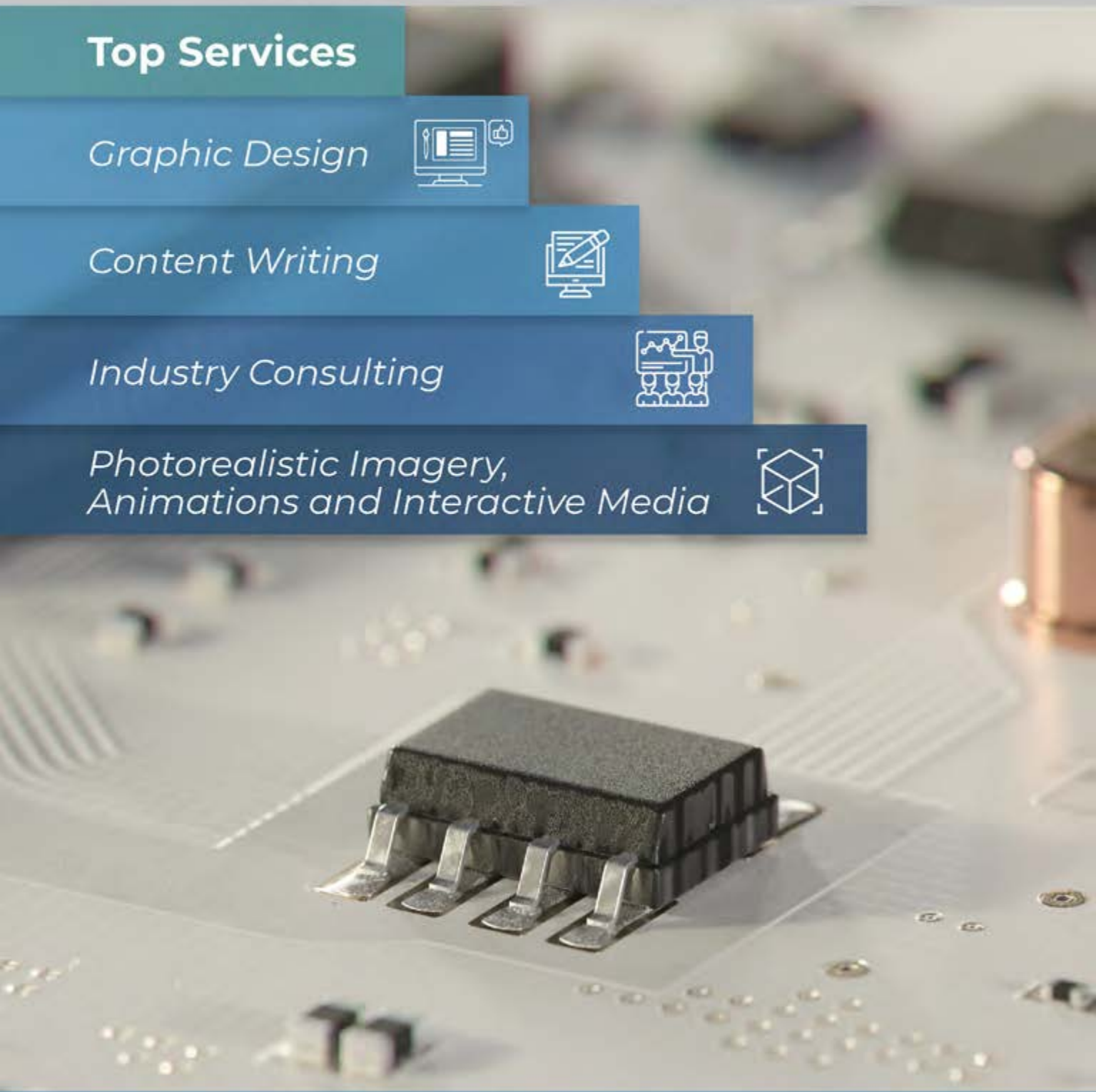

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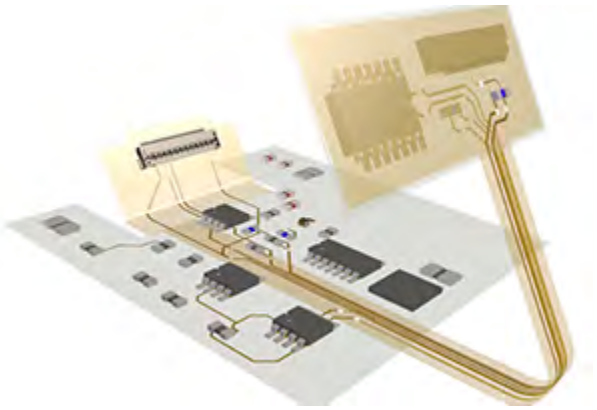

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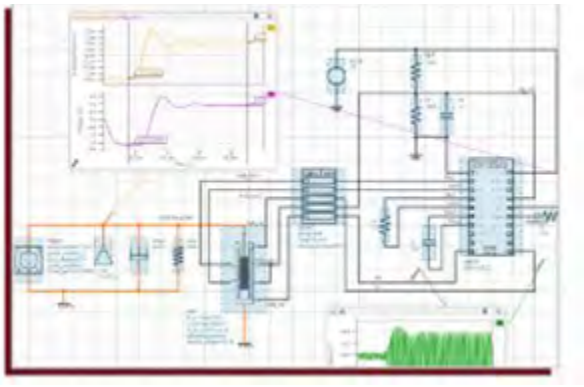

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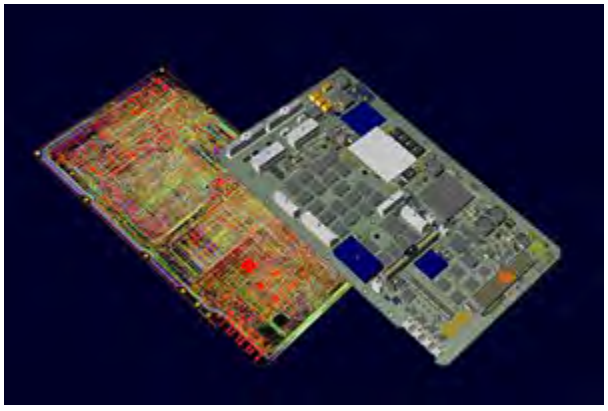

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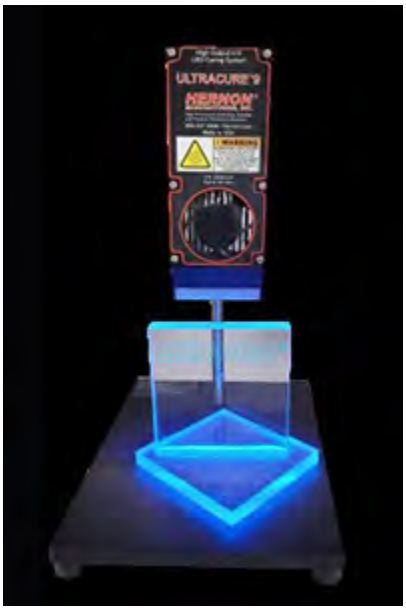

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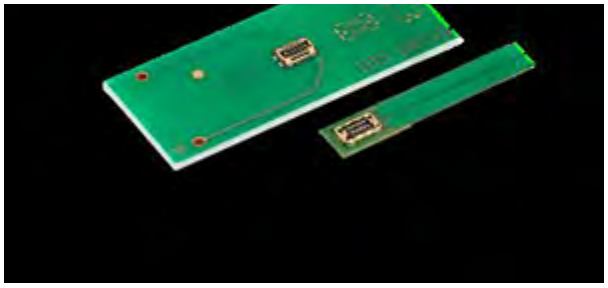

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"Measurement of Mixing Enthalpies for Sn-Bi-Sb Lead-Free Solder System"

Authors: Vikrant Singh, *et al.*

Abstract: Predictions of the thermodynamic behavior of higher-order multicomponent alloys from thermodynamic data of binary and ternary systems have been proven very crucial, as it is extremely challenging to investigate thermodynamic properties of higher-order systems. Therefore, it is necessary to assess thermodynamic data of various binary and ternary systems that are important to lead-free solder applications. The literature lacks thermodynamic information for some lead-free systems. Tin-bismuth-antimony (SnBiSb) is a good option as a solder ternary system free of lead. The integral and partial mixing enthalpies of a SnBiSb system were determined using a drop-solution calorimeter. At 923K, 973K, and 1023K, calorimetric measurements of the Sn-Bi-Sb system were made along five of the cross-sections. Pieces of pure tin were dropped into molten Sb0.25Bi0.75, Sb0.50Bi0.50, Sb0.75Bi0.25 alloys, bismuth into Sb0.50Sn0.50, and antimony into Bi0.50Sn0.50. Using the calorimetric data, partial and integral thermodynamic properties were determined. The integral mixing enthalpy was used to plot iso-enthalpy curves. It was found that the mixing enthalpies were temperature independent. The substitutional solution Redlich-Kister-Muggianu model was used to derive the interaction parameter based on ternary enthalpy values and, to obtain these parameters, a least square fitting model was used. When the estimated and measured values were compared, it was found that there was good agreement among them. (*Journal of Electronic Materials,* July 2023, https://doi.org/10.1007/s11664-023-10579-4)

Solder Joint Reliability

"Mechanical Characterization of SAC305 and SnPb36Ag2 BGA Assemblies Under Static Flexural Loading"

Authors: Jean Baptiste Libot, Olivier Dalverny, Joël Alexis and Jeremy Bosq

Abstract: Static bending-induced solder joints damage is a main reliability concern for aerospace and military industries whose printed circuit board assemblies (PCBAs) are required to remain functional under flexural loading. To dissipate heat in an equipment, it is common to install thermal gap pads on electronic packages. When compressing thermal gap pads during the fixture process, the PCBA can bend and solder joints can therefore crack if the deflection is too significant. This paper reports the durability of 96.5Sn-3.0Ag-0.5Cu (SAC 305) and 62Sn-36Pb-2Ag (SnPb36Ag2) ball grid array (BGA) assemblies under static flexural loading at -55°, 20° and 125°C. As electronics equipment can be stored at high-temperature for prolonged durations, some SAC 305 test vehicles were also aged at 125°C for 192 hr. For each test configuration, the bending tests were conducted at a ramp-rate of 2mm/min and the central displacement-to-failure was measured. Finite element modeling (FEM) analysis was conducted considering a global-local approach and the transfer function between the central displacement-to-failure and the local PCB strain near the critical solder joints were determined for each test configuration. The results give the necessary data for designers to assess whether a specific PCBA design subjected to static bending is at risk. (*Journal of Surface Mount Technology,* vol. 36, no. 1, 2023, https://doi.org/10.37665/smt.v36i1.34)

Sustainability

"Recyclable Paper-Based Electronics"

Authors: Gerhard Domann, *et al.*

Abstract: Millions of tons of electronic waste are produced in the EU every year. With a novel approach, the new EU project "CircEl-Paper" could sustainably improve the recycling process for electronics in the future. Globally, 53 million tons were produced, only about 17% of waste was verifiably collected and properly disposed of, according to the Global E-Waste Monitor 2020 – a

large amount of valuable materials produced at great expense is thus regularly lost. The CircEl-Paper project team will demonstrate the diverse areas in which paper-based PCB technology can be applied with three use cases from the fields of medicine, logistics and consumer electronics: A medical sensor for measuring glucose levels on the skin, packaging with an integrated time-temperature indicator (TTI) or greeting cards that play music exemplify the technology's performance and adaptability. (Project CircEl-Paper, https://circelpaper.eu)

"Sustainability Considerations for Organic Electronic Products"

Authors: Iain McCulloch, *et al.*

Abstract: The development of organic electronic applications has reached a critical point. While markets, including the Internet of Things, transparent solar and flexible displays, gain momentum, organic light-emitting diode displays lead the way, with a current market size of over $25 billion, helping to create the infrastructure and ecosystem for other applications to follow. It is imperative to design built-in sustainability into the materials selection, processing and device architectures of all these emerging applications, and to close the loop for a circular approach. In this perspective, the authors evaluate the status of embedded carbon in organic electronics, as well as options for more sustainable materials and manufacturing, including engineered recycling solutions that can be applied within the product architecture and at the end of life. This emerging industry has a responsibility to ensure a "cradle-to-cradle" approach. The authors highlight that ease of dismantling and recycling needs to closely relate to the product lifetime, and that regeneration should be facilitated in product design. Materials choices should consider the environmental effects of synthesis, processing and end-product recycling as well as performance. (*Nature Materials,* June 2023, https://doi.org/10.1038/s41563-023-01579-0)