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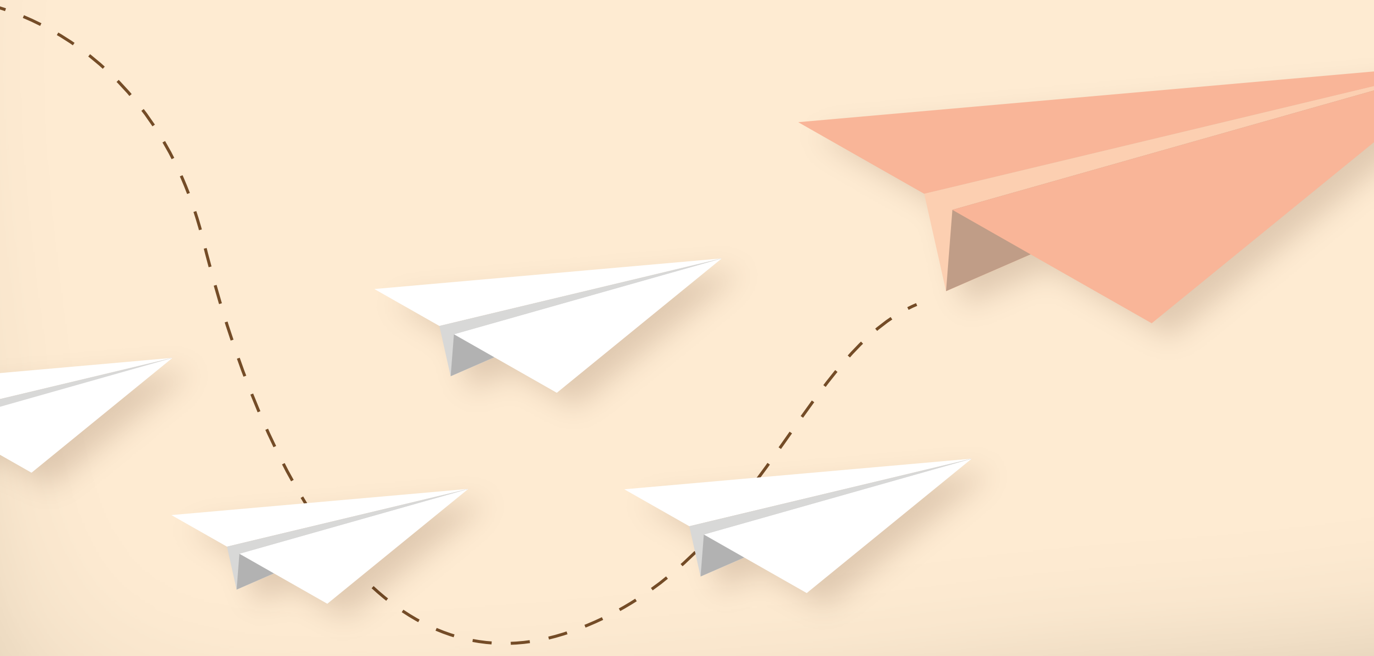
November 2023

CIRCUITS ASSEMBLY

DATA INDEPENDENCE

Critical SPC Assumptions



Design **REUSE**

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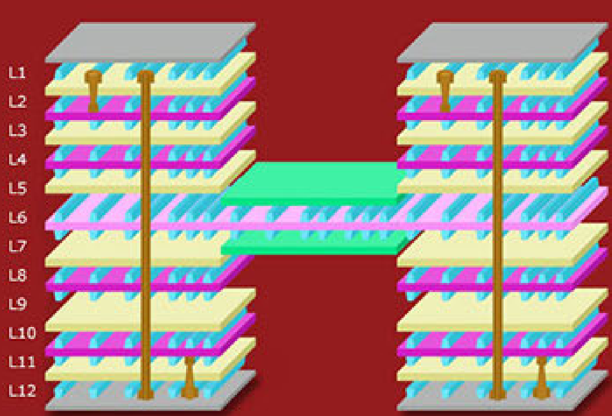

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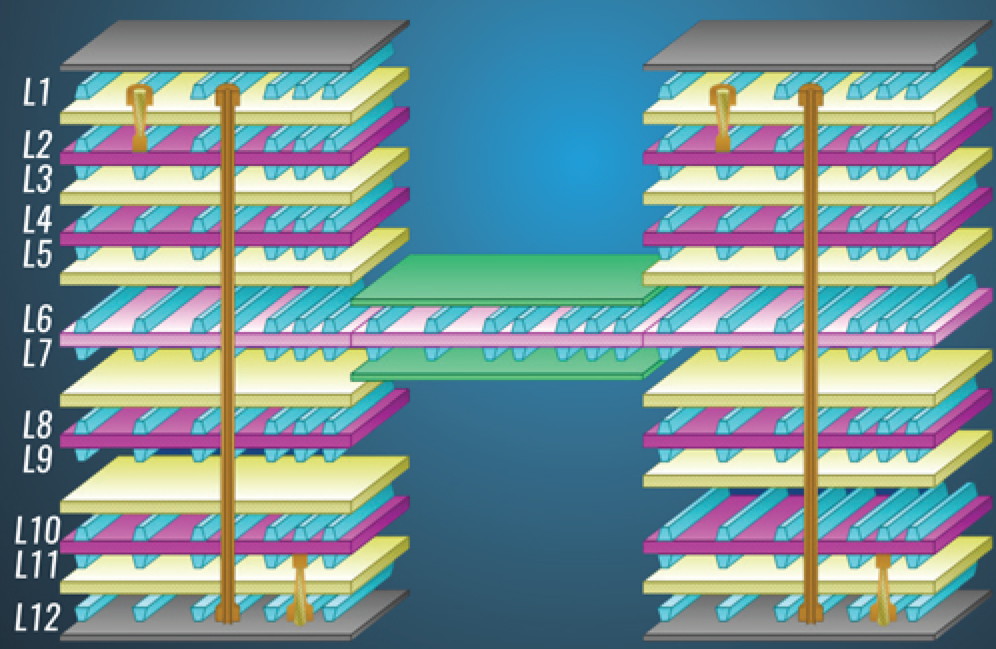

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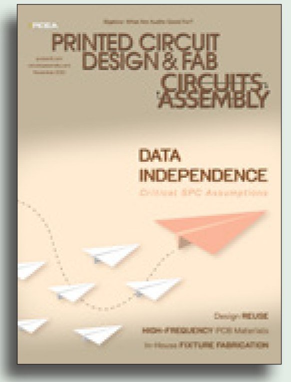

FEATURES

PROCESS CONTROL (COVER STORY)
Assessing Data Independence and Normality for SPC Charts
Many printed circuit board chemical manufacturing processes can violate the assumption of data independence, which along with normality is crucial for accurate statistical process control charts. Being able to confirm data's independence and normality before plotting them on an SPC chart can save valuable time for a process engineer.
by PATRICK VALENTINE, PH.D.

HIGH-FREQUENCY PCB MATERIALS
Basics of High-Frequency PCB Materials
As more electronic devices function at high frequencies, selecting materials suitable for high-frequency work is becoming crucial for new product development. An overview of the important characteristics of high-frequency PCB materials.
by SAGI BALTER, PH.D. and VITALY BENSMAN

HARDWARE DESIGN
5G Open Radio Unit White Box
5G radio networks provide increased bandwidth at the expense of reduced range, so the availability of cost-effective radio units is critical. An overview of the design and development process for the various hardware components that make up Whizz System's 5G Open Radio Unit.
by MUHAMMAD IRFAN

ON PCB CHAT (PCBCHAT.COM)

NETWORK RELIABILITY
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with DR. ALEXIS ABRAMSON

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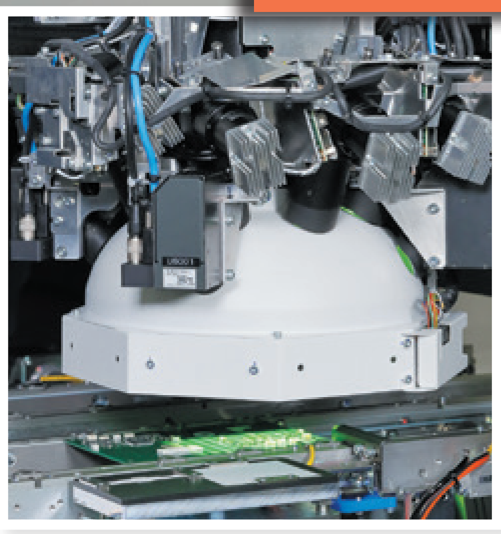

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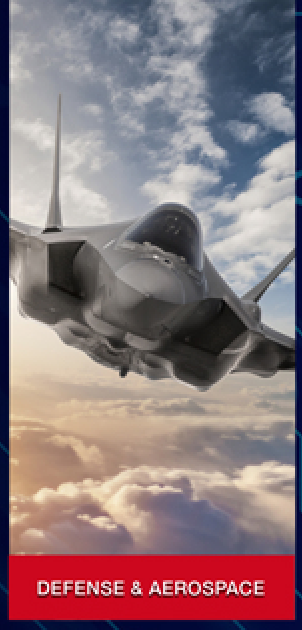

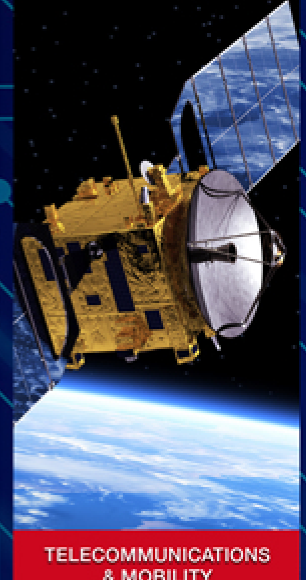

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Why is China Provoking Foxconn?

AS ANYONE WHO has visited Acapulco knows, it is picturesque, with the serene mountain scape overlooking the half-moon bay.

Pictures, as we also know, can be deceiving.

For the better part of the decade, the once-classic vacation spot has been overrun with drug gangs, and the former wave of tourists has diminished to a trickle. And that was before Hurricane Otis hit last month.

As 2023 draws near its end, we are reminded of how much uncertainty lies ahead. Whether man-made, like the regional conflicts in Europe, the Middle East, Africa and the Pacific Rim; or natural disasters, such as those experienced in Mexico, Turkey and the US, we seem awash in challenges and obstacles.

And then there are the completely self-inflicted wounds.

While we've been critics of Foxconn for some time, the recent "inspection" of some of its Chinese offices by domestic tax authorities almost certainly has less to do with corporate malfeasance than it does with Beijing's attempt to influence the outcome of the upcoming Taiwanese presidential election.

A disclaimer: We can't possibly know if Foxconn's finances are on the up and up, and China has both the right and, we would argue, the responsibility to ensure companies operating in its territory are doing so in accordance with local laws. But the timing seems, well, more than coincidental.

Here's why. Terry Gou, Foxconn's founder and former chief executive, has twice made bids for the Taiwanese presidency. The Kuomintang party (KMT) he belongs to is known for wanting closer ties to the mainland. And while he has failed both times to gain sufficient traction among KMT voters, this time he is circumventing the nomination process by declaring an independent bid.

The rub, for Chinese leaders, is that such a move could split votes for the eventual KMT candidate, Hou Yu-ih, the mayor of New Taipei, thus paving the way for the Democratic Progressive Party (DPP) to retain control. And DDP's candidate is seen as more pro-independence than his competitors for the office.

Through this lens, China's raid on Foxconn is seen more as a power play against Gou, who remains Foxconn's largest shareholder, with a net worth of more than $6 billion, to pressure him to withdraw from the race.

It's an audacious move. Foxconn is China's largest private employer, and Gou historically has advocated for closer relations with Beijing. He seems to be gambling that China won't take the chance that Foxconn relocates some of its plants – and the 1.2 million workers it employs – from the mainland. At the same time, however, Foxconn has been hedging its bets, building up its presence in India as an alternative to China (and for real, this time, unlike the vaporware in US states like Wisconsin, Ohio and Pennsylvania, plus Brazil, Indonesia, Vietnam and others).

Like we said, wounds can be self-inflicted. China typically operates with a long-term strategy in mind. Preventing chaos is its hallmark. To jeopardize relations with its most important employer, and one of the most significant companies in the world, is nothing short of rash. Electronics manufacturers, take note: When locating facilities, what weight are you attaching to national stability? If China will threaten Foxconn, is any company there safe from (possibly) unwarranted governmental scrutiny?

PCEA news. Membership is a core benefit of PCEA. Membership offers networking and access to technical content, in written and webinar form. While many of our local chapters could use a hand with meeting logistics, we are planning a series of webinars starting next month to help fill the gap.

We are planning at least a half-dozen webinars in the coming months, with topics ranging from additive manufacturing to printed circuit material characterization, insulated metal substrates

(IMS), component selection, and AI in electronics, to name a few. All webinars are free for PCEA members, and individual membership is also free, so there's no reason to wait to join. Please check the PCEA website for details.

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P.S. See us this month at Productronica (stand B3106) and PCB Carolina!

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Icape Group Makes 3 US Acquisitions

FONTENAY-AUX-ROSES, FRANCE – Icape Group has announced the acquisition of three US companies: PCB Solutions, Ustek Inc. and Nujay Technologies.

The three companies have each specialized in PCB distribution in the US for over 20 years. PCB Solutions and Ustek also distribute technical parts, representing 10% and 30%, respectively, of their businesses. In total, the three companies have a portfolio of more than 180 North American customers from a variety of industries, ranging from medical equipment design to the automotive sector. In 2022, these three companies generated a cumulative net revenue of over $5 million and an EBITDA margin of over 10%.

In making the acquisitions, Icape strengthens its foothold in the US by gathering a strong pool of industrial customers, as well as new distribution channels, and the different locations of the new acquisitions (in Ohio, California and Utah) also enable the group to cover the entire US territory, the company said in a release.

"Since the launch of our external growth strategy in 2021, all acquisitions made by Icape Group have been focused on the European continent. By acquiring the assets of PCB Solutions, Nujay Technologies and Ustek, we are proud to significantly strengthen the international footprint of our solutions dedicated to printed circuit boards and technical parts, as well as the value creation potential of our North American subsidiaries," said Yann Duigou, CEO, Icape Group. "The assets we integrate today brought us a substantial portfolio of over 180 North American customers from a wide variety of industries, as well as their dedicated distribution channels, both in the United States and in Asia. By joining Icape Group, these assets will be able to benefit from numerous synergies as well as from the expertise of our subsidiaries to deliver the highest possible quality of service to their local customers, which should ensure us significant post-integration profitable growth in the

short- to medium-term."

DoD Awards $17M to Microelectronics Industrial Initiatives

WASHINGTON – The Department of Defense's Office of Industrial Base Policy has awarded a combined $17.5 million in contracts to support two initiatives that will strengthen the resilience of the defense microelectronics industrial base – including a project to promote production of ultra-high-density interconnects for PCBs.

The DoD, through its Manufacturing Capability Expansion and Investment Prioritization (MCEIP) office, awarded $11.5 million in the Defense Business Accelerator (DBX) and Printed Circuit Board Market Catalyst project, which will harness private capital and commercial market forces to scale defense-relevant technologies and rapidly expand the industrial base.

The PCB Market Catalyst project will deliver a detailed plan for the creation of a new company that will stimulate demand for domestic production of ultra-high-density interconnects for PCBs. The plan will then be presented to the DoD for a decision on whether to fund the creation of the new company. The PCB Market Catalyst will enable the US to surmount an impasse that has left it behind in the global PCB market. DBX leverages commercial market forces to accelerate the transition of emerging defense technologies into sustainable businesses to fill supply chain gaps. Both DBX and PCB Market Catalyst are being executed by the US Partnership for Assured Electronics in partnership with Advanced Technology International, with initial funding from MCEIP of $11.5 million over three years.

The Enterprise Parts Management System (EPMS) is a cloud-based enterprise-wide microelectronics parts management tool intended to enable parts management at program office levels across DoD throughout the entire parts lifecycle. EPMS will give DoD the ability to aggregate information on parts used in DoD systems and manage those parts at the enterprise level. This enhances insight into critical risks and enables rapid access to remediation measures that are vital to ensuring warfighter safety and mission success.

The $6 million investment will support the iterative design and development of the cloud-based platform. This tool will support Military Service and defense agency weapon system program

offices; prime system developers and maintainers; and acquisition, sustainment, research, development, testing, and evaluation offices across the Department. JRC Integrated Systems, LLC of Washington, D.C. and Systems Innovation Engineering of Mullica Hill, New Jersey will execute the EMPS project.

“EPMS will provide an important ‘whole-of-DoD’ view of the microelectronics parts supply chain and enable better life-cycle management of this critical technology for DoD weapon systems,” said MCEIP Director Anthony Di Stasio.

The two teams will assess DoD, Military Service, defense agency, and commercial capabilities to identify the best make-buy solution and then down-select to the best value in the iterative design and build of this innovative new system.

“These two awards directly support the Biden-Harris Administration’s initiatives to strengthen America’s supply chains as outlined in Executive Order 14017,” said Assistant Secretary of Defense for Industrial Base Policy, Dr. Laura Taylor-Kale. “They will foster collaborative procurements, provide more visibility into global diminishing manufacturing sources and material shortages solutions, and facilitate the rapid dissemination of risk information such as obsolescence, evidence of counterfeit parts, and software vulnerabilities.”

CEA and Siemens Collaborate to Expand Applications of Digital Twin

PLANO, TX – Siemens Digital Industries Software and CEA-List, a technological research institute focused on smart digital systems research, have signed a memorandum of understanding to collaborate on research to further extend and enhance digital twin capabilities with artificial intelligence and explore greater integration of embedded software on both virtual and hybrid platforms.

The research collaboration will bring together the two organizations’ combined industry expertise with the Siemens Xcelerator portfolio and CEA-List’s toolset to help break down the barriers between electronics design, software development and mechanical engineering disciplines using digital twin technologies. This is expected to help customers to significantly reduce the time and cost of verification and validation and to drive significant improvements in product quality and

accelerate time to market across the full electronics systems product lifecycle; from architectural exploration to design and development. Alongside this, the research will further explore the use of digital twin technologies for autonomous driving, smart robotics and health domains.

"With the strong increase in electronics and software content of products and systems, there is a clear need for multi-domain, multi-fidelity system simulation solutions to relieve multiple design and verification challenges. We share a vision with CEA of an even more comprehensive Digital Twin and believe we can implement this vision through the power of the Siemens Xcelerator portfolio because it covers everything from Electronic Design Automation software and hardware tools to system, sensors and multi-physics simulation software," said Jean-Marie Brunet, VP and GM, hardware assisted verification division, Siemens Digital Industries Software. "From chip-to-system, this collaboration with CEA-List is expected to further expand the application domains and technology breadth of these solutions."

"At CEA-List, we are delighted to partner with Siemens, who share our common vision about the importance of a more holistic Digital Twin. CEA-List will contribute its expertise in digital technologies and tools from immersive and functional digital twin platforms (XDE and Papyrus), artificial intelligence and code verification areas," said Alexandre Bounouh, CEO of CEA-List. "We believe that the Siemens and CEA-List Digital Twin research roadmap can offer best in class tools for generating rapid immersive and functional digital twins enhanced with artificial intelligence. This can certainly boost the competitiveness of companies by integrating Digital Twin technology early to innovate in their products and processes while keeping humans in the loop and reducing their environment impact."

SnapEDA Rebrands as SnapMagic, Adds AI PCB Design Features

SAN FRANCISCO – SnapEDA, a provider of footprints and models for electronic components, has announced a rebranding as SnapMagic and the release of a new AI-based tool for circuit board design.

The new tool, SnapMagic Copilot, combines artificial intelligence with the firm's proprietary dataset. The combination, SnapMagic said, streamlines certain repetitive aspects of electronics design.

For instance, the new tool auto-completes circuits and suggests related parts to fill out a design. Users can issue instructions in plain English – for example, requesting "non-inverting amplifier with a gain of 2" – and SnapMagic Copilot will use "solid" circuit theory fundamentals to design the circuits using available parts. It can also propose a manufacturer-endorsed reference design.

For bills-of-materials, the tool will suggest pin compatible replacements at different price points, and can recommend alternatives when inventories are low.

"SnapMagic Copilot is a natural extension of our mission: to help engineers design electronics faster by removing barriers," the company said on its website. "It is possible because of the massive proprietary dataset (millions of schematic symbols, footprints, designs), that we have been creating in collaboration with component suppliers since our inception."

SnapMagic Copilot is intended to augment PCB tools, the founders said, and support the 20+ formats supported today on SnapEDA (now called SnapMagic Search). "This means that engineers can add AI to their PCB tools instantly, without switching tools."

SnapMagic also announced a new round of funding from AI and developer tool investors. It did not disclose the amount or the investors.

Krypton Solutions to Invest $100M in Karnataka Facility

BOMMASANDRA, INDIA – Krypton Solutions is planning to invest $100 million to establish a PCB fabrication facility in the Indian state of Karnataka, the company confirmed to PCD&F/CIRCUITS ASSEMBLY in October.

"We are planning a PCB plant in India in 2024," Dipak Patel, owner, Krypton Solutions, told PCD&F/CIRCUITS ASSEMBLY.

The decision to invest was announced during a meeting between the company's representatives and an official delegation led by MB Patil, Karnataka's Minister of Large & Medium Industries.

Krypton Solutions intends to set up its new plant in Bommasandra, Bengaluru and has already engaged in preliminary discussions with the government.

"During the meeting, the company also explored potential investment opportunities in Mysuru and Chamarajanagar within the state. Furthermore, Krypton expressed interest in forming local partnerships and sought support in identifying suitable entry and growth partners in the Indian market," Patil said in a statement.

Krypton also has EMS facilities in Plano, TX; San Jose; and India.

IPC Updates Board Qualification Spec

BANNOCKBURN, IL – IPC has released IPC-6012F, *Qualification and Performance Specification for Rigid Printed Boards,* the base standard for bare circuit boards.

IPC-6012 provides requirements for the qualification and performance of rigid printed boards based on constructions and /or technologies such as; single-sided, double-sided printed boards with and without plated-through holes (PTH), multilayer printed boards with PTHs with or without buried/blind vias/microvias, active/passive embedded circuitry printed boards with distributive capacitive planes and/or capacitive or resistive components and metal core printed boards with or without an external metal heat frame, which may be active or non-active.

Among the many additions to IPC-6012F, are expanded requirements in the following areas: printed board cavities, copper wrap plating, "Intermediate" target lands, solderability testing, dewetting, microsection evaluation, internal plated layers, dielectric spacing and reliability issues with microvia structures.

"The hard work put in by the IPC D-33a Rigid Printed Board Performance Specifications Task Group over the past three years has resulted in a substantial revision to IPC-6012," said John Perry, IPC's director of printed board standards and technologies. "IPC-6012F incorporates test coupon designs well suited to evaluate complex, interconnected via structures as part of an overall effort to address microvia reliability. Add to that new criteria for printed board cavities, hole registration, internal plated layers and dielectric spacings and you have a performance specification that addresses advances in rigid printed board fabrication processes."

Calumet Electronics to Build Substrate Manufacturing Facility in MI

CALUMET, MI – Calumet Electronics is on track to building a substrate factory in the US with a 60,000 sq. ft. facility on its campus in Michigan's Upper Peninsula.

The project is expected to generate a total capital investment of up to $51 million. That amount includes a $7.5 million incentive from the Michigan Economic Development Corporation and a 15-year tax break of up to $758,877 per year.

Over the next three years, while the company scales its substrate production with training and technology, 270 of its current 350 employees will be retained to maintain the standard current production needs. Forty existing employees will receive initial upskilling critical to manufacturing advanced package substrates and complex PCB technologies in support of the semiconductor ecosystem and defense complex.

"We extend our gratitude to Governor Whitmer, MEDC CEO Quentin L. Messer, his dedicated team for their tireless effort and unwavering support, and the Michigan Strategic Fund," said Calumet Electronics President Stephen Vairo. "Additionally, we thank InvestUP, Warner, Norcross & Judd and Marketing Department for helping bring this project over the finish line. The funding will allow Calumet Electronics to advance our technology with a primary focus on bringing semiconductor and microelectronics manufacturing back to the United States. We are thrilled about the prospect of expanding our operations and facilities right here in Calumet, MI, creating increased opportunities for career retention, upskilling, and job growth in the Copper Country."

Calumet is pursuing federal funding to address the needs of the Defense Industrial Base and support the strategic semiconductor and defense goals of the State of Michigan. In response to concerns raised by US defense and commercial OEMs regarding the availability of package substrates produced within the US, Calumet Electronics may become the primary supplier, potentially even an exclusive supplier to US strategic programs, the company said.

Amphenol to Acquire PCTEL for $140M

WALLINGFORD, CT – Amphenol has announced an agreement to purchase wireless equipment maker PCTEL for $139.7 million. The transaction is expected to be finalized in the fourth quarter or in early 2024, subject to customary closing conditions and approval by PCTEL stockholders.

Amphenol said the acquisition of PCTEL, which specializes in purpose-built Industrial IoT devices,

antenna systems, and test and measurement products, will enable the company to further expand its portfolio and strengthen its position in the market.

"Our team has done an excellent job of growing the business, establishing a leadership position in both antenna and test & measurement (T&M) innovation, and meeting our customers' strong global demand for high reliability applications," said PCTEL CEO David Neumann. "Amphenol is a leading global provider of interconnect, sensor, and antenna solutions. Their sustained financial strength and unique entrepreneurial culture will create a valuable home for our employees around the world. We look forward to the accelerated growth opportunities enabled by the combination of our two companies."

Following the closure, PCTEL will no longer be listed on any public market.

Foxconn Subjected to Tax Inspections by Chinese Authorities

TAIPEI – Foxconn's Chinese facilities were recently subjected to searches by Chinese tax authorities, and speculation is rampant that the investigation was spurred by Foxconn's largest shareholder's bid for the Taiwanese presidency.

The company had its offices in Guangdong and Jiangsu provinces searched by tax officials, according to a report in China's *Global Times* newspaper.

The Ministry of Natural Resources also inspected Foxconn offices in Henan and Hubei provinces, where the company has major factories. Foxconn employs hundreds of thousands of workers across China.

Observers suggested that the tax investigation is a smokescreen to put pressure on Terry Gou, Foxconn's founder and principal owner. Gou is running for president of the island nation, and his independent bid could split the vote for the Kuomintang party, which is said to be preferred by the Chinese leadership because of its mainland leanings.

New Roadmap Identifies Critical

Semiconductor Research Priorities

WASHINGTON – The Semiconductor Research Corporation has unveiled the Microelectronics and Advanced Packaging (MAPT) Roadmap, which defines critical chip research priorities and technology challenges that must be addressed to support the "seismic shifts" outlined in the Decadal Plan for Semiconductors released by SRC and SIA in January 2021.

The Decadal Plan identified five seismic shifts in the industry related to smart sensing, memory and storage, communication, security, and energy efficient computing. The MAPT Roadmap continues the spirit of the Decadal Plan and discusses how to achieve its system-level goals, outlining the implementation plan for the semiconductor industry.

The fundamental research that will transform these obstacles is focused on advanced packaging, 3-D integration, electronic design automation, nanoscale manufacturing, new materials, and energy-efficient computing. The MAPT Roadmap is framed around fundamental and practical limits of information and communications technology sustainability: energy sustainability, environmental sustainability, and workforce sustainability.

Federal government and private sector investments in semiconductor R&D have propelled the rapid pace of innovation in the US semiconductor industry, spurring tremendous growth throughout the U.S. and global economies. The MAPT Roadmap is intended to serve as a guide to sustain and expand public and private investments in chip research to help unlock the transformative technologies of the future.

Indium Acquires Low-Heat Solder Developer

CLINTON, NY – After partnering with the company last year to develop a supercooled liquid metal solder paste, Indium Corp. in October announced the acquisition of Safi-Tech. Financial terms were not disclosed.

Last year, Indium collaborated with Safi-Tech to launch a supercooled BiSn solder paste using the latter's solder platform. That platform permits molten metal to remain liquid far below its freezing

point by encapsulating it in a smooth shell – known as supercooling. The shell of these microcapsules can be removed using a traditional flux and reflow process, or by mechanically crushing a powder of supercooled liquid metal microcapsules. Using this platform, industry-standard alloys such as SAC 305 can be soldered at below typical low-temperature solder (LTS) specifications, while other alloys can be soldered at temperatures as low as ambient.

"Safi-Tech's supercooling platform is an exciting addition to our award-winning product portfolio, allowing us to deliver next-generation soldering materials," said Ross Berntson, president and COO, Indium. "This innovation has far-reaching potential and embedding Safi-Tech into Indium gives it the opportunity to succeed widely and quickly."

In addition to acquiring the Iowa-based company, Indium will also benefit from Safi-Tech's cofounder, coinventor and president Dr. Ian Tevis joining the company as an R&D manager. In this role, Tevis will oversee a team dedicated to application technology and manage the ongoing research and design of Safi-Tech supercooled products.

"As a key partner to Safi-Tech over the past five years, we have witnessed Indium's position as an industry leader first-hand," said Tevis. "We are confident that the company's state-of-the-art facilities, network of customers and equipment suppliers, and talented team members will accelerate our work in bringing supercooled solder to a worldwide audience."

Originating from Iowa State University with the discovery of no-heat and low-heat solder and metallic joining products, Safi-Tech was founded in 2016 by Tevis and Dr. Martin Thuo. It was backed by Rhapsody Venture Partners.

"We have been tremendously impressed by Indium's vision for Safi-Tech and the capabilities they possess," said Carsten Boers, managing partner at Rhapsody Venture Partners and lead investor in Safi-Tech. "This transaction was the natural next step in our great collaboration and we look forward to seeing the success which comes from it."

Ed.: Listen to the PCD&F/CIRCUITS ASSEMBLY podcast on low-heat solders with Indium and Safi-Tech here.

AIM Solder Purchases William Rowland's Solder Business

LUTON, UK – AIM Solder UK has announced the acquisition of William Rowland Ltd.'s solder products business, encompassing solders and alloys. Financial terms were not disclosed.

This acquisition will expand AIM Solder's capabilities and enhance customer offerings in the metal industry, the company said in a release.

"This strategic move allows AIM Solder to further enhance its position in the solder industry by leveraging William Rowland's legacy and expertise in this specific sector," said Ricky Black, president, AIM Solder. "We are excited to welcome William Rowland's solder customers into the AIM Solder family, and we are committed to preserving the values that have made them a trusted name in this field."

ECIA Publishes Update on Anti-Counterfeiting Standard

ATLANTA – ECIA's Global Industry Practices Committee (GIPC) has published an ECIA Update document based on the five-year review process conducted by SAE's AS6496 Standard Committee. There have been changes to the standard, which is out for the final vote. The updated version, AS6496A, is expected to be available by the end of the year.

The Society of Aerospace Engineers' (SAE's) AS6496 is an anti-counterfeiting measure outlining requirements for mitigating counterfeit products in the authorized supply chain by distributors performing authorized distribution. SAE adopted this standard on Aug. 20, 2014, with the official title of "Fraudulent/Counterfeit Electronic Parts: Avoidance, Detection, Mitigation and Disposition – Authorized/Franchised Distribution."

The standard is used by authorized distributors to reduce the risk of counterfeit components entering the aerospace supply chain, but it is a reliable anti-counterfeiting model for any customer.

The ECIA Update includes a background on the standard, a detailed explanation of what has changed in the updated version, and how customers in any industry can mitigate the risk of counterfeit components entering their manufacturing processes.

"A number of ECIA distributor members have been working on this standard since its inception,"

remarked Kevin Sink, VP of total quality, TTI. "Anti-counterfeiting measures are deeply embedded in the way authorized distributors do business. The best way to avoid counterfeit components is to buy components from authorized distributors."

Read the ECIA Update here.

Zollner Opens Chinese Plant Expansion

TAICANG, CHINA – Zollner Elektronik has expanded its plant here to meet the growing demands of the international market.

With around 17,000 sq. m. of building space, the new plant building includes a cleanroom, two stories of production space for PCB and device assembly, a large warehouse area, a large cafeteria, and social areas as well as office space. The additional production space takes up 15,000 sq. m. and was conceived specifically to increase the company's production efficiency and capacity and create more jobs, Zollner said in a release.

The company said the expansion also underscores its long-term vision and commitment to the Taicang region and is a significant milestone in the history of the company.

"We are confident that Taicang offers excellent opportunities and conditions, particularly for the production of complex products, which will unlock further possibilities and potential for our company," said board member Markus Aschenbrenner.

Cicor to Acquire STS Defence

BRONSCHHOFEN, SWITZERLAND – Cicor will acquire STS Defence, a UK-based provider of sustainment, support and modernization solutions for the aerospace and defense markets.

STS Defence has earned an outstanding decades-long reputation for solving complex technical challenges by delivering innovative solutions and programs, and employs around 150 people, Cicor said in a release announcing the acquisition.

The company said the combination of the strengths of Axis Electronics, which was acquired in

2021, and STS Defence, will ideally position Cicor to implement the most demanding customer programs with a focus on the UK market. STS Defence generated sales of GBP27.5 million ($33.5 million) in the fiscal year ended on June 30.

Cicor said it will continue to provide engineering support and manufacturing services from the existing STS Defence site under the current management team, and closing of the transaction is expected within 2023 and is subject to regulatory approvals and other customary closing conditions.

PCD&F

Eltek announced a $2.9 million purchase order from an existing customer.

Foxconn will reportedly set up a PCB fabrication plant in India.

Jingwang Electronic broke ground on a high-rise multilayer PCB production facility in Xinfeng County Shenzhen Industrial Park.

Korea Circuit won a large order from **STMicroelectronics** to supply it with FC-BGA substrates.

PS Electronics has ramped up its investments in LCP PCB manufacturing technologies and equipment.

Trilogy will represent **Schweizer Electronic** in North America.

TSMC reportedly grabbed orders for **Nvidia's** next-generation AI processor called B100, which requires the foundry's 3nm process fabrication.

Walton Digi-Tech Industries, the sole PCB manufacturer in Bangladesh, has started exporting boards to Greece.

Zhiboxin Group broke ground on a 5 billion yuan ($685 million) PCB production base in the Jinxian Industrial Park in Nanchang, China.

Zhichao has invested tens of millions of dollars in a new factory in North Vietnam.

CA

ANYbotics is collaborating with **Zollner Elektronik** for serial production of its ANYmal robot.

Asus is setting up a factory in Chennai, India, through its contract manufacturer **Flex.**

CDIL has commenced production of silicon carbide devices through surface mount technology at its manufacturing facility in Mohali.

CoolCAD announced a strategic partnership with rep agency **NWN.**

Creation Technologies will supply circuit card assemblies, cables and connectors to **L3Harris Technologies** for a multitude of mission critical defense programs.

Dixon Technologies subsidiary **Padget Electronics** has entered into an agreement with **Xiaomi** to manufacture smartphones and other related products.

Escatec Switzerland purchased a **Mycronic** MY700 jet printer.

Jabil will produce optical network terminals and optical line terminals for **Calix** at its manufacturing facility in Auburn Hills, MI.

Jabil expects $300 million in pretax restructuring and related costs throughout 2024 related to the sale of its Chinese electronic components manufacturing business to **BYD Electronic,** according to a statement filed with the US Securities and Exchange Commission.

Kitron will produce **BRC Solar's** Power Optimizer.

Kyocera AVX is acquiring the assets of **Bliley Technologies,** a developer of low-noise

frequency control products.

Kyocera International purchased a **Hentec Industries/RPS Automation** Odyssey 1325 robotic hot solder dip component lead tinning machine.

Nortech Systems' Suzhou, China, facility has been certified by the National Medical Products Administration to produce Class II Medical Devices for customers in Asia.

Offshore Electronics is set to add a large solar PV array to its 20,000 sq. ft manufacturing headquarters in St. Peter Port, Guernsey.

Selecs will represent **ITW EAE** in Germany, Austria and Switzerland.

Shenzhen Grandsun is keen on expanding its presence in the Philippines, with plans to add two more facilities by 2025, according to the country's Board of Investments.

Q Source signed a distribution agreement with **XDry.**

Yamaha Robotics SMT Section supplied three Sigma G5SII surface mounters and the latest YRi-V 3D optical inspection system to **Vimar's** new plant in Marostica, Italy.

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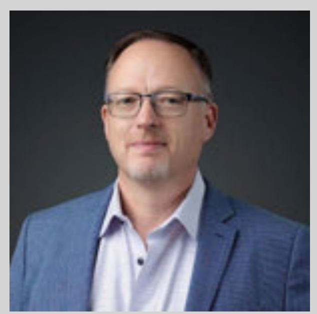


Peter Austin

Karl Sauter

Michael Garrett

Greg Zweigle

Dan Boehle

APCT appointed **Peter Austin** president and CEO.

HDP User Group named **Karl Sauter** project facilitator.

MacDermid Enthone Industrial Solutions named **Hui Hui Kiw** vice president Asia.

Mark Hughes, Jesse Robinson and **Kaushlesh Chandel** have founded Boondock Technologies.

Nano Dimension appointed **Gen. (Ret.) Michael Garrett** to its board of directors.

Schweitzer Engineering Laboratories promoted **Greg Zweigle** to CTO.

TTM Technologies CFO **Dan Boehle** was honored at the 2023 Los Angeles Business Journal CFO of the Year Awards ceremony.

CA

Henry Colina

Josh Zhou

Kim Newman

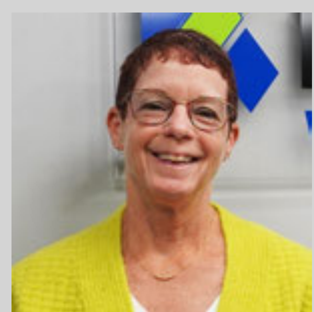
Landon Robertson

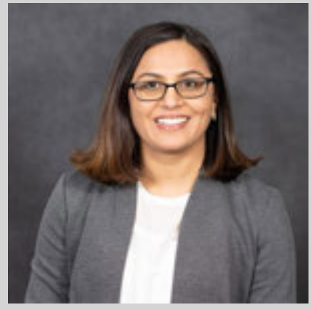
Atul Lall

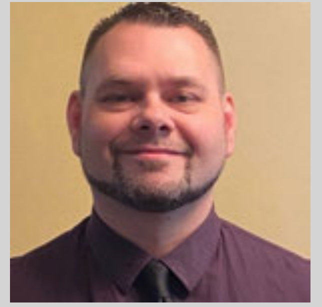
Lambert Schutters

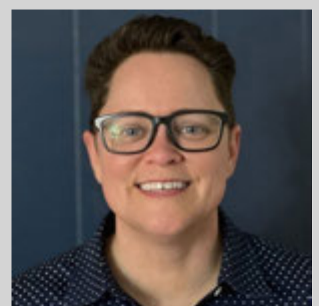
Yann Visintainer

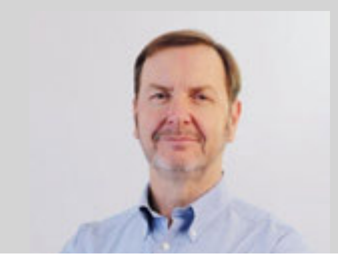
John Barraclough


Beth Bivins


Rubi Catuna


Jeff Schartiger


Jennifer Mullins



Battista Remati

Peter France

AIM Solder appointed **Henry Colina** technical sales engineer and **Josh Zhou** regional sales manager.

Alliance Memory appointed **Kim Newman** global account manager for Jabil.

Bowman XRF named **Landon Robertson** technical sales engineer for the US Eastern region.

Elcina elected Dixon Technologies' **Atul Lall** president for 2023-24.

Escatec promoted **Lambert Schutters** to CPO.

Entrepix hired **Yann Visintainer** as business development manager, EMEA.

Flex appointed **Tippy Wicker** operations manager.

Gen3 appointed **John Barraclough** head of business development.

Kyzen hired **Beth Bivins** as global key accounts manager for solvents.

NeoTech appointed **Rupinderjit "Rubi" Catuna** CFO.

RBB Systems promoted **Jeff Schartiger** to operations manager.

SelecTech named **Jennifer Mullins** inside sales representative.

StenTech appointed **Battista Remati** chief marketing officer.

TT Electronics appointed **Peter France** CEO.

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PCB Design Training Classes for 2024 Announced

PEACHTREE CITY, GA – PCEA Training is offering three upcoming training classes in 2024 over a span of five days (one class per week) for printed circuit engineers, layout professionals, and other individuals currently serving in the design engineering industry or seeking to get into it. The one-day-per-week class schedule varies from previous iterations in which classes were held five straight days.

Upcoming class dates include:

- Class 1: Feb. 5, 12, 20, 26, March 4
- Class 2: April 5, 12, 19, 26, May 3
- Class 3: June 14, 17, 21, 24, 28

These instructor-led classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

There are no prerequisite requirements to enroll. Upcoming classes will be held online. All courses

are led by experienced instructors.

Registration fees include a copy of *Printed Circuit Engineering Professional*, a 400-page handbook on circuit board design authored by Michael Creeden, Stephen Chavez, Rick Hartley, Susy Webb and Gary Ferrari.

The course includes an optional certification exam recognized by the PCEA.

For information about the course overview, class format, and materials to prepare in advance for the class, visit pceatraining.net/course-overview.

For information about the instructors of the course and authors of the course material, visit pceatraining.net/instructors-authors.

To enroll, visit pceatraining.net/registration for the next available class or email pceatraining@pcea.net for additional information.

PCB West 2024 Opens Booth Space to All Vendors

PEACHTREE CITY, GA – The exhibition floor for PCB West 2024 is now open to any interested company, the Printed Circuit Engineering Association (PCEA) announced in late October.

The show floor is expected to sell out, show organizers added, as booth space is now open to companies that did not exhibit last year.

Booth sales opened in mid-October to returning exhibitors, and the show floor is currently more than 50% sold out.

“PCB West has sold out nine of the past 10 years, and we fully expect it to do so again,” said Frances Stewart, vice president of sales and marketing at PCEA. “Attendance at the show was up 5% year-over-year in 2023, and attendees have noted the access to vendors and each other as the primary reasons why they come to PCB West.”

PCB West will be held Oct. 8-11, 2024, at the Santa Clara (CA) Convention Center. The event includes a one-day exhibition on Oct. 9.

For more information about PCB West, visit pcbwest.com.

PCEA CURRENT EVENTS CHAPTER

National. PCEA will hold a series of free webinars for members over the coming months. Topics include AI in electronics, component research and parts introduction, PCB material properties and how they affect design and processability, and additive manufacturing. Check the PCEA website calendar for updates.

Ontario (Canada). The chapter is planning an event in December. The likely speaker is Ata Syed, who is continuing a series on flex circuits.

Portland (OR). The chapter held a planning session in October as it prepares for its 2024 calendar.

San Diego. The chapter is looking for a meeting location. It is also on the lookout for guest speakers.

Silicon Valley. The chapter's next meeting is on Nov. 16. Cadence Design Systems will be hosting and sponsoring lunch. Michael Catrambone, product engineering architect for Cadence Allegro PCB products, is the speaker.

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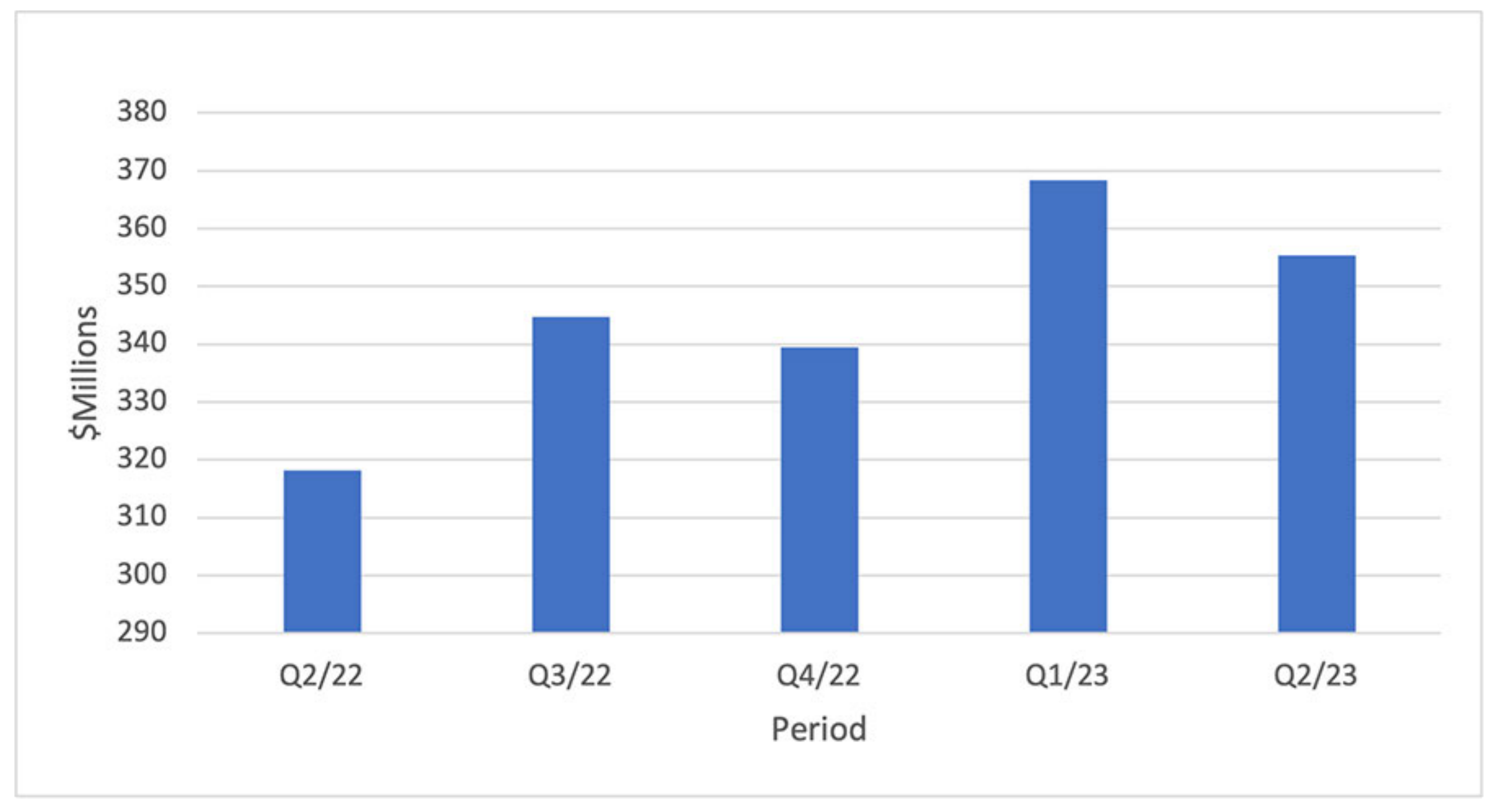
PCB Design Software Revenue Increases 6% in Q2

MILPITAS, CA – Printed circuit board and multichip module design software revenue increased 6.3% in the second quarter to total $369 million, according to the ESD Alliance in October. The four-quarter moving average for PCB and MCM, which compares the most recent four quarters to the prior four, rose 11.7%.

As a whole, ESD revenue increased 5.3% to $3.96 billion in the second quarter from $3.76 billion in the second quarter of 2022. The four-quarter moving average rose 9.5%.



PCB/MCM design software sales trends.

"Growth in total electronic design automation (EDA) revenue in Q2 23 was limited by weak semiconductor IP revenue," said Wally Rhines, executive sponsor of the SEMI Electronic Design Market Data report. "However, total license and maintenance revenue, which includes all design tools, was strong at 16.1% overall with double-digit growth in all regions except Japan."

The companies tracked in the EDMD report employed 59,160 people globally in the second quarter, an 11.8% jump over the headcount of 52,918 in the second quarter of 2022 and up 2.5% compared to the first quarter of 2023.

The Americas, the largest reporting region by revenue, procured $1.63 billion of electronic system design products and services in Q2 2023, a 0.6% decline. The four-quarter moving average for the Americas rose 7.5%. Europe, Middle East, and Africa (EMEA) procured $509.4 million, up 7.8%. The four-quarter moving average for EMEA grew 8.2%. Japan's share decreased 4.3% to $241.6 million. The four-quarter moving average for Japan fell 0.3%. Asia Pacific (APAC) procured $1.58 billion, a 13.1% increase. The four-quarter moving average for APAC grew 14.4%.

PC Push

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	JUN.	JUL.[r]	AUG.[p]	YTD
Computers and electronics products	-0.1	0.4	0.3	2.2
Computers	-2.4	3.9	4.0	11.3
Storage devices	-11.9	13.5	-2.8	12.8
Other peripheral equipment	3.8	-14.5	7.8	33.6
Nondefense communications equipment	1.4	0.3	-0.7	-1.5
Defense communications equipment	-3.4	5.6	-3.3	3.9
A/V equipment	8.6	44.6	-17.2	11.4
Components[1]	0.7	1.7	3.6	1.5

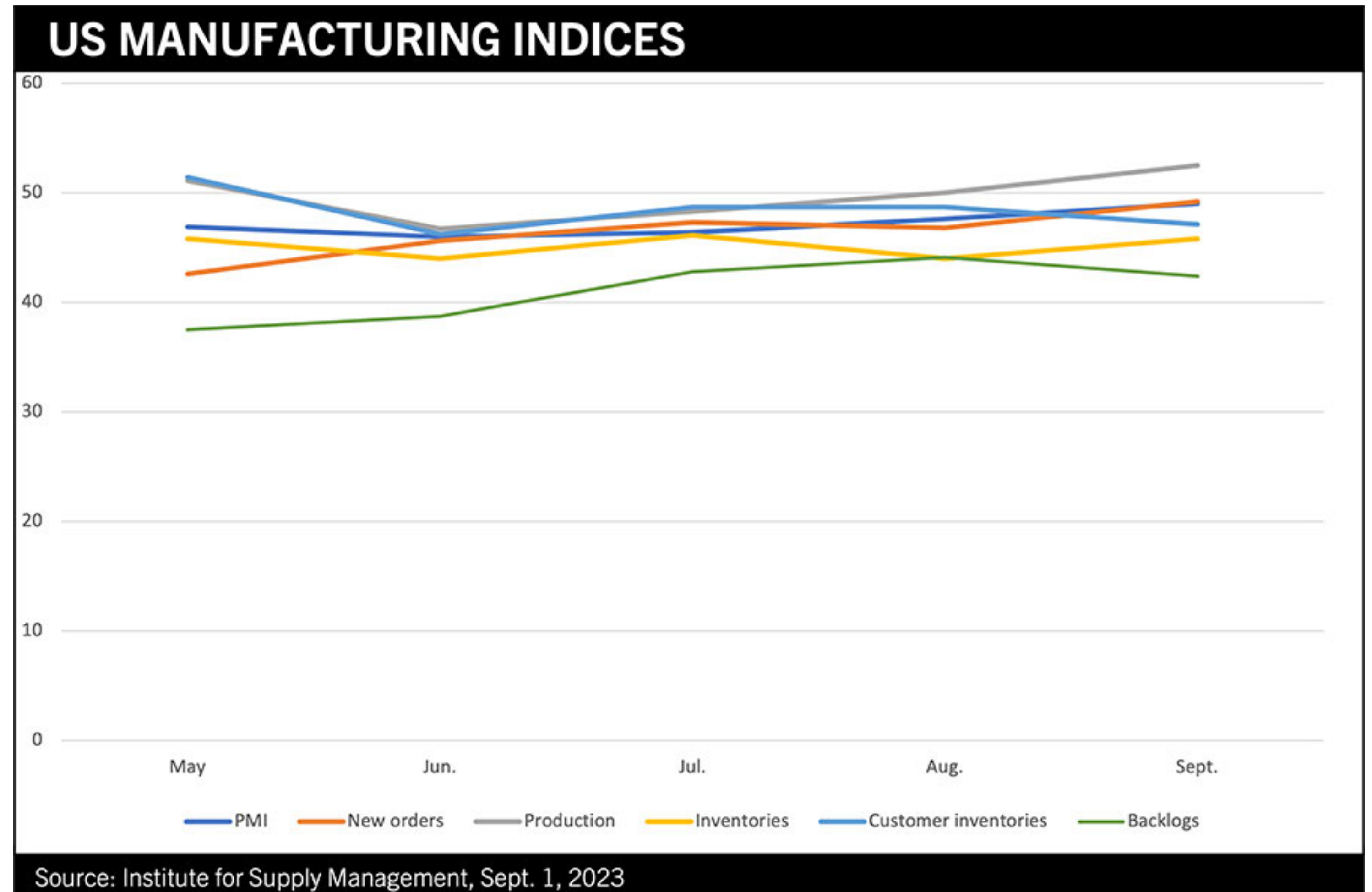
Components[1]	0.7	-1.7	3.6	1.5
Nondefense search and navigation equipment	-1.3	-0.4	-1.0	1.5
Defense search and navigation equipment	0.1	0.6	0.2	4.0
Electromedical, measurement and control	0.2	-0.1	0.9	1.3

[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Oct. 4, 2023

Key Components

	MAY	JUN.	JUL.	AUG.	SEPT.
EMS book-to-bill[1,3]	1.24	1.24	1.24	1.27	1.27
Semiconductors[2,3]	-21.1%	-15.7%	-11.8%	-6.8%	
PCB book-to-bill[1,3]	0.89	0.98	0.98	1.00	1.01
Component sales sentiment[4]	72.2%	76.3%	83.0%	90.3%	86.7%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA



Source: Institute for Supply Management, Sept. 1, 2023

Hot Takes

Orders for **electronic products** fell 17% year-over-year to $17.2 billion in September, attributable to lower demand for memory chips, foundry services and printed circuit boards as customers were in the process of digesting excessive inventory. (Taiwan Ministry of Economic Affairs)

Taiwan's PCB output has resumed its growth path after declining in the first half of the year, and is estimated to increase 8.1% annually. (Taiwan Institute of Technology and Research)

North American **EMS shipments** in September fell 9.8% compared to the same month last year, and dropped 12.4% sequentially. Bookings decreased 17.4% year-over-year and fell 14.2% from the previous month. (IPC)

North American **PCB shipments** fell 14.6% in September from a year ago but climbed 35.7% from August. Bookings slipped 32.7% from last year and jumped 45% sequentially. (IPC)

India's electronics exports hit a 13-month low in September, declining 3.7% from a year ago, and marking a contraction for the first time in 31 months.

Tech companies around the world laid off more than 400,000 workers in 2022 and 2023, according to Layoffs.fyi, a site that tracks job losses across the industry.

The global **notebook market** is set to rebound in 2024, with a projected 2-5% growth projected in yearly shipments. (TrendForce)

Solder accounted for the largest global share of **refined tin use** in 2022, increasing marginally to 50% in 2022. (International Tin Association)

Worldwide **IT spending** is projected to total $5.1 trillion in 2024, an increase of 8% from 2023. (Gartner)

Global spending on **GenAI solutions** will reach nearly $16 billion in 2023 and is projected to reach $143 billion in 2027. (IDC)

PC shipments declined 7.6% year-over-year to 68.2 million units in the third quarter. (IDC)

Japan's industry ministry is seeking funds totaling some 3.4 trillion yen ($22.8 billion) for **subsidies for the semiconductor industry** as part of economic measures to be finalized in October. (Japan METI)

NAND flash spot prices have started to rise, and in turn, suppliers have started reporting growth in their monthly sales. Price hikes for DRAM are relatively moderate, as DDR4 suppliers have not yet broken even in their operations. (TrendForce)

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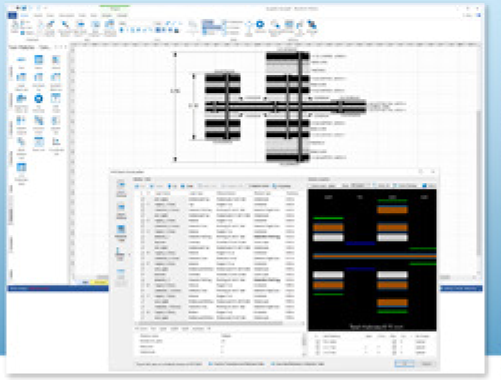
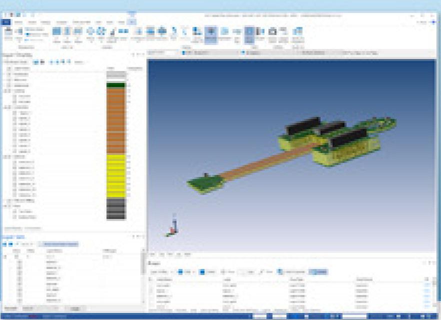
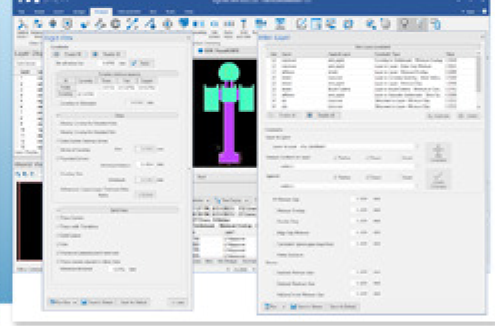
- Manage Variable Stackup Zones for Rigid-Flex Designs
- Easily Create Custom Flex or Rigid-Flex Fabrication and Assembly Documentation
- Use DFM analysis to analyze a flex or rigid-flex design for potential fabrication or bend related defects



Use Stack Up Visualizer and Blueprint's Rigid-Flex Stackup template to easily manage and document rigid-flex stackups.



A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



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Auditing the Auditors

They may be a hassle, but audits can provide valuable insights and ideas for your company.

DURING THE FOURTH quarter of this year, it seems that everyone and their brother have scheduled audits at my company. Some are for certifications such as ISO 9001 and AS9100. Others are customer-driven, as the cloud of Covid has at least partially lifted and after a three-year hiatus customers are able to travel to meet their suppliers. I have always hated audits; however, I also have learned that they can be a powerful tool when incorporated into the business planning process.

First, a disclaimer: I truly hate audits, for three basic reasons.

First, those conducting the audit – especially certification audits – have no clue what you make, the manufacturing challenges faced in producing the product, or industry-specific acceptability standards related to the product that you must meet. These auditors just follow a flat checklist and try to jam the proverbial square peg (your facility) into a round hole (their certification program).

Second, related to the first, is that auditors too often ask dumb questions that have no bearing on what or how you produce product or the quality of product you produce. One example from several years ago occurred during a customer audit when the "experienced" auditor asked, "Why don't you just plate the inside of a drilled hole instead of leaving plating on the entire panel?" 'Nuff said.

Third, more often than not, there is no reason for the audit. The audit wastes all their time and ours to validate that a company knows how to manufacture the product they produce.

With that as background, I have found that despite the above, audits can be useful if put into the context of a planning tool. Having different eyes looking at your facility, its processes, and deliverables validates that you know what you are doing and enables a company to create a punch list of "opportunities for improvement."

During certification audits, the auditor might not know anything about your industry, product or processes, but they have been in a wide variety of manufacturing facilities in a broad cross-section of industries that include large corporations as well as smaller companies. While querying the auditor about best practices they have seen – and the type of environments they were observed in – will provide many inputs that are not applicable to your company, it also will result in many inputs that could be very applicable and should be considered when planning improvements. Most will not be the type of input that causes an "aha!" moment, but many will be useful to tweak a process to improve efficiency or make it more robust.

Customers that audit your facility typically have audited many companies in your industry as well as a bunch of your competitors. When a customer audits your facility, engaging them to discuss best practices and observations can again provide some fodder for thinking about what could be implemented to improve your facility. No auditor will name the company they saw some process in, but they will provide input of the environment and size of facility they observed a process in. Again, many inputs based on an auditor's observations of best practices will not be applicable to your situation, but some will be gems to consider.

No idea, good or bad, can be investigated unless someone has the presence of mind to write it down. During an audit, typically the person doing the writing or documenting the event is the auditor. Regrettably, most of those being audited are simply supplying inputs, documents and responding to the auditor's questions. This is regrettable because the inputs and ideas discussed are often not written down for future consideration. Yes, a big idea discussed will be remembered, but little inputs that collectively add up to an implementable improvement instead get forgotten by all.

As with any type of business, some basic protocols should be incorporated into the audit plan before an audit is performed at your facility. Clearly, the auditor will drive the agenda, but those being audited should be made aware that they also should ask questions. When an auditor makes an observation or questions why your company is doing something, ask the auditor what alternative ways have they observed other companies doing the same or similar activity, and do not be afraid to

drill down to determine whether the environment in which the auditor observed an alternative method is applicable to your environment.

After the audit, besides discussing the auditor's findings and recommendations with your team, spend time with those involved to discuss what your team observed or learned that might be applicable to improving your company. Ideas that initially appear to have merit in pursuing should be assigned to the appropriate person to explore, investigate and report back to the team, optimally with an implementation action plan.

Yes, I still hate going through an audit, but over time I have learned that as intrusive as they may be, good information can be gleaned from the auditor that can lead to inputs and ideas that should be incorporated into the future business planning process to improve the business. By doing this, the time spent during an audit is no longer wasted time, but time well invested in the planning process.

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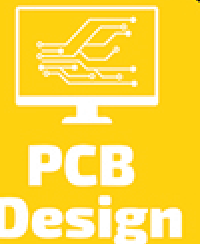

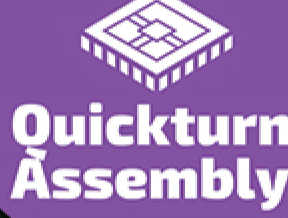

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DESIGNER'S **NOTEBOOK**

PCB Design for Virtual and Augmented Reality Headsets

"Non-standard" head shapes mean flex circuits are a given.

WE'VE COME A long way in the AR/VR space. It seems like we're going to have this stuff whether we want it at the moment or not. It's kind of like the Northwest Passage through the ice cap. It's new. We're not sure what the result looks like, but we're charging ahead with a virtual and/or augmented future.

Set the wayback machine to 1939, when both my father and the View-Master stereoscope entered the room. This wasn't long after Kodachrome was invented, so it was cutting-edge at the time. We put circular cards into the slot and could browse seven different views that somehow tricked the eye into seeing depth from isolating each eye on two similar slides **(Figure 1)**.

Figure 1. They still make these View-Masters 85 years after introduction. (Source: Target)

Back in “real” reality, this technology still has a lot of room to grow. It was about a decade ago when virtual reality started to bubble up into the lexicon at Google. We knew that a new industry was coming into existence and wanted to at least provide a gateway to the content. A group adjacent to the Chrome team developed a product called “Cardboard” that reminded me of the View-Master.

The difference between the View-Master and Cardboard is that each eye gets an altered video instead of a slide show. Add in some audio tailored to each ear and presto, you have virtual reality. Note that companies like HTC were already trailblazing the VR space back then. It continues to set the pace with a wide range of products for consumer and enterprise applications.

Creating content for VR is pretty fascinating; not just a green screen but a green world for the actors to play in. The rigging, lighting and multiple camera placements capture action in a way that immerses the user in the synthetic worldscape. Wearing the headset for the first time can be a little disorienting.

It’s hard to say exactly where all this is leading but immersive video games seem to be the essential starting place. While I was working on Daydream VR, around 2015, I had the idea of remotely

touring real estate as a possible application. Spurred by the pandemic, we now have that as an option in some apartment complexes. Still, I see virtual tours and remote learning as potential VR opportunities, though Daydream itself was taken off the market in 2019.

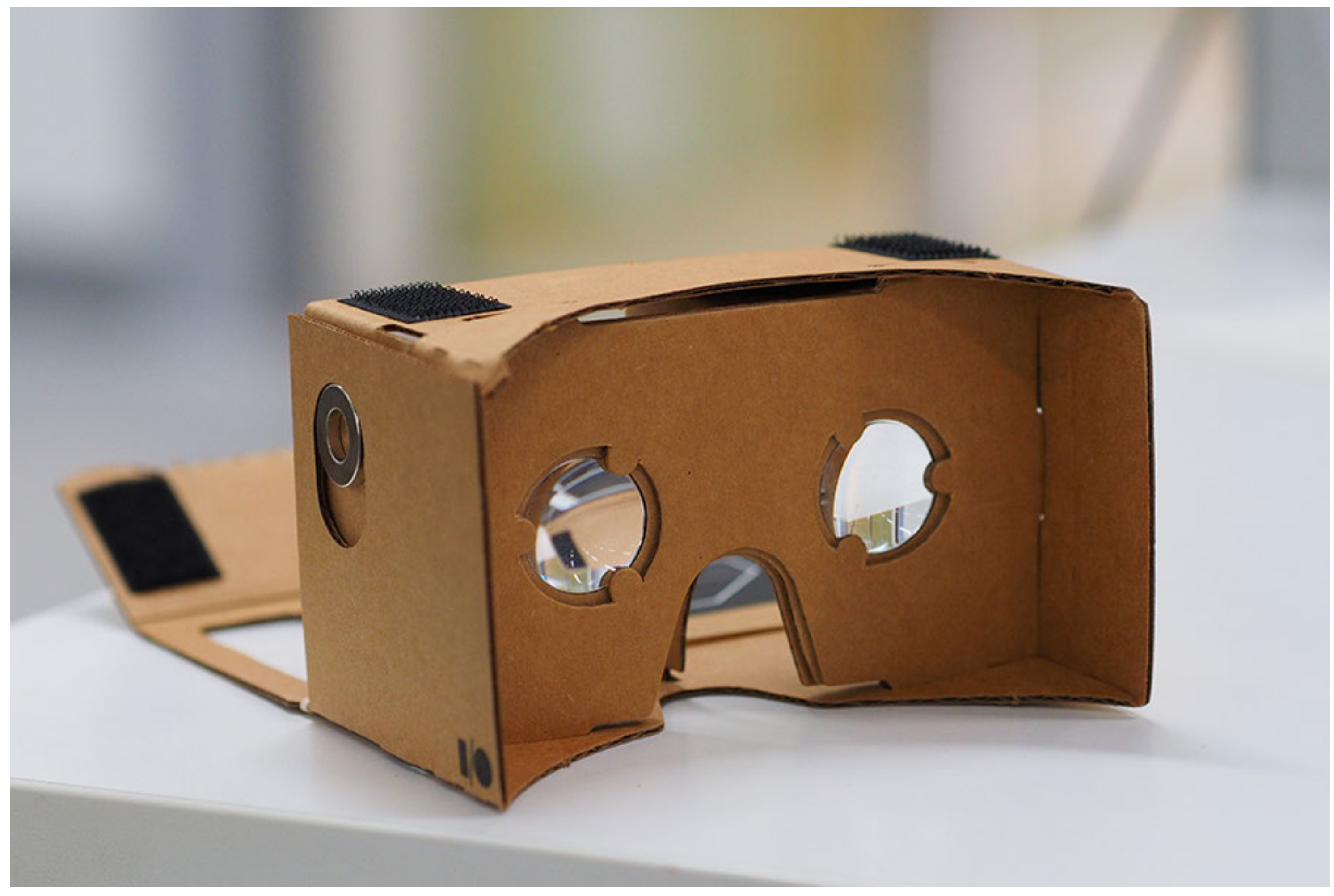

Figure 2. Just insert a smartphone and you're in a form of virtual reality. (Source: RoadToVR.com)

Why AR/VR is different in terms of PCB layout. Wearable technology deals with the human element, and we're not made of rectangles. The printed circuit boards that fill the volume of the headset must adapt to the shape of the average size person's head but with the means to accommodate larger and smaller people. Parts of the system must articulate as necessary.

Another aspect of streaming graphics is simply the amount of computational work that entails for the system. A device that warms your pocket is one thing. Warming your forehead is quite another. Those little flat fans that inhabit most laptops also find their way into mixed reality headsets. They are about as thick as the printed circuit board and often take up residence in a cut-out that would remind one of a nautilus shell as those fans use the same golden ratio principles to move air. Passive

cooling in addition to active heat spreaders is to be expected.

The main logic board of an AR/VR system has everything a smartphone has other than the actual phone call part. The SoC (system-on-a-chip) that went into the Daydream headset was the same SoC used in the Pixel 3 phone. I worked on the phone project just before jumping to virtual reality. Mobile chips are the thing for obvious reasons. The standard stack-up is going to be 12 layers with microvias for every layer.

Flex circuits: Endemic to mixed reality. Flex circuits get a lot of use in consumer electronics, especially with goggles and headsets. The unique anatomy each of us has means that the system must be adjustable in specific ways. Joining the HoloLens team exposed me to all the flexes that I sent off to the original design manufacturer (ODM) while at Google. That was an eye-opening experience in both flexes and rigid-flexes being way more than a purpose-built flat cable.

Think of the number of different sizes available at the optometrist. The distance between our eyes is a key factor that must be dialed in for the system to work properly. Meanwhile, our eyes are monitored by separate cameras to figure out which way we are looking while wearing the apparatus. The software uses that information to maximize the resolution of the virtual thing that you're actively observing.

The virtual and augmented worlds are all about control. Controllers usually come with the device and work in one of two ways. One uses at least two base stations in the VR space and triangulates on the headset and controller(s) using what amounts to LiDAR in the infrared band. This technology is known as the Lighthouse Tracking System and is found in HTC products. Meta, meanwhile, goes with infrared LEDs and tracks them with cameras rather than photodetectors. Its technology is called Inside Out Tracking.

The new spatial computer from Apple does away with the controllers, preferring to run off hand gestures that you would learn for different ways of manipulating items in mixed reality. I recall gestures being done on early Pixel phones. That wasn't the most popular user experience on the phone back then. Meanwhile, today's content creators have high praise for the hand tracking on the Vision Pro platform.

Credit no fewer than 12(!) cameras plus a lidar unit for the overall performance. That's even more

than a Tesla. What I know about it is just from Apple's marketing material. Augmented reality is adding content to the real world. Virtual reality is closer to a video game where the world is 100% special effects.

Either way, if you have to have a controller, you want six degrees of freedom; up, down, left, right, forward and back. It should be a simple design and robust enough so that you can break the wall-mounted television with it. For some reason, that seems to be the most video-worthy failure mode of virtual reality. Does artificial intelligence want you to punch your TV right in the mouth? The less-amusing failure mode is neck strain.

When it comes to wider adoption, less is more. It's not a huge leap to conclude that the only way the industry is going to really take off is to take considerable mass away from the whole system. The various circuits that make up the entire product must be further integrated into chipsets that combine more features, and that can be hard to do, especially when it comes to the plethora of sensors.

The interoperability of the various sensors depends on board layout to some extent. Every antenna, especially the unplanned ones, creates a new dimension of coexistence issues. Simply put, one more antenna or noise source doesn't add on, it multiplies the possible emissions problems.

Just combining WiFi and Bluetooth on a single radio chip is a huge challenge. To get the most from the experience, we want the new WiFi 6 with the 60GHz band that replaces the HDMI cable. Meanwhile, everything from batteries to memory chips must shrink for this to really work for everyone.

In the marketplace, the early adopters are always the ones to pay the price for getting a new product off the launch pad. Count camcorders and DVD players among my adoptees. Maybe someday, we'll be using a device on our heads to fly though a virtual printed circuit board looking for trouble from the signal's perspective. Our virtual future will arrive in one form or another. It will take time, but not another 85 years.

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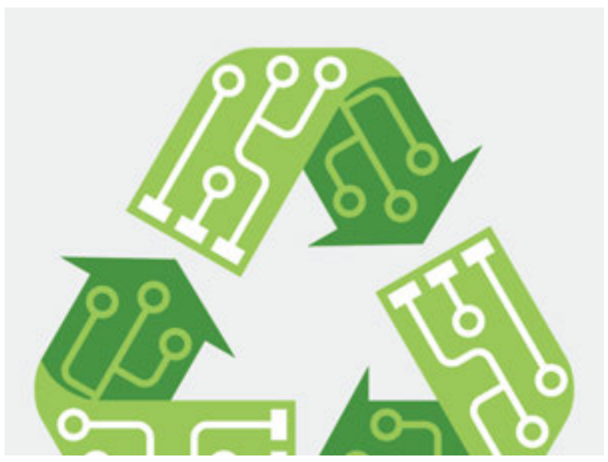
PCB Design Reuse

Reusing proven circuits and layouts can enhance innovation. Here's how.

IN THE EVER-EVOLVING field of engineering, the ability to innovate quickly and efficiently is paramount. Design reuse, a practice that involves repurposing and incorporating existing design elements into new projects, has emerged as a powerful strategy to achieve these goals. Boosting efficiency and innovation in the world of engineering, design reuse is a powerful strategy to implement that has the potential to be a game changer.

By reusing known, good, tested, validated, approved circuits and layouts, engineers can save design cycle time, reduce costs, and foster innovation. Plus, IP can be shared throughout enterprise and across designs. Design reuse is not restricted to one discipline as it can be implemented in all the engineering disciplines/domains. The key is to take advantage of the opportunity when it presents itself by not reinventing the wheel every time on a new project/design. This month's column delves into the concept of design reuse, its benefits, challenges, and how it's shaping the future of engineering.



What is design reuse? Design reuse refers to the practice of using previously created circuitry, layouts, PCB stackups, constraints, components, and hierarchical modules in new projects/designs or products. A good, yet simple example of design reuse is a library component. In this example, the component is created once, approved, and released into the master library. Then, that released component can potentially be used and reused repeatedly in multiple designs and throughout the enterprise. This same concept can be applied in a more complex yet efficient engineering approach to design. Instead of starting from scratch, engineers leverage existing proven designs as building blocks to create something new.

There are two main advantages for implementing design reuse. The first advantage is the time you'll save by implementing an existing proven design or circuit(s) rather than having to reinvent or recreate that same design or circuit in a new project/design. The second advantage is the use and implementation of already tested and validated components or circuitry. This translates to lower project risks since the new project/design is designed with partial or all reused proven/tested components or circuitry.

In addition to the two main advantages mentioned, even more benefits are to be gained from design reuse:

- **Cost savings.** Reusing designs can lead to substantial cost savings. It eliminates the need to invest in the development of redundant components and reduces expenses associated with redesigning or retesting parts of a project. This is particularly valuable for companies with tight budgets.
- **Enhanced collaboration.** Design reuse promotes collaboration by enabling teams to work on a common foundation. Engineers can easily share and modify designs, fostering a collaborative environment that encourages knowledge sharing and innovation.
- **Innovation.** Contrary to the misconception that design reuse stifles creativity, it can actually foster innovation. Engineers can focus on solving unique and complex challenges rather than reinventing the wheel. This allows them to explore more innovative solutions and concepts.

While the advantages of design reuse are evident, there are also challenges that engineers and organizations must address:

- **Compatibility issues.** Integrating components from different sources may lead to compatibility problems. Differences in design standards, software versions, or hardware specifications can create headaches if not carefully managed.
- **Intellectual property concerns.** Reusing designs may involve navigating complex IP issues. Engineers must ensure that they have the rights to use and modify existing designs or acquire the necessary licenses.
- **Documentation and version control.** Maintaining an organized and up-to-date repository of reusable designs requires robust documentation and version control systems. Without proper management, confusion and inefficiency can arise.
- **Resistance to change.** Some engineers may resist design reuse, preferring to stick to familiar methods simply because they don't trust another engineer's work. Overcoming resistance and promoting a culture of reuse within an organization can be a challenge.

Design reuse is a powerful strategy for PCB designers, electrical engineers and organizations looking to enhance efficiency, reduce costs, and foster innovation. While it presents some challenges, the benefits outweigh the drawbacks. As technology and collaboration/integration between engineering tools continues to advance, design reuse will play an increasingly critical role in shaping the future of PCB design, enabling designers and engineers to build upon the work of the past by utilizing proven designs.

STEPHEN CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience and integrating the design-to-source Intelligence insights from Supplyframe into design for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com.

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Preparing for 6G

While the 5G era continues to take hold, materials science must advance for us to move to the next stage.

IT'S PART OF the human condition to never be satisfied. We are always looking forward to what comes next, and this tendency is starkly evident in our attitudes toward technology. As our daily lives have become substantially enabled, empowered, and – many would probably agree – enhanced by the technology in our pockets, in our cars, and in our homes and offices, we have become increasingly demanding of more and better. More features and functions, more sophistication, faster responses, less waiting.

Our attitudes toward mobile services illustrate the point. No sooner had 5G networks started rolling out than the focus shifted to 6G and the exciting new opportunities it could bring. But is this a harsh truth about our nature, or simply the reality of a massive scientific and engineering challenge? The mobile industry has established a rhythm that introduces a new generation about once every 10 years: 3G arrived around 2000, 4G-LTE in 2010, and 5G rollouts based on Release 15 of the 3GPP specification began around 2020. 5G evolution has continued, with non-standalone deployments giving way to standalone 5G core and further enhancements in 3GPP Release 16 and 17 to support industrial IoT (IIoT) applications. Release 18 now paves the way for 5G Advanced, which will offer energy savings and greater spectral efficiency, leverage AI to improve network performance, and, of course, enable additional new services and enhanced capabilities.

To ensure 6G – taking performance, reliability, efficiency, and service advancement even further – can be ready for deployment by 2030, work needs to begin now to determine performance targets and start drafting specifications. Where 5G has brought advanced services such as cloud gaming,

augmented/virtual reality (AR/VR), and 4K video to our mobiles, 6G will raise the peak data rate from 5G's 20Gbps to 1Tbps and maximum bandwidth from 1GHz to 100GHz. Latency is expected to reduce from 1ms in 5G to just 100μs, while mobility will double from 500km/h to 1000km/h. Connection density is also expected to rise significantly, to 10 million devices per square kilometer from 1 million today. We can expect these improvements to be manifested in more immersive extended reality (XR) experiences and new capabilities in wireless positioning and remote sensing.

It's exciting to imagine all this happening, particularly as many of us will have a direct role in bringing it to life. Our wishes are constrained by the laws of physics, however: so often this is the issue that divides the possible and the impossible.

Materials science is one of the defining disciplines in the PCB industry. Substrate properties such as dissipation factor and dielectric constant are a limiting factor governing maximum data speed, signal power and transmission distance, and thermal management, while CTE and high-temperature performance heavily influence circuit integrity and reliability. We depend on the work of materials scientists and the properties of advanced synthetic materials such as the PPE (poly-phenylene ether) resins that allow us to engineer high-performing prepregs and laminates to handle multi-gigahertz signal frequencies and multi-gigabit data rates.

Currently, PTFE-based materials offer exciting opportunities to raise substrate performance to new heights. Its molecular structure has a very low dipole moment that ensures minimal absorption of energy from signals carried in the adjacent conductive foil. This extremely low energy loss enhances signal integrity at extremely high frequencies and demands less power at the transmitter in relation to signal-path length. Heating of the substrate is also reduced. Adjusting the PTFE resin/filler blend allows control over the dielectric constant of materials, permitting a range of Dk from a little over two to around 10 while the dissipation factor (Df) can be engineered to be extremely low, in the region of 0.002 or even 0.001. There are some challenges, however. From a technical standpoint, the low surface energy makes PTFE difficult to use for building multilayer substrates.

Despite this, the industry sees PTFE as an essential tool enabling the evolution of 5G networks and the transition to 6G in the future. However, PTFE – polytetrafluoroethylene – faces legislative challenges as a member of the group of synthetic chemicals known as PFAS, or per- and polyfluoroalkyl substances.

There are about 10,000 of these in existence, products of the global chemicals industry. They have become known as “forever chemicals,” or persistent organic pollutants (POP), because they decompose extremely slowly, if at all, and hence remain in the environment. They are widely used in a huge variety of products and processes, including liquid-resistant coatings, clothing, food packaging, even fuel-production processes. They are easily absorbed in the body – including ourselves and the animals we farm and eat – and can adversely affect the endocrine system.

There are moves to restrict the production and use of PFAS. Earlier this year, the European Chemicals Agency (ECHA) published proposals as an update to the EU’s REACH legislation. Clearly, restrictions would have major implications for many industries, including our own. CEFIC, the European Chemical Industry Council, have set up a dedicated sector group, FPP4EU, whose remit is to represent the views of producers, importers, and users of fluorinated products and PFAS and other parties with an interest in the fluorinated products and PFAS sector group activities in Europe. Its aim is to ensure that any eventual regulatory measures are science-informed, implementable and enforceable.

New materials suitable for substrate applications capable of delivering performance comparable to PTFE will be difficult to formulate: those strong molecular bonds that prevent degradation and earn their “forever” nickname are the same characteristics that ensure the high-frequency performance we need to build future mobile infrastructures, including 5G Advanced and 6G.

While the industry seeks exemptions, it’s equally important to begin work to engineer suitable alternatives. Quantum computing may help, having already shown its ability to accelerate materials science simulations. We need a solution, and fast. We also need to have faith in technology’s ability to deliver.

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Assessing Data Independence and Normality for SPC Charts

PCB chemical manufacturing processes can violate data independence and normality.

by PATRICK VALENTINE, PH.D.

The most critical assumption made concerning statistical process control (SPC) charts is that of data independence from one observation to the next (free from autocorrelation).[1,2] The second critical assumption is that the individual observations are approximately normally distributed.[1,2] The tabled constants used to calculate the SPC chart limits are constructed under the assumption of independence and normality.

Many printed circuit board chemical manufacturing processes can violate the assumption of data independence. This is because inertial elements drive reduction-oxidation (redox) chemical processes. When the interval between samples becomes small relative to the inertial elements, the sequential observations of the process will be correlated over time.

Statistical process control charts do not work well if the quality attributes charted exhibit even low levels of correlation over time. Correlated data produce too many false alarms – correlated data underestimate the upper and lower control limits.

Statistical process control charts are designed to capture 99.73% of the data within a ±3σ interval. In other words, there is a 0.9973% probability of not receiving a signal when the process is in control, the data are not autocorrelated, and normality is assumed. The distribution tails are symmetrical, each being 0.135% (100% – 99.73% = 0.27% / 2 = 0.135%) **(Figure 1)**. Non-normal data change the

tail probabilities. Departures from normality can significantly alter SPC detection rules.

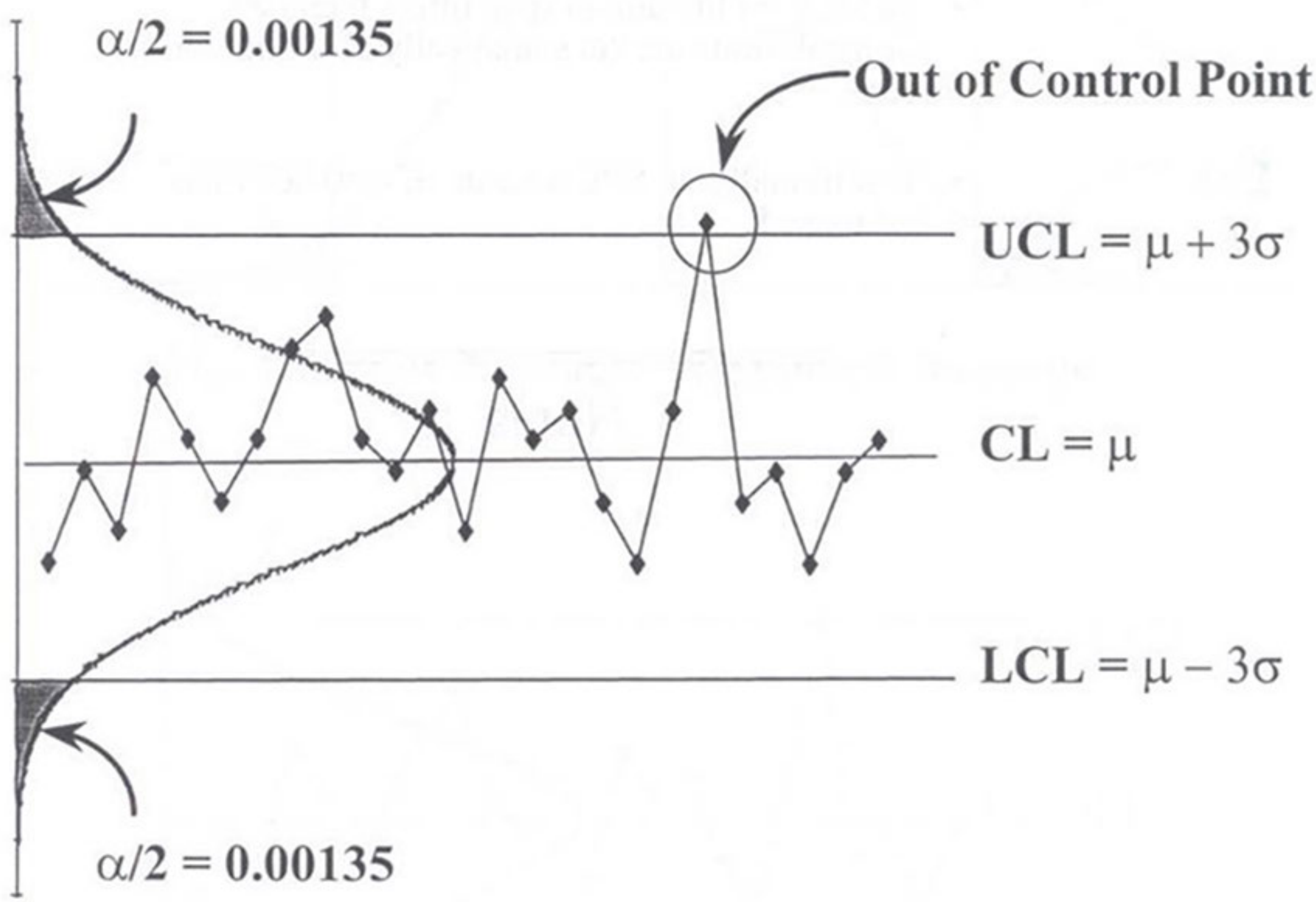


Figure 1. Symmetrical control chart.

Data Independence

There are two primary plots for checking data independence. These plots are the time series plot and the autocorrelation function plot. The time series plot is qualitative, while the autocorrelation function plot is quantitative. Details are given below.

Time series plot. Time series plots are an easy way to summarize a univariate data set graphically. Common assumptions of univariate data sets are that they have a fixed distribution, with a common location (mean) and common variation (standard deviation). With time series plots, shifts in location and variation are easy to see, and outliers can easily be detected, giving the process engineer an excellent feel for the data. Time series plots can answer the following questions:

1. Are the data independent?
2. Are there any shifts in location?
3. Are there any shifts in variation?
4. Are there any outliers?

Autocorrelation function plot. The autocorrelation function is used to detect independence in univariate data sets. The autocorrelation is a correlation coefficient. Instead of a correlation between two variables, however, the correlation is between two values of the same variable at times X_i and X_{i+k}. Although the time variable, *X,* is not used in the formula for autocorrelation, the assumption is that the observations are equispaced.[3,4] Usually, only the first few autocorrelations (lags 1, 2 and 3) are of interest in detecting independence. The autocorrelation function can be used to answer the following question:

1. Was the sample data set generated from an independent (random) process?

Data Normality

There are two primary plots for checking data normality. These plots are the histogram and the probability plot. The histogram is qualitative, while the probability plot is quantitative. Details are given below.

Histogram. The most common form of the histogram is obtained by splitting the range of the data into equal-sized bins. Then, the number of data points that fall into each bin is counted. This allows the histogram to summarize the distribution of a univariate data set graphically. These summarizations provide strong indications of the proper distributional model for the data, in this case, the normal distribution for SPC charts.[4] The histogram can answer the following questions:

1. What is the center of the data?
2. What is the spread of the data?
3. Are there any outliers?
4. Are there multiple modes in the data?

5. Are the data bell-shaped?

Probability plot. The probability plot is a graphical technique for assessing whether a data set follows a given distribution.[4] The data are plotted against a theoretical distribution so that the points should form an approximately straight line on the diagonal. Departures from this straight line indicate departures from the specified distribution. The probability plot can answer the following questions:

1. Does the normal distribution provide a good fit to the data?
2. What are reasonable estimates for the location and variation parameters?

Examples

The process engineer gathers two data sets from the electroless nickel immersion gold (ENIG) final finish line. Data set one: the cleaner concentration (ml/L). Data set two: the microetch's sodium persulfate concentration (g/L). The assumptions of data independence and normality are checked. Data set one is shown in **Figure 2,** and two in **Figure 3.**

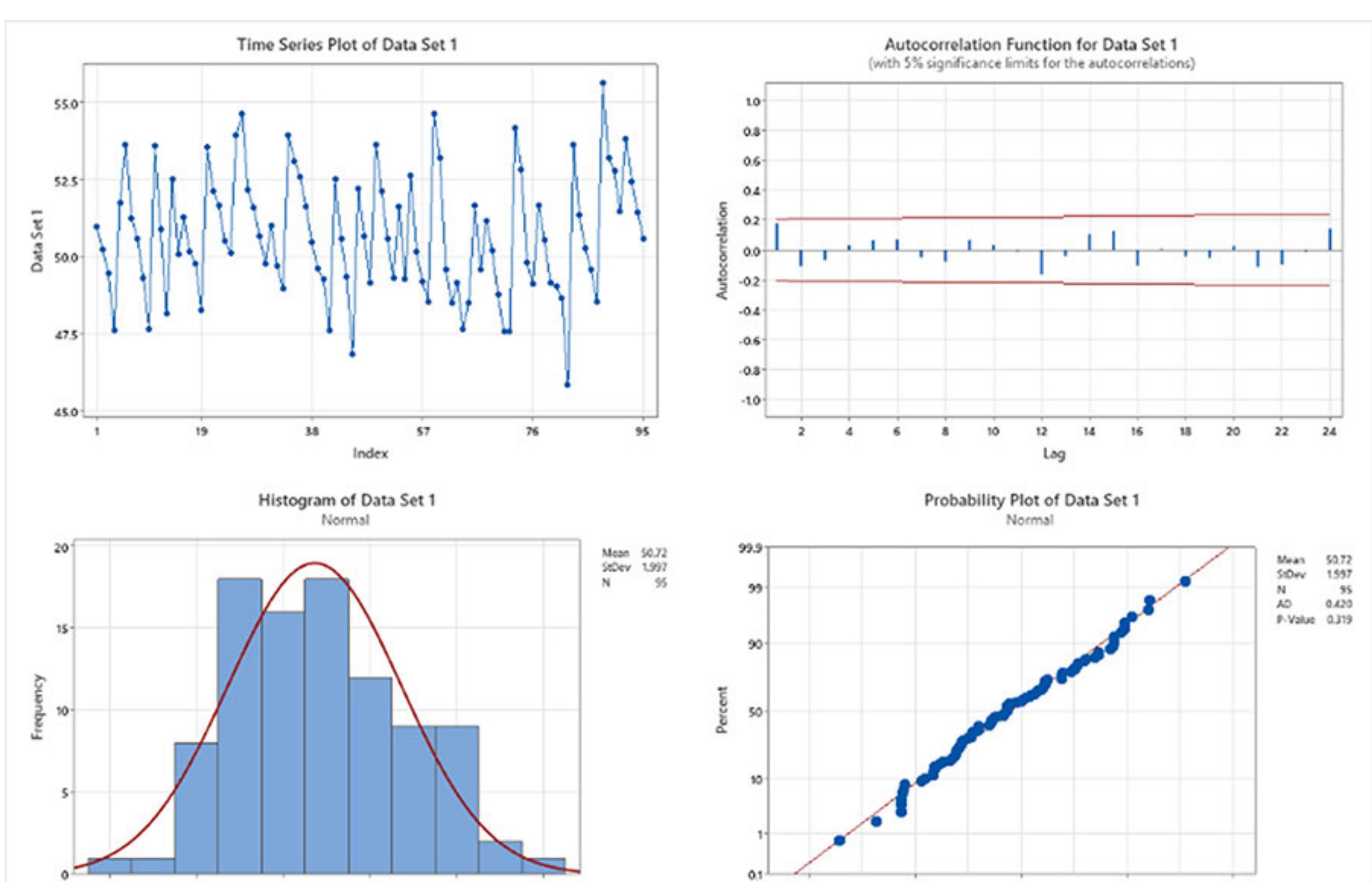


Figure 2. Data set one: four-in-one data independence and normality plots.

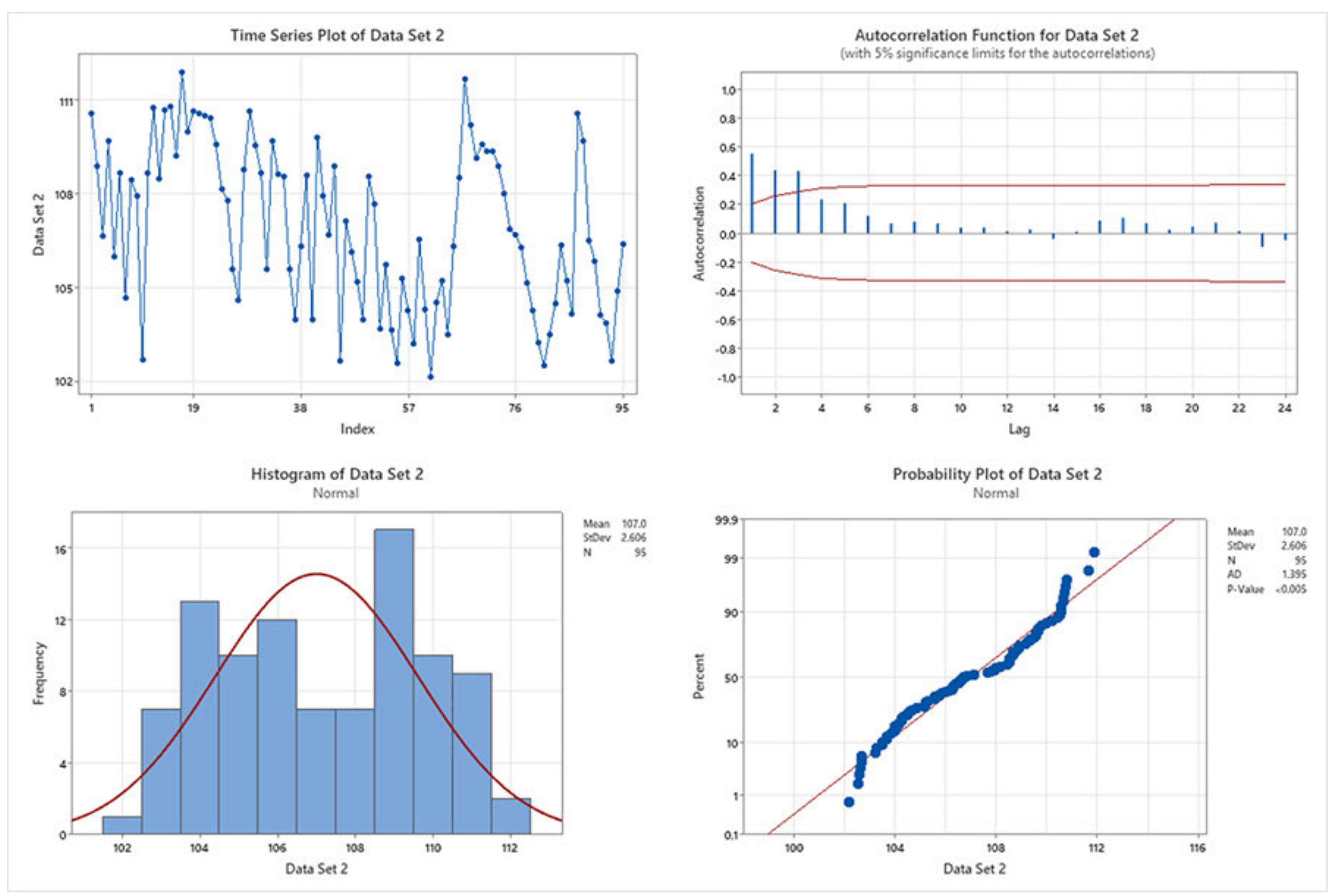


Figure 3. Data set two: four-in-one data independence and normality plots.

Data set one. The time series plot appears to have a fixed distribution, with a common location (mean) and common variation (standard deviation). There are no shifts in location or variation and no outliers. The autocorrelation function shows no statistically significant autocorrelations at lags 1, 2 or 3 (bars outside the red 95% confidence limit lines). The assumption of data independence has been met.

The histogram indicates that the data follow a normal distribution (a bell-shaped curve) and that there are no outliers. The probability plot points form an approximately straight line on the diagonal, and the p-value is significantly greater than 0.05. The assumption of data normality has

been met.

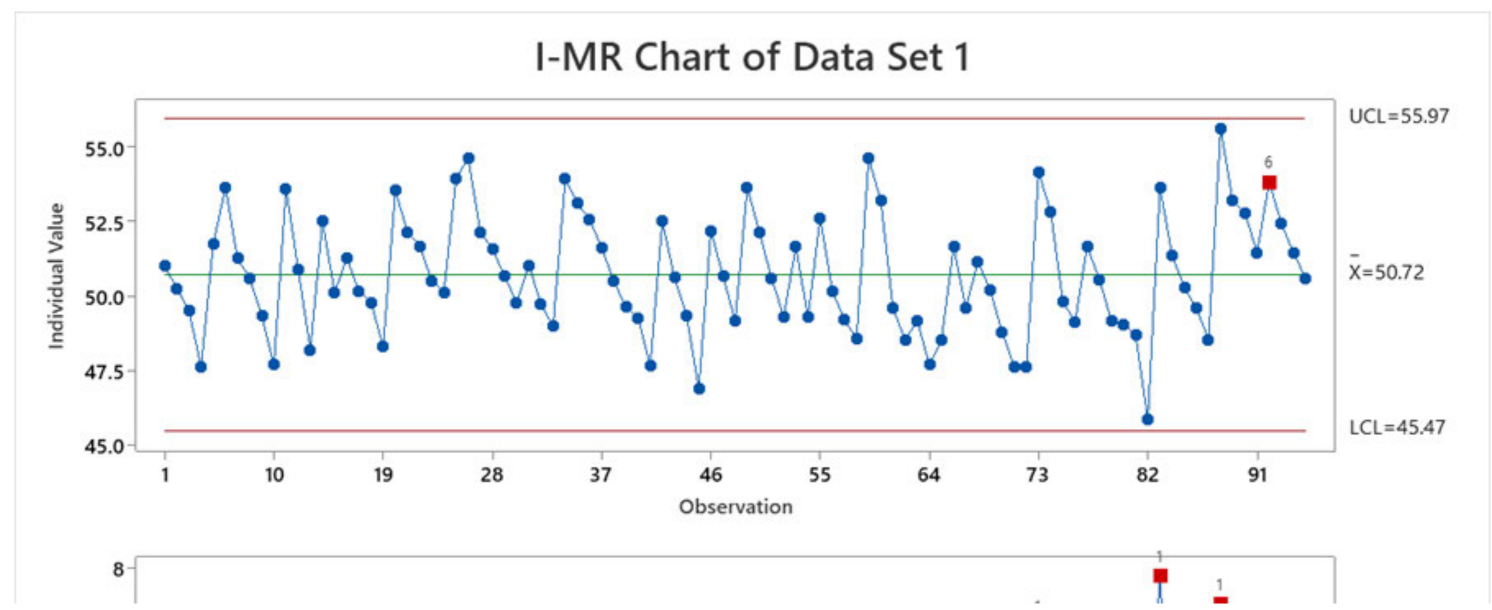
Data set two. The time series plot appears not to have a fixed distribution, and there is not a common location (mean) or common variation (standard deviation). There are shifts in the location and variation; no outliers are present. The autocorrelation function shows statistically significant autocorrelations at lags 1, 2 and 3 (bars outside the red 95% confidence limit lines). The assumption of data independence has been violated.

The histogram indicates that the data follows a bimodal distribution (two distinct peaks). The probability plot points do not form an approximately straight line on the diagonal, and the p-value is significantly less than 0.05. The assumption of data normality has been violated.

Statistical Process Control Charts

The two data sets were plotted on individual moving range SPC charts for discussion. Data set one is shown in **Figure 4,** and two in **Figure 5,** with the Western Electric Co. Rules violation points in red. The four Western Electric Co. Rules are listed below:[4]

1. One point more than three standard deviations from center line
2. Two out of three points > two standard deviations from center line (same side)
3. Four out of five points > one standard deviations from center line (same side)
4. Nine points in a row on the same side of the center line.



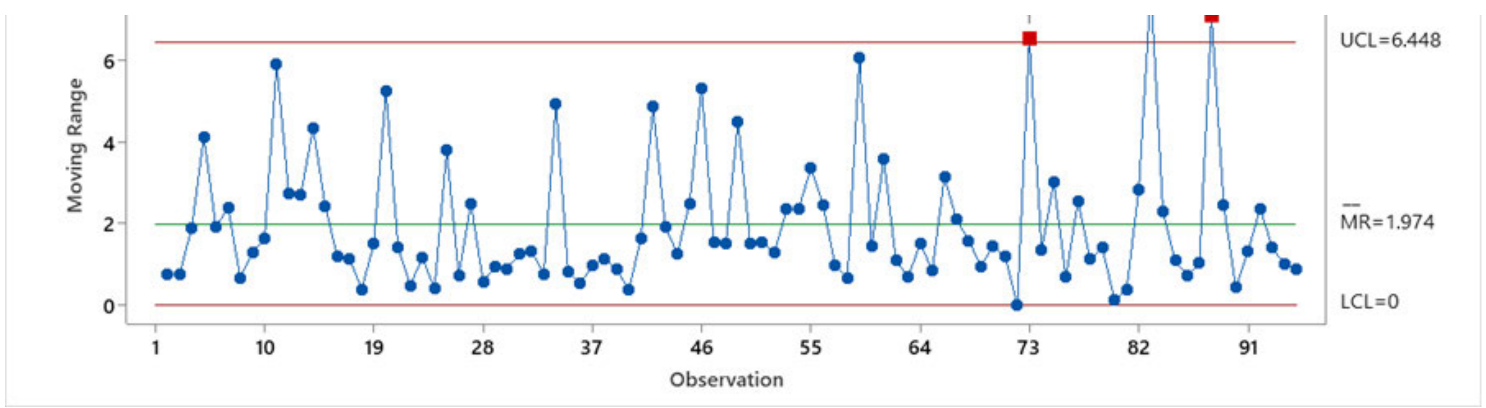


Figure 4. Data set one: individual moving range SPC chart.

Figure 5. Data set two: individual moving range SPC chart.

All detection rules are subject to Type I false alarms (a point falling beyond the control limits, indicating an out-of-control condition when no assignable cause is present).[1,4] False alarm rates are reported as average run lengths (ARL). The ARL tells us, for a given situation, how long, on

average, we will plot successive control chart points before we detect a rule violation. Using just the first Western Electric Co. Rule provides an ARL of ~371. Using all four Western Electric Co. Rules reduces the ARL to ~92. The process engineer must decide whether this price is worth paying (signal sensitivity versus false alarms). One strategy is to use the four Western Electric Co. Rules but take them "less seriously" regarding the effort put into troubleshooting activities when out-of-control signals occur.

Data set one discussion. The non-correlated data result in accurate upper and lower control limit estimations. The normal data provide the correct symmetrical tail probabilities. There are a few detection rule violations (points in red). The process engineer has reliable evidence that these rule violation points are out-of-control, not false alarms. The capability indices C_{pk} and P_{pk} should be computed. These capability indices will aid the process engineer in determining if the violation points are common causes or assignable causes.

Data set two discussion. The correlated data result in underestimating the upper and lower control limits. The non-normal data change the tail probabilities. There are many rule violations (points in red). The process engineer cannot determine which violation points are out-of-control or false alarms. The process engineer would waste valuable time investigating all the violation points. The capability index C_{pk} would be misleading and is therefore not recommended to be computed. The capability index P_{pk} would be much more informative.

Conclusions

Data independence and normality are underlying crucial assumptions for statistical process control charts. SPC charts do not work well if the quality attributes charted exhibit even low levels of correlation over time. Correlated data produce too many false alarms. Non-normal data alter the symmetrical tail probabilities. Violating independence and normality can significantly increase statistical process control detection rule false alarms. With a lack of data independence and normality, a process engineer has virtually no way of knowing which violation points are real and which are false alarms. Valuable time is wasted by not confirming the data's independence and normality before plotting them on a statistical process control chart.

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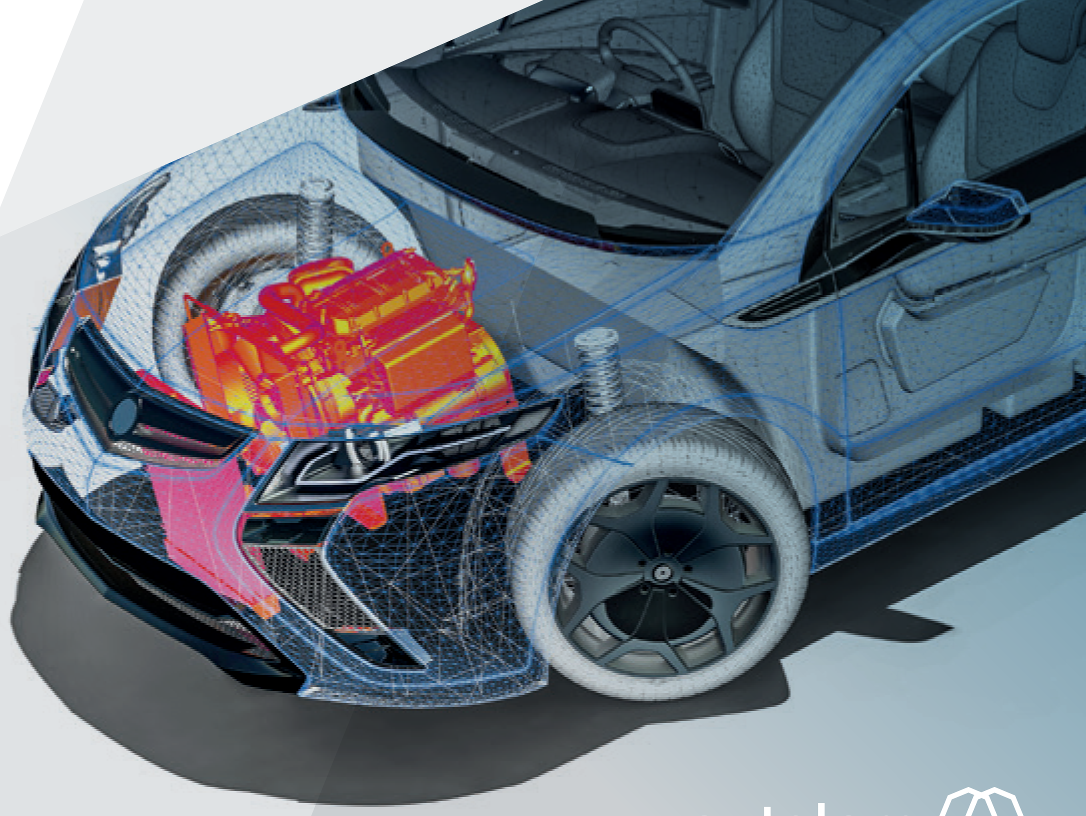

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Basics of High-Frequency PCB Materials

An overview of the physical and electrical characteristics of rigid and flex laminates.

by SAGI BALTER, PH.D. and VITALY BENSMAN

Electronic devices functioning at high frequencies are currently evolving at a dizzying pace, particularly within the field of wireless communication. When developing new products, therefore, emphasis is placed on utilization of materials suitable for high-frequency work, above 1GHz.

When selecting materials intended for high-frequency printed circuit boards, several characteristics are of importance:

- Dielectric constant (D_k) – dielectric coefficient of the resin. This parameter must be low and stable within a wide range of high frequencies. High D_k values may decelerate signal transfer speed.
- Dissipation factor (D_f) – the parameter responsible for the signal's quality. The D_f value should be low. The lower this value, the more stable the signal, and losses will be reduced.
- Moisture absorption – another imperative parameter when selecting materials intended for high frequencies. This is important because the D_k of water is $D_{k;water}$ = 80.4, a value so high, in fact, the absorption of very small amounts of moisture will instigate a significant increase in the overall D_k of the material.

- Coefficient of thermal expansion (CTE) – thermal dimensional expansion parameter of the dielectric material. This parameter must be close to the CTE of the conductive metal; in the case of PCBs, it is copper. Working at high frequencies causes increased heating of the PCB and thus if a significant discrepancy exists between the CTE of the dielectric material and the copper, structure delamination may occur during the activation of heating/cooling cycles.

- Additional important parameters such as:

  o Thermal resistance.
  o Chemical resistance.
  o The adhesion strength between copper and the dielectric material.

Traditionally, PCBs intended for high frequencies are designed or manufactured using polytetrafluoroethylene (PTFE)-based materials, known widely as Teflon. In fact, presently, a wide range of resin-based materials, such as epoxy-glass, are suitable for production of PCBs intended for diverse applications of high-frequency.

One of the common methods for improving the performance of non-PTFE-based materials (and that of PTFE-based materials as well) in high frequencies is to select a suitable type of copper, meaning the roughness profile.

When working with high frequencies, an influential and significant phenomenon for signal transfer quality is called skin effect. As frequency increases, the electromagnetic field generated as a result of electron conduction in the conductive material influences the flow of the electric current in the conductor and "shoves" it closer to the outer skin.

The skin effect phenomenon intensifies the impedance and causes increased conduction losses as well as deceleration of signal transfer **(Figure 1)**. Upon increase of the frequency, the skin depth (the skin's thickness) is reduced.

The Skin Effect

Frequency	Skin Depth (Copper)
50 Hz	9.3 mm
10 MHz	21 micron
100 MHz	6.6 micron
500 MHz	2.95 micron
1 GHz	2.1 micron

5 GHz	0.93 micron
10 GHz	0.66 micron
30 GHz	0.38 micron
50 GHz	0.30 micron
80 GHz	0.23 micron

Figure 1. Skin effect and typical values.

To reduce skin effect during production of copper-clad laminates (CCL) intended for high-frequency use, low-profile copper is used at the bonding side – the side adjacent to the dielectric resin **(Figure 2)**. The main types of copper utilized in the production of CCLs are standard, low-profile and very low-profile.

Resist side

Standard foil

~10 µm

Bonding side

Frequency	Skin Depth
10 MHz	21 µm

Signal Path

The current is able to tunnel below the surface profile and through the bulk of the conductor

Frequency	Skin Depth
100 MHz	6.6 µm

The current is forced to follow every peak and trough of the surface profile increasing path length and resistance

Figure 2. Copper roughness and skin effect. (Source: Isola)

To improve performance, low-profile copper with tooth size (roughness) less than 5µm is preferred **(Figure 3)**. Nonetheless, if using this type of copper foil combined with PTFE, which is known to have low adhesion strength, consider that the likelihood of delamination between the copper and PTFE in the diverse production processes, as well as thermal shock, is very high. This point is

precisely when thermoset materials (such as epoxy-glass), which possess a high adhesion strength to copper, gain an advantage over PTFE.

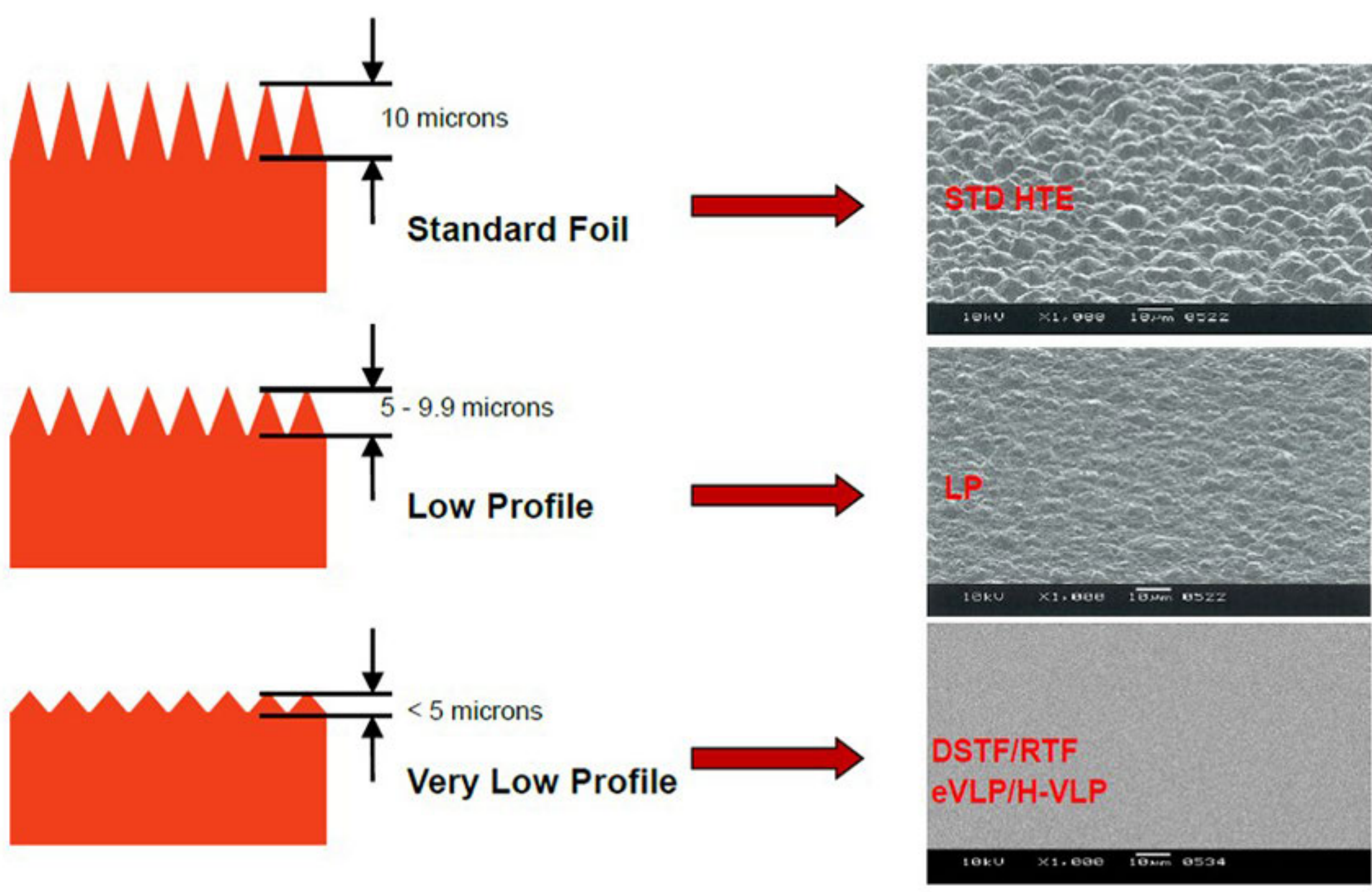


Figure 3. Copper roughness.

In addition to the copper type, meaning the roughness characteristic, another parameter contributes to the stability of signal transfer in a PCB. The dielectric base of CCL exhibits a nonhomogeneous and anisotropic structure in terms of D_k values.

In general, the D_k values for resin and glass fibers are not identical: D_k resin < D_k glass fiber.

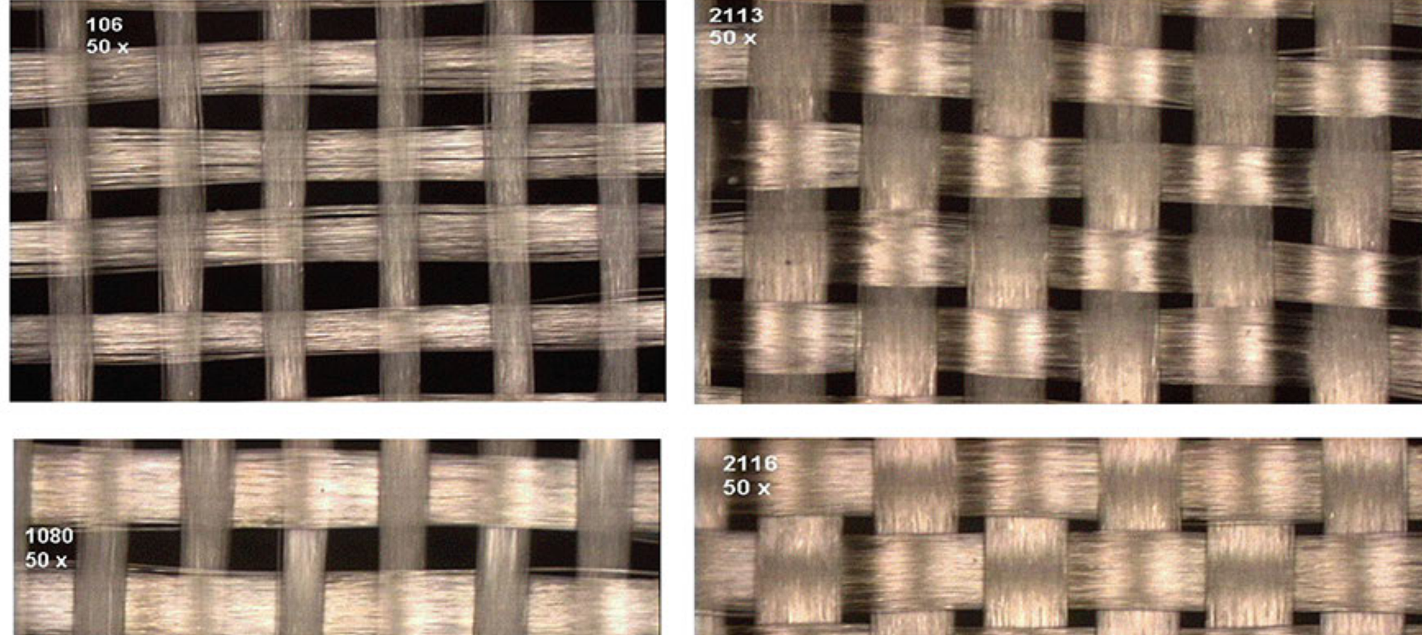
A conductor that will traverse over a fiber bundle (1) and a conductor that will traverse over a resin-saturated area (2) will exhibit a different D_k **(Figure 4)**. The solution proposed for this phenomenon is the utilization of a more homogenous glass fabric, such as 2116 or 3113, instead of 1080 or 106, or the use of flattened glass fibers, such as spread glass, which enables the production of a more homogenous dielectric material **(Figure 5)**.

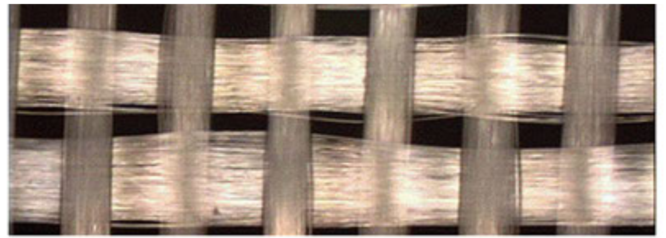
1080
50 x

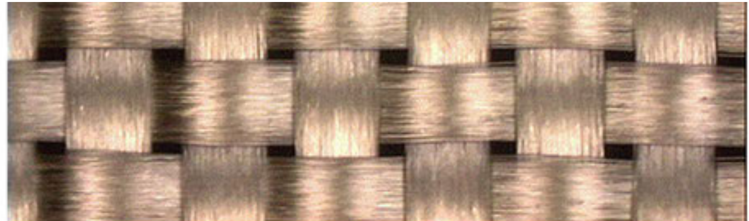
(1)

(2)

Figure 4. Conductors that traverse over fiber exhibit a different D_k than those that traverse over resin.







Standard Glass Spread Glass

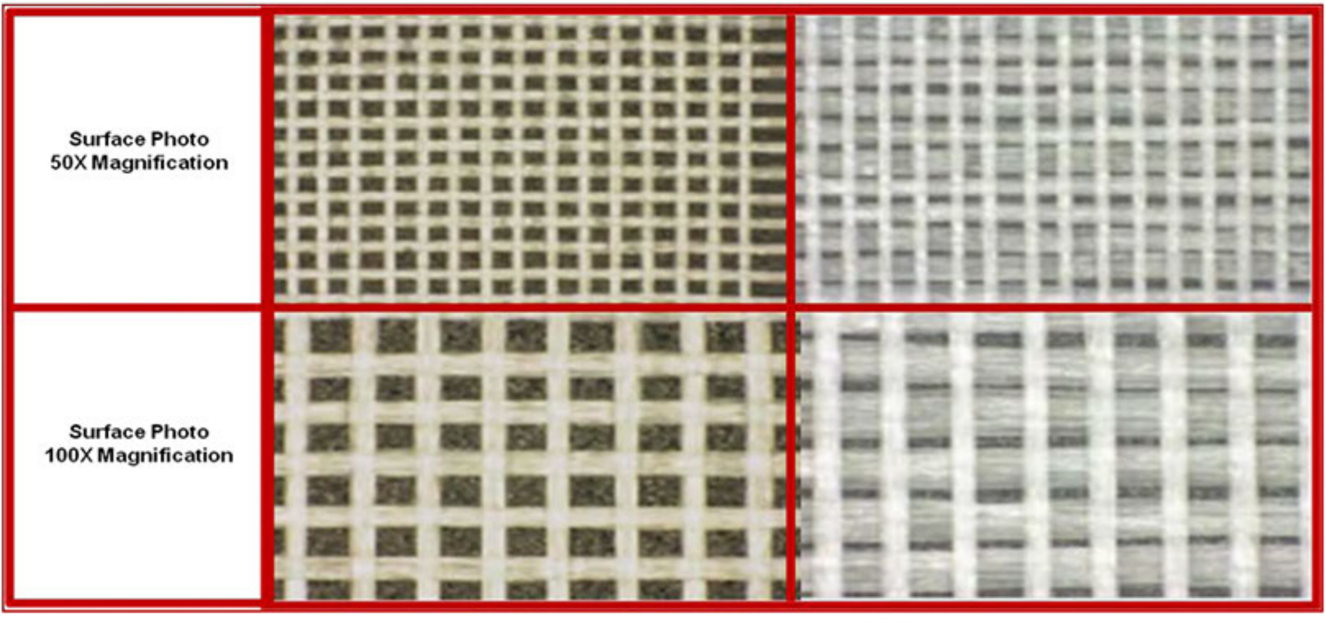


Figure 5. Glass fiber types. (Source: Isola)

Naturally, the PTFE resin occupies a prominent place in a very broad variety of raw materials designated for PCB production. Presently, companies that produce PTFE-based CCLs offer varied solutions for improving the electrical performance of these materials; for instance: improving dimensional stability through use of glass fiber fabrics or other hardening materials; utilizing ceramic fillers for controlling the D_k or D_f values. Another advantage of PTFE is its very low moisture absorption level and high resistance in aggressive work environments.

On the other hand, PTFE has significant disadvantages in the production processes of PCBs: high cost; low copper adhesion strength; significant difficulties in the preparation of surfaces for copper plating in holes and lamination with other materials. In most cases, use of PTFE-based CCLs requires PCB manufacturers to use multiple expensive, complex and aggressive processes, which raise the price of the final product and influence yield of Teflon-based PCBs.

RD Cu

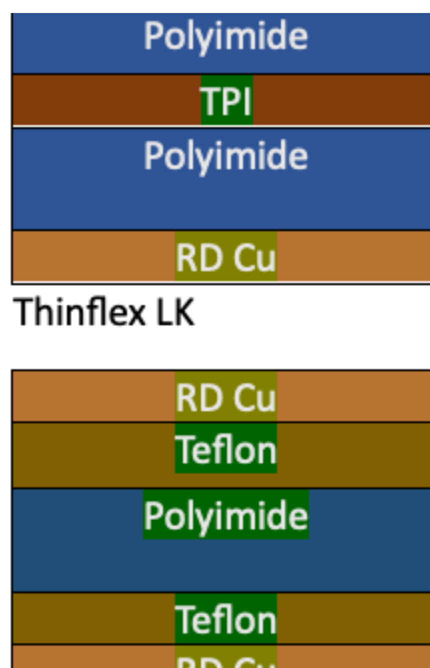


Figure 6. Thinflex LK and Pyralux TK constructions.

In work frequencies ranging above 10GHz, Teflon-based raw materials have very few competitors, nonetheless, a range of alternative glass epoxy-based materials are available in frequency ranges of 1 to 5GHz, such as PPO (polyphenylene oxide) or PPE (polyphenylene ether) as well as diverse polymer mixtures.

Currently many companies manufacture CCLs intended for high frequencies. For Teflon-based laminates, they include (but are not limited to):

- Rogers – with the following series of materials – RO3000, RT/Duroid and CuClad series as well as several additional types.
- AGC (Taconic) – with the TLY, TLC and RF series of materials, and a few others.
- Ventec – with the Tec-Speed 30.0 series of materials (a relatively new material on the market).

Some technical data for PTFE materials are shown in **Table 1.**

Table 1. Technical Data for Select PTFE Materials

	Rogers				
Property	RO3203	RT/Duroid 5880	RT/ Duroid 6002	AD250C	CuClad250
D_k	3.02	2.20	2.94	2.50	2.50
D_f	0.0016	0.0004	0.0012	0.0013	0.0017
CTE (ppm/°C)					
X/Y	13	31/48	16/16	47/29	18/16
Z	58	237	24	196	177
Water absorption (%)	<0.1	0.02	0.02	0.04	0.03
Td (°C)	500	500	500	500	N/A

	AGC				
Property	RF30A	TLC32	TLE95	TLY5A	TLY5Z
D_k	2.97	3.20	2.95	2.17	2.20
D_f	0.0020	0.0030	0.0026	0.0009	0.0015
CTE (ppm/°C)					
X/Y	8/11	9/12	9/12	26/12	30/40
Z	60	70	70	217	130
Water Absorption (%)	N/A	N/A	0.02	0.02	0.03

	Ventec	
Property	Tec-Speed 30.0 (VT-6702)	Tec-Speed 30.0 (VT-3703)
D_k	2.94	3.00
D_f	0.0011	0.0019
CTE (ppm/°C)		
X/Y	N/A	16/17
Z	24	25
Water Absorption (%)	0.02	0.04
Td (°C)	520	520

For laminates based on non-Teflon materials, several companies also supply products, including but not limited to:

- Isola – with materials such as I-Tera MT40, Astra MT77, Tachyon 100G.
- Ventec – with the Tec-Speed series of materials.

Some technical data for non-Teflon materials are shown in **Table 2.**

Table 2. Technical Data for Select Non-PTFE Materials

	Isola		
Property	**I-Tera MT40**	**Astra MT77**	**Tachyon 100G**
Tg °C (DSC)	200	200	200
Td °C	360	360	360
D_k	3.45	3	3.04
D_f	0.0031	0.0017	0.0021
CTE X/Y ppm/°C	12/13	12/13	15/15
CTE Z (50°-260°C) %	2.8	2.9	2.5
Water absorption (%)	0.01	0.10	0.10

	Ventec		
Property	**Tec-Speed 20 (VT870)**	**Tec-Speed 7.0 (VT463-H)**	**Tec-Speed 5.0 (VT464-G)**
Tg °C (DMA)	280	220	175
Td °C	402	430	400
D_k	3.3	3.7	3.81
D_f	0.0025	0.0018	0.0031
CTE Z (50°-260°C) %	35	45	35
Peel strength lib/in	6	4.5	5
Water absorption (%)	N/A	0.1	0.08

In addition to rigid materials, special flexible materials are utilized for production of flexible/rigid (rigid-flex) PCBs intended for high-frequency use. In fact, in the field of flexible materials for high frequencies, as of today, the materials available are modest compared with rigid versions. Presently, only two companies provide flexible materials intended for high-frequency use: DuPont with its Pyralux TK material, and Thinflex with its Thinflex LK material.

Pyralux TK is an adhesive material that uses Teflon-based adhesive for bonding the flexible base polyimide (Kapton) and the copper foil layers. As a result of the use of Teflon-based adhesive, this

flexible material is characterized by advantages and disadvantages similar to Teflon-based rigid materials.

Thinflex LK is an adhesiveless material made of a polyimide base layer and copper foil on both sides. The production processes of PCBs with a Thinflex LK layer are identical to production processes using standard flexible materials.

Technical data that characterize Pyralux TK and Thinflex LK are shown in **Table 3.**

Table 3. High-Frequency Polyimide Specifications

Property	Pyralux TK	Thinflex LK
D_k (10GHz)	2.5	2.8
D_f	0.002	0.005
Peel strength (kgf/cm)	>0.7	>0.6
CTE (ppm/^{o}C)	27	28
Peel Strength (lib/in)	6	4.5
Water absorption (%)	0.6	1.0

In conclusion, in our experience the most suitable materials for conventional and standard production processes are epoxy glass-based thermoset materials and non-Teflon materials that are adapted for use in high-frequency ranges. As opposed to Teflon-based materials, thermoset materials can be used for building a variety of rigid, rigid-flex and HDI (high-density interconnect) PCBs. It is impossible to ignore that the most efficient materials for high-frequency performance that are suitable for a wide range of frequencies are Teflon-based materials, yet these materials pose numerous fabrication challenges, the cost of this type of product is very high, and its production time is significantly longer compared with the other materials.

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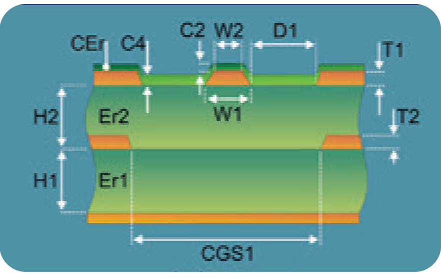

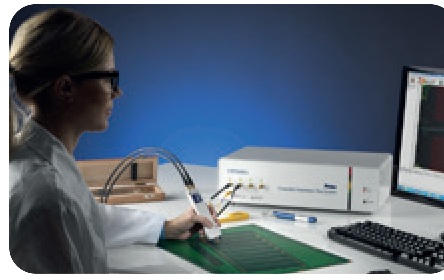

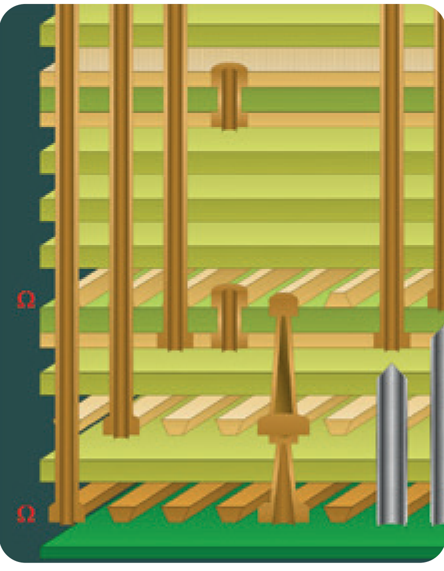

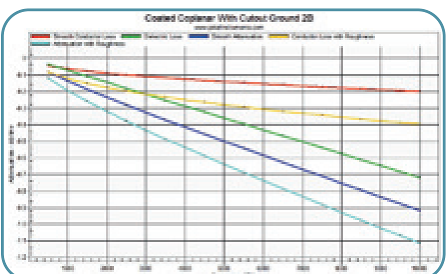

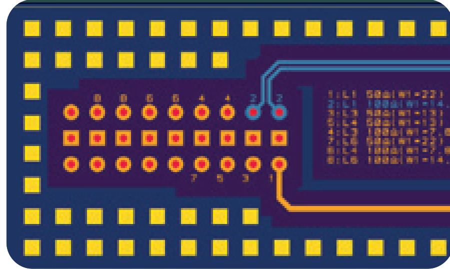

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HARDWARE **DESIGN**

5G Open Radio Unit White Box

An overview of the design and development process.

by MUHAMMAD IRFAN

5G radio networks provide increased bandwidth at the expense of reduced range. To compensate for the reduced range and to increase coverage, availability of cost-effective radio units is critical. In collaboration with Intel, Analog Devices, Comcores and Radisys, Whizz Systems has developed a 5G Open Radio Unit (ORU) white box solution to meet this market need. A broader overview of the 5G architecture can be found in Comcores[1] and Radisys.[2]

Here we provide an overview of the design and development process for the various hardware components that make up the 5G ORU white box. Whizz Systems is responsible for the electrical, thermal, mechanical engineering and manufacturing aspects, as well as system validation and bring up of the turnkey white box ORU solution. This includes design of the individual PCBAs and industrial design of the enclosure.

The hardware design leverages Intel's Arria 10 reference design as a starting point, with power and clocking schemes revamped to meet the updated power and clocking requirements for the ORU platform. An additional JESD interface as a communication pathway is added between the Arria 10 FPGA and Analog Devices-based chip ADRV902X. A board-to-board (BTB) header is added to mate with either the ADI-designed radio frequency front-end (RFFE) card or the Whizz-designed ORU adapter card.

SI/PI simulations are carried out to guarantee the design meets requirements of the 5G ORU. The mechanical team designed the chassis and simulation of thermal characteristics of the board for heat sink and fan selection.

The 5G white box PCB is fabricated at Whizz Systems using internal standards for process and inspection. The manufactured board is tested for shorts, proper power on sequence, and bring up of all interfaces. Finally, the software team is involved for validation of QSFP, DDR, Madura and other major subsystems.

Hardware Electrical Specifications

The white box product consists of both the ORU PCBA and the RFFE PCBA, but the focus here is mainly on ORU design. The ORU card is designed using a low-power, high-performance and logic-intensive Arria 10 SoC processor to create custom radio solutions with 4T4R TDD (four transmit and four receive time division duplex) communication radio link with a tunable range of 600MHz to 6GHz, with a 100MHz signal bandwidth (oBW).

The white box ORU card design supports Arria 10 SX 320/480 SoCs and has onboard 1GB DDR4 HPS memory and 2GB DDR4 FPGA memory **(Figure 1)**. The design also hosts a 1Gbps Ethernet interface, a USB-to-UART interface, and two optical QSFP ports with each channel capable of 10Gbps, with a total transfer rate of 40Gbps along with 1PPS/10MHz clock for external synchronization. Two warm/cold reset push switches for the Arria 10 are on the faceplate along with a slide switch for power cutoff.

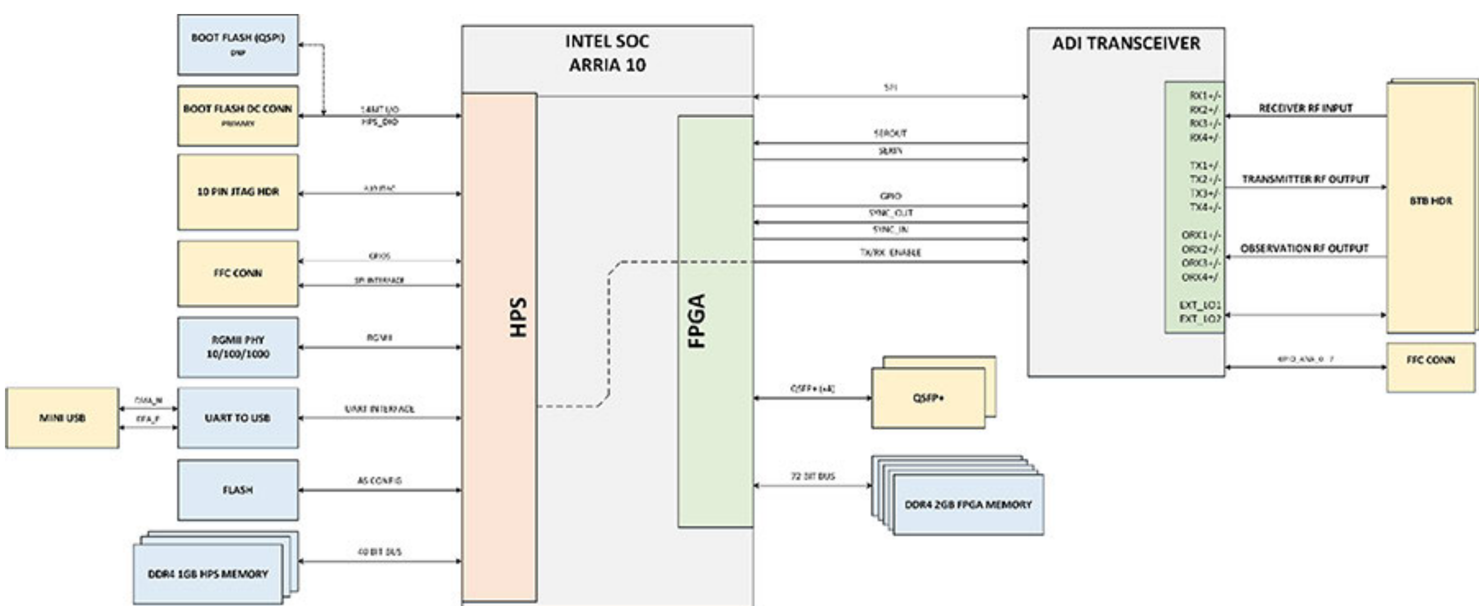


Figure 1. System block diagram for the ORU card.

The Arria 10 communicates with the QSFP ports using two SERDES banks, has dedicated RGMII

interfaces for the ethernet port, and uses a UART port for UART-to-USB conversion. HPS/FPGA banks are used for the HPS/FPGA memories whereas a JESD interface in the form of SERDES is used to communicate with the ADI ADRV902X chip.

The user can use the onboard BTB boot flash connector to mount either an SD card module or a QSPI module as boot-up options for the device. The board also hosts a total of three fan headers, eight user LEDs, an eight-port SPST dip-switch and six-pin user IO connector.

The 5G white box radio card also provides support for IJ5 series Samtec board-to-board connector for an external RFFE/adapter board and another board-to-board connector for an external SD card boot flash for the Arria 10 SoC. **Figure 2** shows various components of the ORU PCBA.

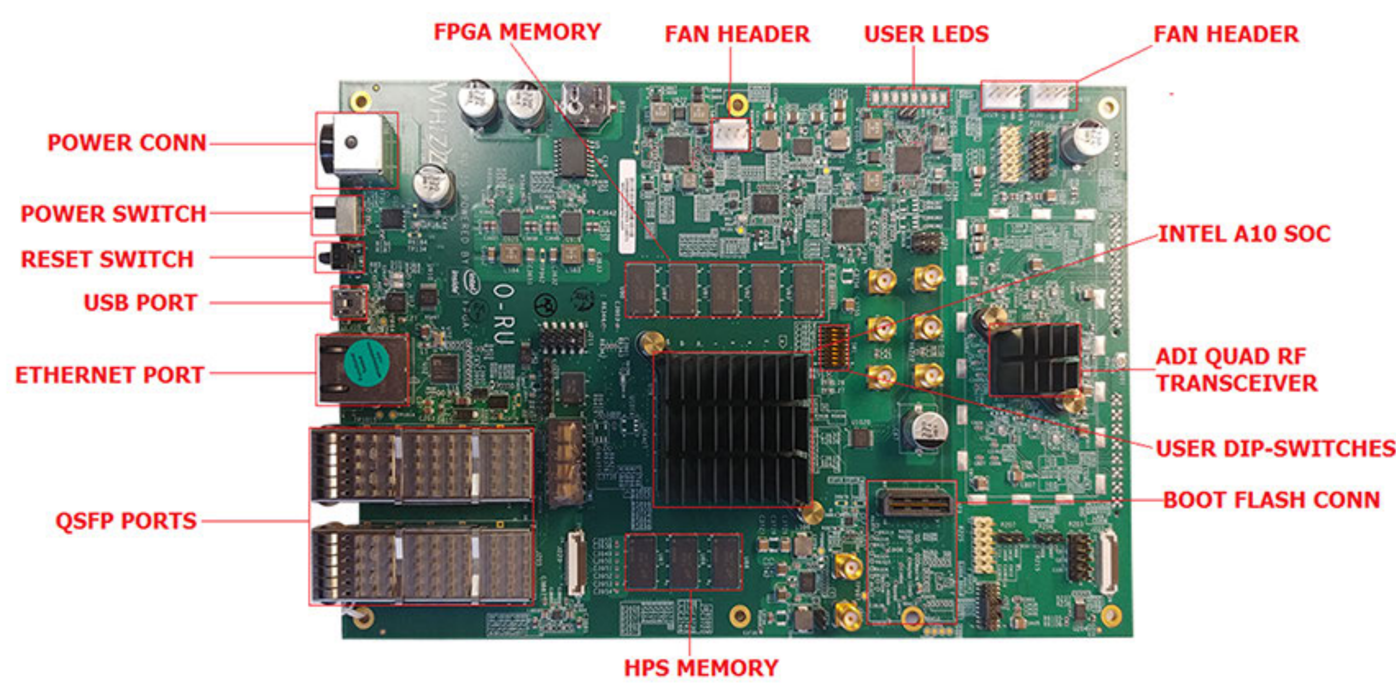


Figure 2. ORU PCBA.

PCB Layout

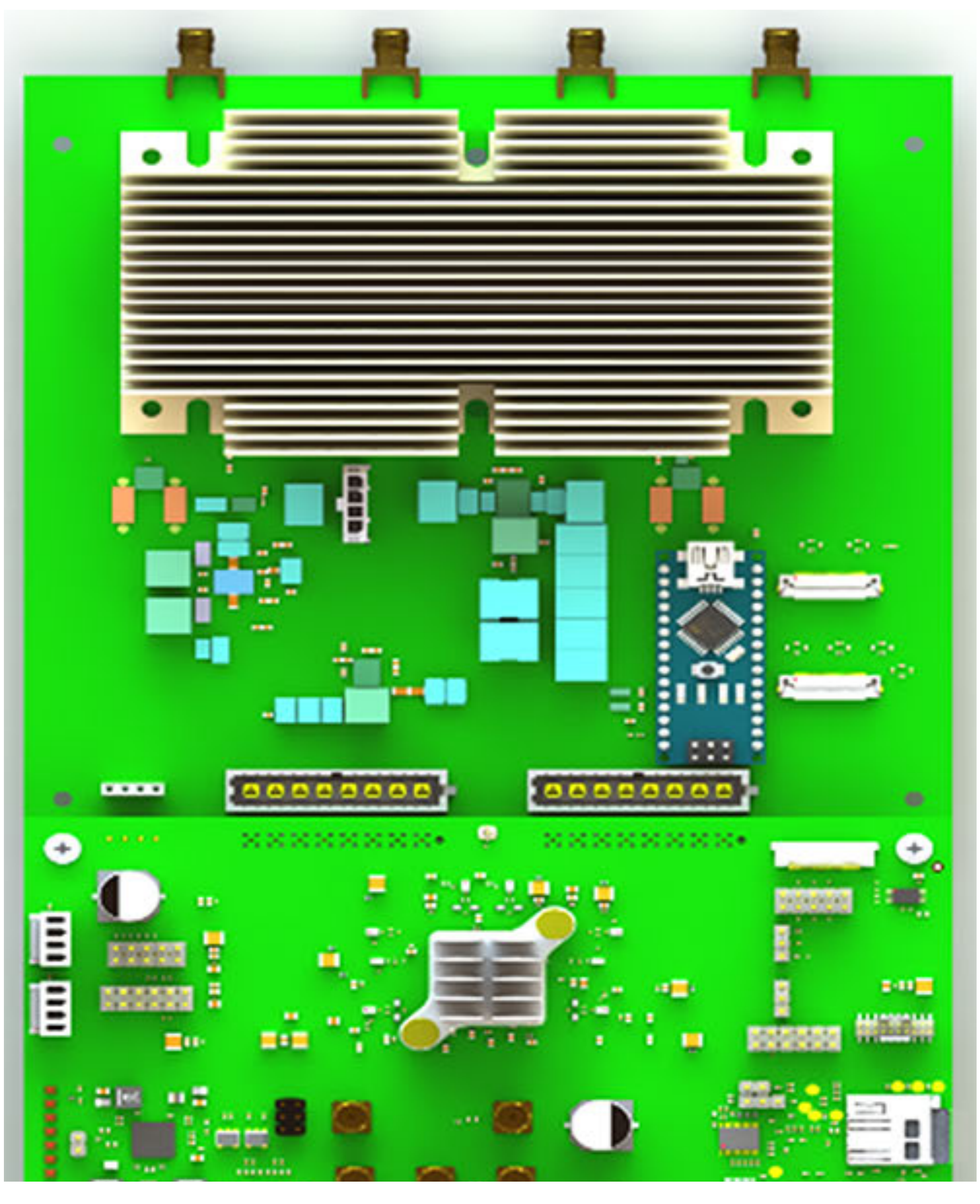
PCB layout is performed with consideration for electrical and mechanical constraints for the application of the unit. The dielectric material is Isola 408HR, chosen because it's cost-effective and simulation/lab results of insertion loss are low enough for the required maximum signal speed.

Several layout techniques are used for improved performance. For example, backdrilling is adopted

to eliminate stubs, and separate analog/digital sections are employed to reduce noise and interference. Moreover, standard through-hole via technology is used to reduce cost.

Reference planes are taken into consideration while routing high-speed signal pairs. Fewer bends and optimized trace lengths are achieved to minimize signal losses, maintaining adequate space within traces and to all other features. Electrical rules checks (ERC) and design rules checks (DRC) are run to ensure all established constraints are met.

Layout iterations are made based on analysis feedback such as thermal simulation, enforced placement of power supplies and mechanical allowance for heat sinks. Connector placements and enclosure-related changes are driven by 3-D modeling of all subsystems. SI/PI simulation recommendations are implemented for verification of optimum board functionality. **Figure 3** shows the RFFE and ORU cards.



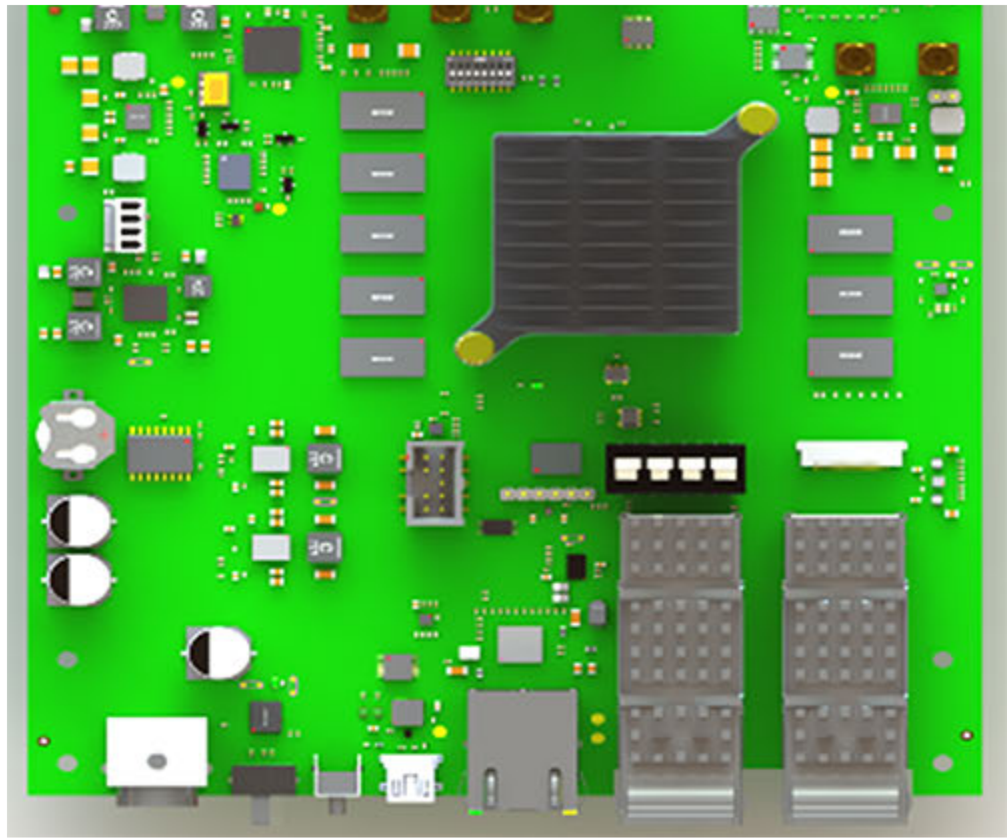


Figure 3. RFFE and ORU cards.

Among the challenges involved are making a special GND shield around ADI chip for RF signal isolation, FFC connector placement due to its connecting cable length constraint, power supply layout design due to complex copper pour shapes, implementation of special GSSG via pattern, and plane voids for high-speed signal integrity of QSFP signals.

SI/PI Simulations

Multiple simulations are run to optimize functionality and performance of each interface, minimizing chances of design revision.

Stackup is calculated by selecting the dielectric material type required to meet the signaling performance requirements. Prepreg/copper thickness as well as the number of signal layers/GND /power planes are carefully set up to meet the design requirements and maintain cost-effectiveness. Trace width calculations are performed to meet impedance requirements.

Parametric via optimization simulation is also performed to design an impedance-controlled via for minimizing signal losses **(Figure 4)**.

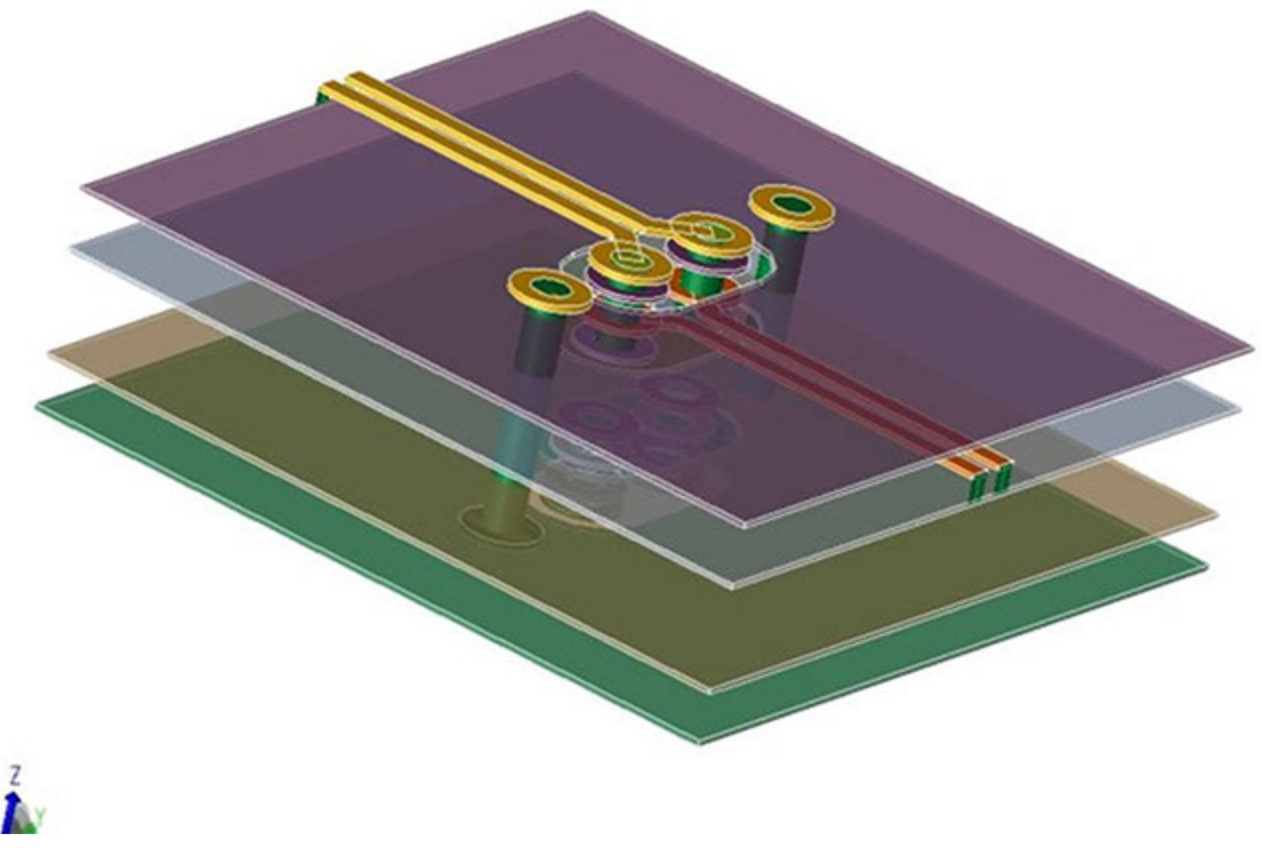
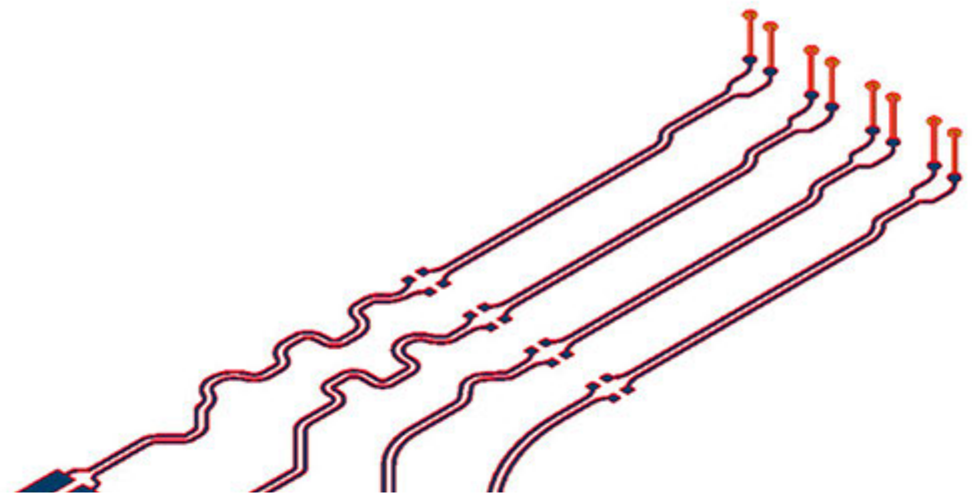


Figure 4. 3-D via structure for design optimization.

Critical high-speed signal design rules like maximum allowed trace length are defined through several pre-layout simulations. This is the key to first time success of this design. The via stub is minimized by back-drilling to reduce return loss and improve signal quality of the high-speed differential pairs **(Figure 5)**. To validate the routing rules, insertion and return loss measurements as well as serial link simulations are performed for the QSFP signals which produce eye diagrams **(Figure 6)**.



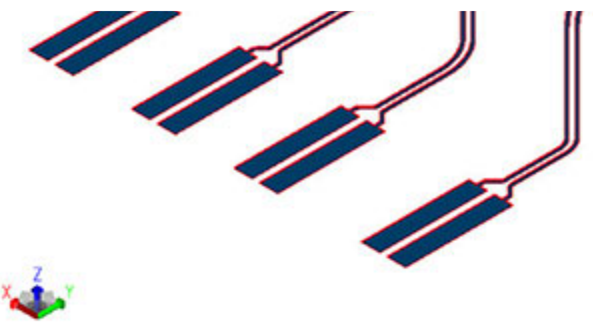


Figure 5. 3-D view of high-speed routing.

The DDR interface is demanding in terms of signal integrity and timing requirements. To ensure the DDR interface functions properly, pre-layout simulations are run to determine routing topology and set delay matching rules. The termination resistor value selected minimizes ringing, noise and reflection. Post-layout simulation is done to get eye, wave and timing/mask results for verification that the signals are matched within required timing with less ringing and maximum eye-aperture widths.

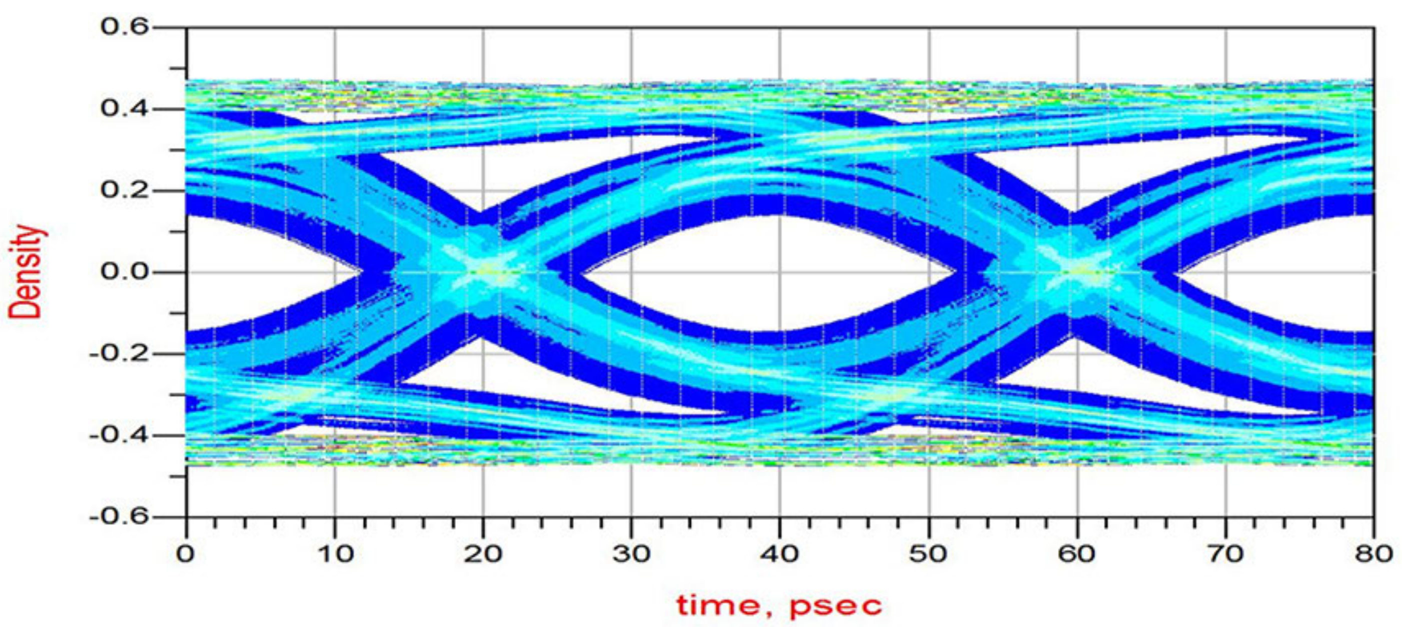


Figure 6. Eye diagram results of serial link simulation.

Power is one of the main challenges faced in designing this board. Power AC simulation is done to optimize the power delivery network and reduce the cost of decoupling/bypass capacitors.

Power DC simulation is run to ensure that the IR drop is within acceptable limits for this design.

Care is taken while selecting ferrite beads, inductor or supply regulators for critical power rails to minimize IR drop and thermal heating issues. To ensure the PDN circuit will work effectively, IR drop, via current, plane current density, and Joule heat thermal simulations are performed on all power rails. **Figure 7** shows IR drop simulation results.

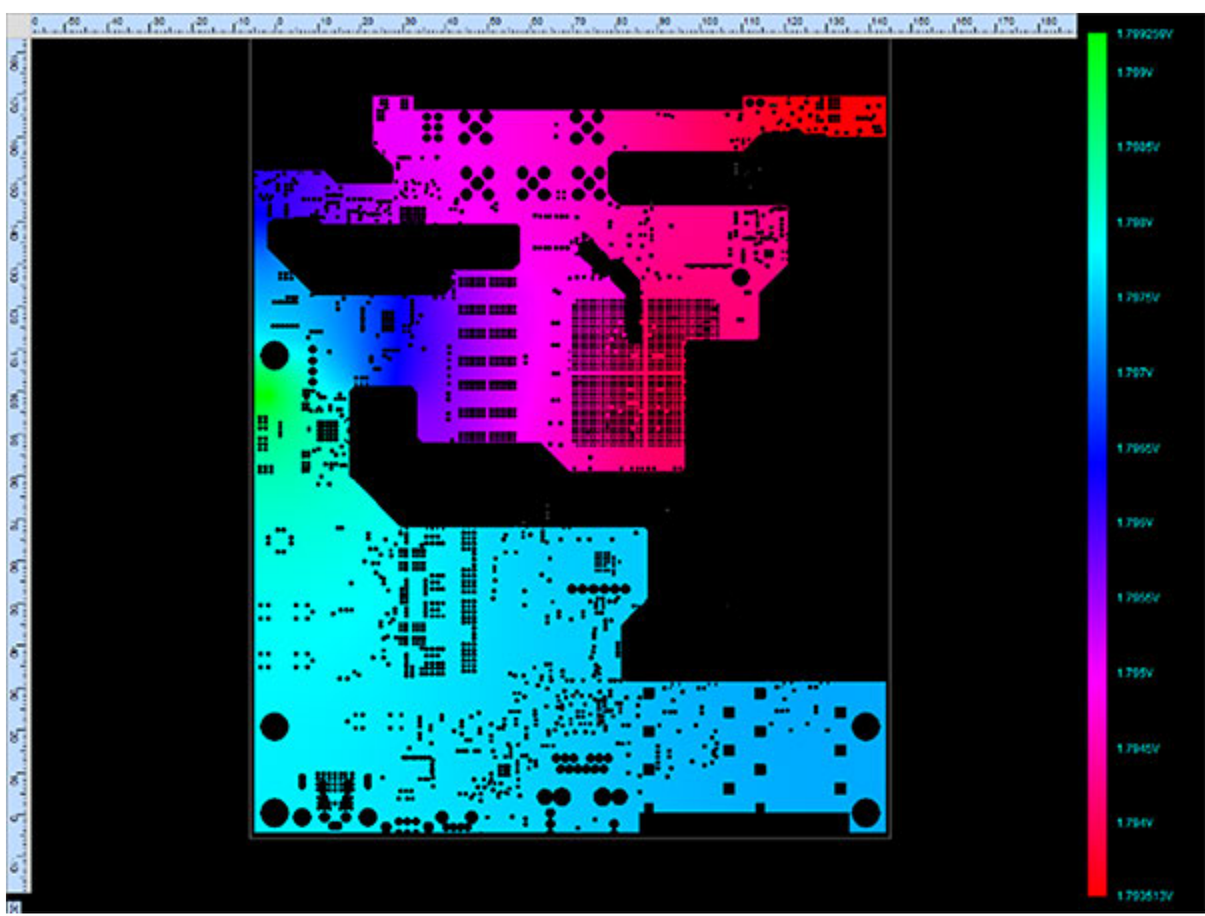


Figure 7. Power DC analysis results.

Mechanical Enclosure

The mechanical board and enclosure size are designed optimally to meet the overall product design constraints and requirements. The ORU card size is 9 x 6 x 1.5″; the adapter card is 6.5 x 6 x 0.5″ and the RFFE card is 6.4 x 6 x 1.2″. The overall enclosure size specifications are 14.9 x 8 x 2.6″ **(Figure 8)**.

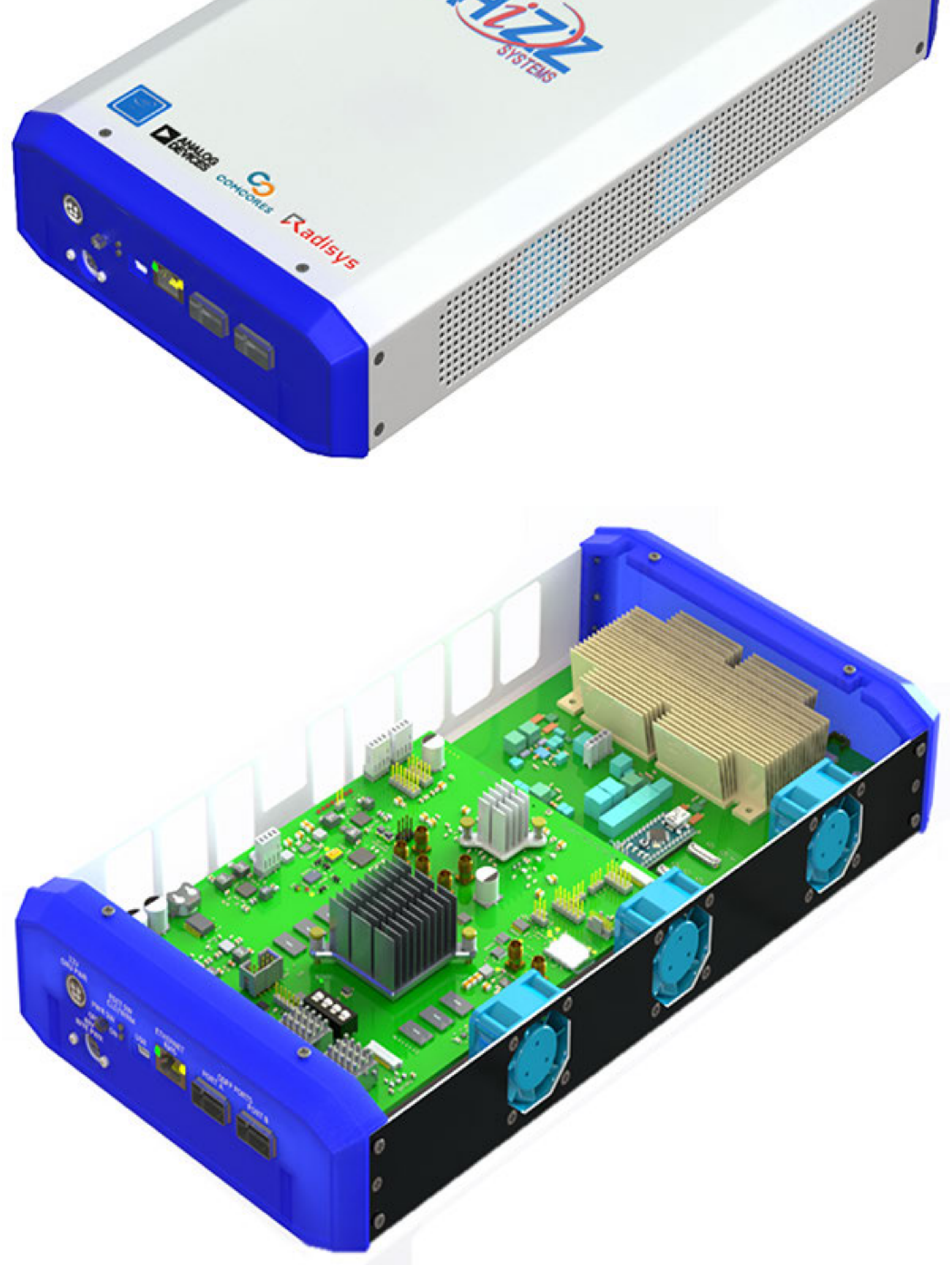


Figure 8. ORU enclosure.

Sheet metal for the enclosure is aluminum alloy, which is lighter and easier to manufacture compared to options such as low-carbon steel. Encapsulations are ABS plastic, which is inexpensive, lightweight, shock-absorbent, and durable.

Off-the-shelf hardware selection is generally preferred for mechanical assembly for lower cost and simplification. This includes washers, screws, standoffs, and other mechanical components.

Several enclosure joining mechanisms like sliding, top/bottom joining, etc., are used, but mating of covers with screws is preferred, in consideration of the application of the unit. Chassis shape design underwent several revisions for contour changes to lower the cost while retaining aesthetic appeal.

Thermal Analysis

ORU and RFFE cards are thermally simulated to determine critical components temperature and heat flow under certain power loads and ambient conditions. The objective is the critical component temperatures must not exceed the rated maximum temperature range.

The unit is thermal compliant for system-level (inside the enclosure) as well as module-level (the standalone PCB), verified using a CTM (compact thermal model).

Different configurations are applied for both the ORU and RFEE cards. Connectors and heighted components in the ORU are positioned to ensure no airflow blockers, and that temperatures are within the allowed range. Heat sinks are selected according to major heat-dissipated components. As the RFFE is designed after ORU, configurations for the RFFE are optimized for a new fan with more airflow but the same position.

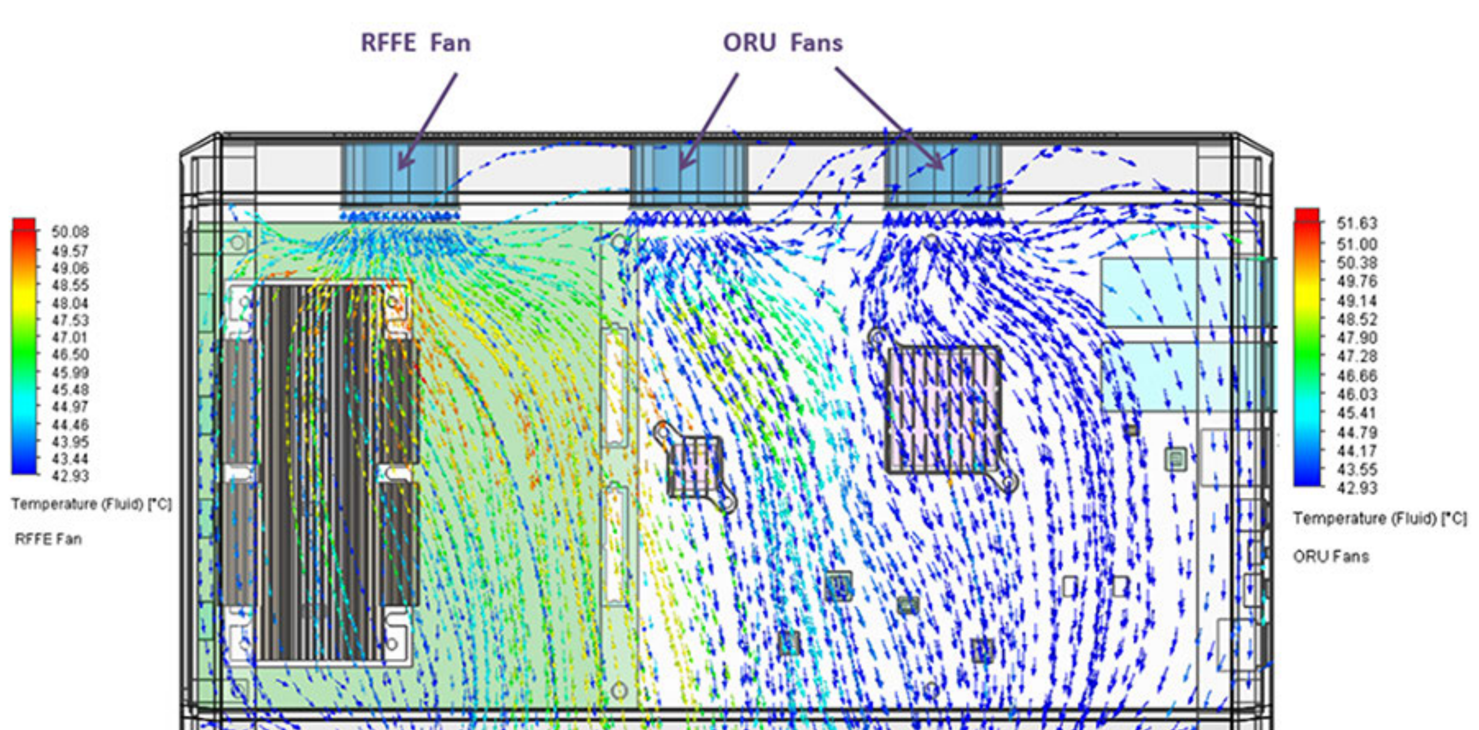


Figure 9. Thermal analysis results.

As a result, all thermal model simulation results are PASS based on selected thermal solutions of heat sinks and fans with better air flow but less pressure noise **(Figure 9)**.

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MUHAMMAD IRFAN is founder and CEO at Whizz Systems; mirfan@whizzsystems.com.

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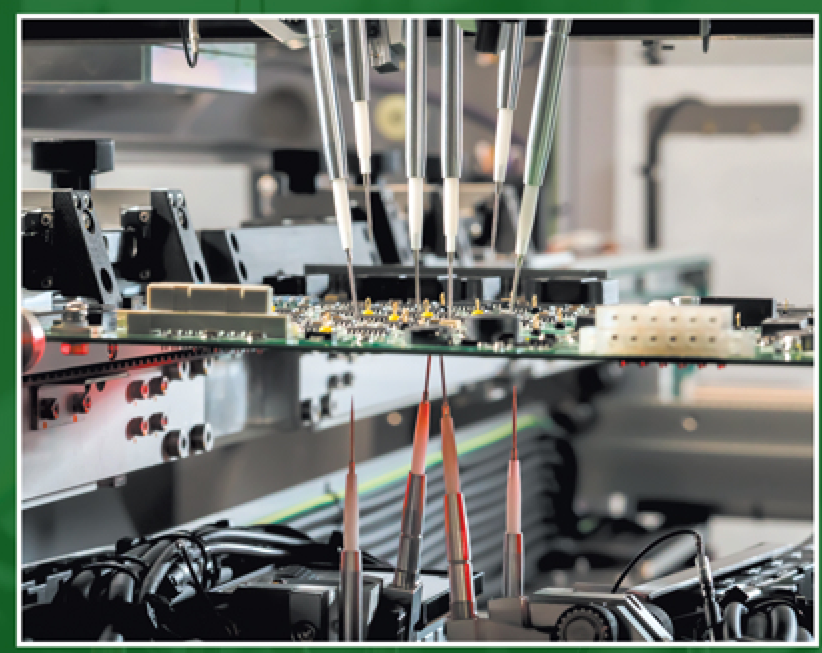

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GETTING **LEAN**

In-House Fixture Fabrication

Leveraging additive manufacturing technology to mistake-proof production.

ONE THING OEMS universally agree on is that none of them likes non-recurring engineering (NRE) charges. Implemented as part of new product introduction (NPI), however, custom tooling, fixtures and jigs can eliminate defect opportunities by minimizing process variation that could otherwise occur when those issues can't be resolved through product design changes. They are also a good tool when a production team identifies the need for a poka-yoke, or mistake-proofing solution, later in a product's lifecycle.

The concept of poka-yoke was developed by Shigeo Shingo as part of the Toyota Production System (TPS). When applied, the resulting process improvement eliminates a specific defect. Its focus on simplicity is its strength, in that simple fixes are often the best solution for small variances in the manufacturing process. Simple fixes are also easy to rapidly implement and encourage production operator involvement in the pursuit of product perfection. That said, when fixtures are procured through third parties, the cost may exceed the benefit.

The Lean Six Sigma team at SigmaTron International's facility in Tijuana, Mexico, decided to investigate ways to reduce tooling-related NRE costs by developing in-house 3-D printing and computer numerically controlled (CNC) machining capability. In 2022, they initiated a DMAIC (define, measure, analyze, improve and control) effort to determine necessary equipment and the likely return on investment if the capability was added.

The facility now has two 3-D printers, two CNC-controlled routers and the software tools

necessary to design and fabricate a range of fixtures. In the first seven months of 2023, designing and fabricating fixtures internally has generated cost savings of almost 200% over the costs had the fixtures been purchased from external suppliers.

In addition to lowering tooling-related NRE costs as programs are ramping up, the lower cost of this in-house capability has made it possible to expand use of specialized tooling for poka-yokes identified in Kaizen events. Improvement opportunities are identified by Lean Six Sigma-trained personnel in regular Gemba walks through the production area. The facility's Industry 4.0 AOI inspection capability, which covers both SMT and secondary assembly operations, is also helping rapidly identify quality trends where a poka-yoke fixture solution would eliminate a defect opportunity.

In one case, an overlay was created to cover an unused plugged via on a printed circuit board assembly (PCBA) used in a harness assembly. Production operators soldering the harness to PCBA were confused by the via because it looked similar to pads for the harness attachment and was in the same area of the PCB. Once the overlay covered the via, yield improved from 95% to 100% on the product. The annual return on investment exceeded the cost of the overlay by over $3,000.

In another case, wave soldering had become a production bottleneck due to a shortage of fixtures used to stabilize a capacitor on PCBA. Lower cost in-house fixturing capability enabled the team to add 20 additional fixtures. Waiting takt time per assembly dropped to 1 min from 10 min. The annual return on investment exceeded the total cost of the fixtures by nearly $1,500.

In a different example, a manually inserted connector needed to be pressed into a socket on the PCBA. Manual pressure increased the risk of damage and had a 5 min. takt time. Internally designed and fabricated small press tools controlled the pressure, eliminating the damage risk. Takt time on the operation dropped to 30 sec. The annual return on investment exceeded the cost of the presses by over $2,500.

In addition to quality, cost and efficiency improvements, moving to an in-house fabrication option has given the team better control of the tooling design and reduced tooling fabrication lead time. The fixtures are utilized in a variety of operations including manual insertion, wave solder, AOI, SMT, test, secondary assembly and box-build.

The Lean Six Sigma team is now evaluating ways to better automate the tooling fabrication process, to further shrink lead time and cost.

FILEMON SAGRERO is continuous improvement engineer at SigmaTron International (sigmatronintl.com) and a Six Sigma Black Belt; filemon.sagrero@sigmatronintl.com.

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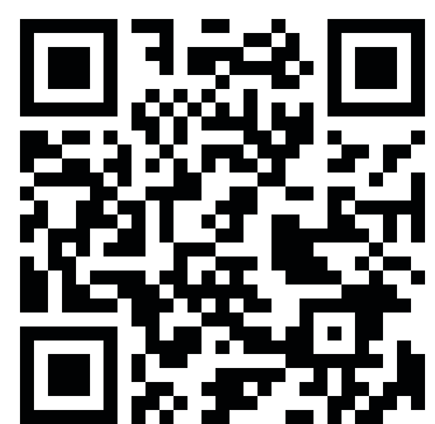

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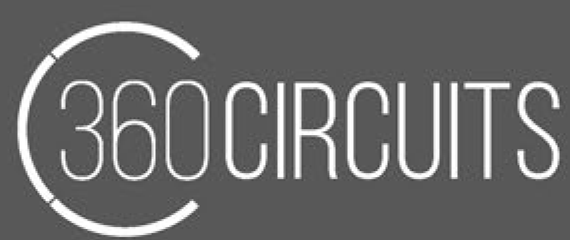

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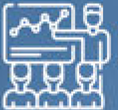
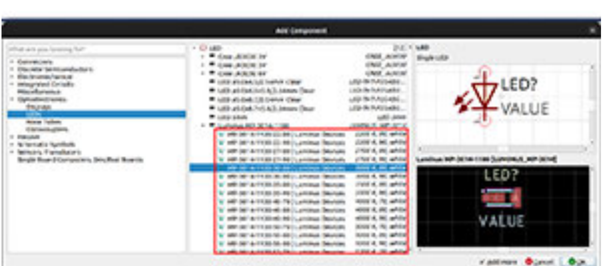
Industry Consulting 

Photorealistic Imagery, Animations and Interactive Media

ALTAIR HYPERWORKS 2023 CAE

HyperWorks 2023 introduces platform-wide enhancements, including a new user experience, faster speeds, an open and programmable architecture, and AI-powered workflows. Allows developers and users to integrate solutions seamlessly, maximizing the platform's technological potential. All solver solutions – Altair OptiStruct, Altair SimSolid, Altair Feko and others – have also added significant new capabilities. Altair Simulation Cloud Suite allows simulation data management, and Altair HyperMesh CFD features a particular focus on external aerodynamics.

Altair
altair.com



LIBREPCB DESIGN SOFTWARE VER. 1.0

LibrePCB Ver. 1.0 includes new features such as a 3-D viewer and export format for working with designs in a mechanical CAD tool, support for manufacturer part number (MFN) management, and simplified exporting of production data. Also includes new board editor features such as thermal relief pads in planes, blind and buried vias, keepout zones, custom footprint pad shapes, and more.

LibrePCB

librepcb.org

MOLEX KICKSTART CONNECTOR SYSTEM

KickStart OCP-compliant connector system combines low- and high-speed signals, as well as power circuits, into a single cable assembly. Eliminates need for multiple components, optimizes space and accelerates upgrades by offering server and device manufacturers a flexible, standardized and easy-to-implement approach for boot-drive peripheral connections. Features a standardized Small Form Factor TA-1036 cable assembly that complies with OCP's Data Center Modular Hardware System (DC-MHS) specification, and is recommended in OCP's M-PIC specification for cable-optimized, boot-peripheral connectors. Accommodates PCIe Gen 5 signal speeds, with data transfer rates up to 32Gbps NRZ, and includes planned support for PCIe Gen 6. Offers a lowest mated profile height of 11.1mm for improved space optimization, increased airflow management and reduced interference with other components, and also allows simple, hybrid cable assembly pinout from KickStart connectors to Sliver 1C for Enterprise and Data Center Standard Form Factor (EDSFF) hard-drive docking.

Molex

molex.com

PETERS ELPEJET IJ 2467 SOLDER RESIST

Elpejet IJ 246 is a crack-resistant inkjet solder resist. Is solvent-free and is said to be precise, for selective control coverage on PCBs to save resources and increase reliability. Allows individual marking of PCBs, e.g., by a QR code, so that each individual PCB can be identified and traced reliably.

Peters

peters.de

SABIC LNP THERMOCOMP WF006V

LNP Thermocomp WF006V compound is designed for laser direct structuring (LDS) of antennas that are integrated into the housings and covers of consumer electronics devices, appliances and other electronic components. Is said to provide a tensile modulus more than two times higher than that of unfilled polybutylene terephthalate (PBT) or polycarbonate (PC) resin, and can be used for molding small, thin-wall parts. Delivers good surface quality to meet aesthetic requirements, and offers good signal gain and LDS performance. Provides improved chemical resistance, hydrolytic stability and lower warpage compared to traditional materials. Also features good impact resistance and laser welding capability.

Sabic

sabic.com

SATURN PCB DESIGN TOOLKIT V. 8.33

PCB Toolkit V8.33 features updates and additions from previous versions. Corrects images in the Help PDF file, and adds an MSI image file to the website for silent installs.

Saturn PCB Design

saturnpcb.com

ULTRA LIBRARIAN AI-DRIVEN CAD ENGINE

AI-driven CAD modeling engine is designed to drastically reduce the time it takes to build CAD models. Leverages extensive Ultra Librarian expertise to automate CAD model creation. Has been trained on library of over 16 million CAD models currently available through Ultra Librarian, which has allowed for tuning to handle myriad variations and differences that exist between vendors’ part data. Available as free beta in early 2024.

Ultra Librarian

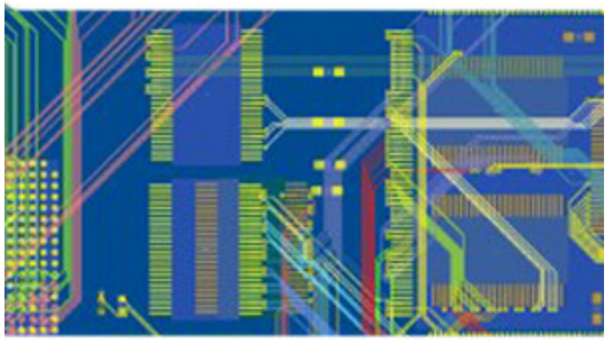
ultralibrarian.com

WÜRTH ELEKTRONIK USB 3.1 SMT CONNECTOR

USB 3.1 Type-C High-Rise SMT connector is a 24-pin fully configured horizontal receptacle for SMT assembly. Allows complete visual control of soldering thanks to two rows, each with 12 contacts. Is compatible with USB 3.2 Gen 1×2 signaling and USB power delivery standards, and can be used for alternative and accessory modes, including transmitting analog signals via the (D+/D-) pins. Is designed for at least 10,000 mating cycles and operating temperatures from -40° to +120°C. Pin contacts and outer retaining pins of the shielding are gold-plated in the contact zone to ensure connection to PCB. Stable receptacle is suitable for all consumer and IT applications.

Würth Elektronik

we-online.com



ZUKEN E3.SERIES 2023

2023 release of E3.series design platform includes enhancements in 3-D functionality for control panel design, circuit diagram generation, and an improved user experience. Enhancements to 3-D functionality include the ability to arrange and edit elements such as mounting panels at any angle, and an enhancement to the 2-D view of the elements to allow the creation of multiple directly linked 2-D views. Automates correct stop part selection from a group of parts provided by a chosen manufacturer with the enhancement of cross-section checks for stop parts and component connection points. Cross-reference text for cable duct inlets/outlets is now available to jump to and from quickly, and cross-reference texts are also active links with the PDF export.

3-D enhancements in E3.series, E3.3DTransformer, and E3.formboard allow import of 3-D geometries from mechanical CAD systems in a single operation, and 3-D geometric cable routes from industry-standard MCAD tools are converted into the 2-D views required to create manufacturing documents for harness assembly. Supplements views in E3.formboard with the necessary electrical information, such as connector pins and assignments, conduit protection elements, and dimensioning, and users can also directly import harness description formats into E3.series such as Harness XML files, KBL files, and PLMXML files. Also features ability to rename conductors of database cables within the project.

Ease-of-use features include extended access and modification options for device properties, dimensions, and part attributes, and an extension of the cross-section checks for connectors and devices by introducing a new option to check that the wire or conductor outer diameter is valid when selecting the appropriate wire ferrules or pin terminals for the cavity. Also includes an additional check to aid with automating part selection. Simplifies inclusion of images in a project, allowing users to paste graphics and pictures from the Windows clipboard directly onto an E3.series sheet.

Zuken
zuken.com

CA

BOWMAN K SERIES BENCHTOP XRF

K Series benchtop XRF features an expansive measurement area, selectable spot sizes, and high levels of both precision and speed. Has a 12"x 12" measurable area for parts up to 9" tall and selectable spot sizes accommodate a wide range of features; focal distances from 0.25" to 3.5". Has cantilever door design for easy access, and servo motor-driven programmable stage streamlines sample positioning. Also includes table-view functionality to image the entire measurable area and allow the operator to navigate to any location with a single click.

Bowman

bowmanxrf.com

BTU AURORA 200N REFLOW OVEN

Aurora 200N convection reflow oven has closed-loop convection control, and 200" of heat to support faster line speeds up to 25% faster than those supported by Aurora 150N. Includes modern conveyor options, flexible heating and cooling configurations, an updated user interface, integrated Aqua Scrub flux management technology, Smart Power energy savings software, and advanced process control technologies. Unit can be shipped in two pieces.

BTU International

btu.com

COUNT ON TOOLS CUSTOM FUJI NXT H02 NOZZLE

Custom Fuji NXT H02 nozzle is designed specifically for the placement of Panasonic AYC2F automotive board-to-board connectors. Crafted to ensure a seamless fit and reliable performance during the assembly process, and meets the stringent requirements of the automotive industry.

Count on Tools

cotinc.com

EMIL OTTO ROL0 FLUX PASTE

EO-FP-003 is a ROL0 flux paste developed for repair work on printed circuit boards and for applications according to IPC-A-610. Can be used for repair work in highly-stressed assemblies, and can activate contaminated pads and component pins. Can be used in small quantities due to good activation properties, and is processable via hot air and soldering irons or mini wave.

Emil Otto

emilotto.de

IDENTCO VORTEXID WIRE MARKING SYSTEM

VortexID wire label system can place up to 20 labels per minute and operate 24/7. Handles a variety of American wire gauge sizes, making it suitable for a broad array of sectors whose products incorporate wires and harnesses – particularly automotive and electronics components manufacturing. Offers high-resolution, 300dpi printing capabilities, with labels applied via a vacuum plate whose rotating mechanism is said to ensure reliable application to cylindrical products. Is materials-agnostic, and applies self-laminating and flag labels.

Identco

identco.com

MASTER BOND EP21LVFL EPOXY

EP21LVFL two-part epoxy is said to combine flexibility with a solid strength profile. Curable at room temperature with a long working life of 120-160 min. at 75°F for a 100g batch and features a flowable initial mixed viscosity of 10,000-14,000cps. Generates low exotherm making it suitable not only for bonding and coating, but also for sealing and potting applications. Is said to be useful in bonding substrates with different coefficients of expansion such as metals, composites, glass, ceramics, rubbers and plastics. Has an elongation of 120-150%, tensile modulus of 1,500-2,500psi and shore D hardness of 40-50. Features a volume resistivity exceeding 10^{15}ohm-cm and a Dk of 2.95 at 60Hz. Tensile strength is 1,200-1,400psi and lap shear strength measures 900-1,100psi. Withstands rigorous thermal cycling, vibration, mechanical stress and shock. Offers a noncritical one-to-two mix ratio, by weight or volume. Part A is clear and Part B is amber clear, and can be formulated in other colors. Cures more rapidly at elevated temperatures, with optimal performance properties achieved by curing overnight at room temperature followed by 4-6 hrs. at 125°-150°F.

Master Bond

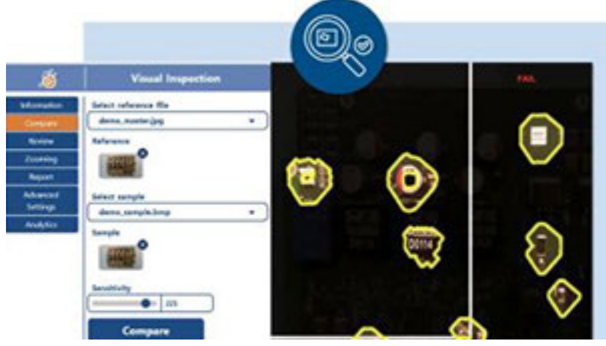
masterbond.com

MASTER BOND SUPREME 17HTND-2 EPOXY

Supreme 17HTND-2 is a toughened epoxy system for bonding and sealing applications. Is a true one-component system, not premixed and frozen, and is said to have unlimited working life at room temperature. Is thermally stable, featuring a glass transition temperature (Tg) of 410°F (210°C). Meets NASA low outgassing specifications per ASTM E595 testing. Volume resistivity exceeds 10^{15}ohm-cm at 75°F. Lap shear strength is 1,900-2,100psi and tensile strength is 7,000-8,000psi. Is designed to withstand thermal cycling and offers service temperature range from -100° to 550°F (-73° to 288°C). Along with simple handling properties, has a paste consistency and is completely non-drip, for applications where no flow is critical. Cures at elevated temperatures with cure schedule options including 300°F for 4-6 hr. or 350°F for 2-4 hr. Optimal cure schedule is at 300°F for 4-6 hr., followed by post-cure at 350°F for 8-12 hr. Bonds to variety of substrates including metal, ceramics, composites and several plastics. Black in color, comes in standard packaging of jars and cans, ranging from half-pint to gallon containers.

Master Bond

masterbond.com

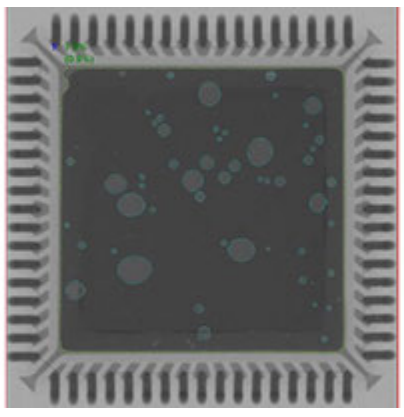


PLEORA VAIRA MANUFACTURING PLATFORM

Vaira manufacturing platform now includes a scalable suite of shop-floor ready AI and digitization apps to help manufacturers automate and upgrade error-prone processes. Now includes AI-based object detection and classification skills that can be integrated with assembly checklist and work instructions, and are said to reduce final verification steps from over 4 min. to 30 sec. Allows an operator to follow digitized instructions that clearly guide product assembly step-by-step, while AI and machine vision automatically verifies quality. Product tracker app capabilities enable product images and operator notes to be captured and stored to a manufacturer's ERP/MES system for compliance, traceability, and continuous improvement initiatives.

Pleora Technologies

pleora.com



SHENMAO PF606-P276 SOLDER PASTE

PF606-P276 is an ultra-low void no-clean zero-halogen lead-free solder paste. Offers superior void performance achieved through special activators, and is halogen-free (ROL0) and fully compliant with international environmental standards like RoHS, RoHS 2.0, and REACH. Is said to excel in solderability, ensuring flawless connections in SMT processes, and features remarkable wettability characteristics to guarantee a uniform soldering process and a design for high-speed printing that optimizes production efficiency. Also features superior solder joint strength and product performance that consistently surpasses expectations. Excels in minimizing gas generation during the reflow process, achieving a void ratio of less than 10% in critical components like MOS and QFN.

Shenmao America

shenmao.com

SOLDERSTAR REFLOW SHUTTLE O2 MEASUREMENT MODULE

Reflow Shuttle O2 measurement module is a repeatable verification tool that combines O2ppm, vibration levels in three axes, vacuum, temperature profiles, and conveyor speed on a single platform. Offers real-time control over oxygen content to aid in the elimination of oxidation issues that could impact soldering quality. Detection nitrogen leaks throughout oven zones and pinpoints oxygen fluctuations. Reportedly seamlessly integrates into a fully operational reflow oven, eliminating downtime during verification. With a button press, initiates data collection, providing a comprehensive pass-through graph of the entire oven, complete with insights into anomalies at the outset of the process, facilitating rapid adjustments if necessary. Custom battery pack enables multiple passes across various production lines before recharging is required. Smartlink connector provides quick connections to SLX datalogger. Auto-configured without computer setup, for both initial setup and daily process checks on production floors.

Solderstar

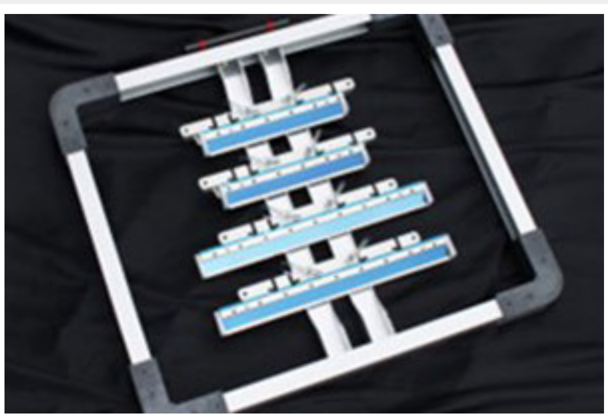
solderstar.com

TRANSITION AUTOMATION PASTE RETAINER SYSTEM

Soft-Touch Paste Retainer system now features dual pin locking that better secures the white dam portion. Attachment screws have also been upgraded to alloy steel compared to the previous galvanized steel, and the spring element has been made thicker to give the design more impact resistance. Total part count was reduced by eight pieces per set. White dam may be adjusted in or out based on the position of the squeegee blade, and the entire assembly can be adjusted up or down to push against the stencil or to ride above it slightly. Users can receive a no-charge update for the next three months.

Transition Automation

metalsqueegees.com



TRANSITION AUTOMATION SQUEEGEE BUDDY

Squeegee Buddy is a new tool for SMT printer users to help improve process quality and organization. Provides a secure storage for squeegees in the form of a frame that looks similar to a stencil frame, meaning it can be inserted into stencil cleaners to clean squeegees without damaging them. Is capable of use for both squeegee storage and squeegee cleaning, and protects the squeegees from damage by keeping them within the outside dimensions of the frame. Can be hung on a wall or inserted into a stencil frame rack to store the squeegees between operations. Can be used with any Transition Universal Holder with the addition of two small holes that allow the squeegee to be inserted onto two secure pins.

Transition Automation

metalsqueegees.com

TRI TR7600 SV SERIES 3-D AXI

TR7600 SV Series 3-D AXI outperforms its predecessor, the TR7600 Series, by a 20% increase in performance. Features 7μm resolution and is equipped with AI algorithms, which are said to be superior to the commonly used gray-level-based algorithms and can accurately detect void defects. Supports current Smart Factory Standards, including the IPC-CFX, IPC-DPMX, and The Hermes Standard (IPC-HERMES-9852).

Test Research, Inc.

tri.com

ULT LRA 400.1 FUME EXTRACTOR

LRA 400.1 soldering fume extractor is a modular and quiet fume extractor that can be used in manual and automated soldering processes. Features a newly developed and unique filter inflow concept that enables increased filter capacity, plus an EC dual blower that can achieve high-volume flow at high vacuum, for laser and soldering applications.

ULT

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In Case You Missed It

Soldering

"Modeling the Effects of Thermal Pad Voiding on Quad Flatpack No-Lead (QFN) Components"

Authors: Ross Wilcoxon, *et. al.*

Abstract: Finite element modeling was used to evaluate the effects of thermal pad solder voiding on the thermal resistance of quad flatpack no-lead components. This included two different approaches for modeling solder voids: many small, distributed voids, the effects of which were averaged across the entire solder contact area, or a single discrete void. Two approaches were used for defining the thermal path established in the solder. Effects of other design parameters – thermal boundary conditions, the presence of thermal vias under the package, and the size of the die power dissipation area – were also addressed. Modeling showed that thermal vias and external boundary conditions had the most significant impact on the package thermal resistance. Solder pad voids and concentrated die-level heat dissipation, for the range used in this study, had noticeable but less significant impacts on thermal resistance. The study also compared different approaches for simulating solder voiding and identified ranges in which modeling simulations are most appropriate. (*Journal of Surface Mount Technology,* July 2023, https://doi.org/10.37665/smt.v36i2.37)

Surface Finishes

"Development of Cost-Effective Ni-Less Surface Finishing Process for High-Speed PCBs"

Authors: Jaeseong Park, *et. al.*

Abstract: The growing need to use low-power and high-frequency signals for the high-speed transmission of large-capacity data is driving the demand for suitable printed circuit boards. Most printed circuit boards use Cu as a conducting material and require a surface finish that forms an organic or a metallic protective layer on the Cu surface to prevent Cu diffusion/oxidation. Metallic protective layers typically have a higher resistivity than Cu, resulting in significant signal transmission losses in the high-frequency range. For example, electroless Ni/electroless Pd/immersion Au (ENEPIG), a surface finish that forms a metallic protective layer, sequentially forms Ni-P, Pd-P, and Au layers on a Cu surface. Among these, the Ni-P layer is the main cause of signal transmission loss owing to its high resistivity. In this study, the authors developed immersion Ag/immersion Pd/immersion Au (ISIPIG), a cost-effective surface finishing process that does not form a Ni-P layer. ISIPIG effectively prevented the diffusion/oxidation of Cu and improved solder wettability while exhibiting a lower insertion loss and higher antenna efficiency than ENEPIG. The authors' results suggest that ISIPIG is a promising surface finishing process for applications that require the high-speed transmission of large-capacity data using low-power and high-frequency signals. (*Journal of Electronic Materials,* August 2023, https://doi.org/10.1007/s11664-023-10616-2)

Sustainability

"Recycling And Sustainable Applications of Waste Printed Circuit Board in Concrete Application and Validation Using Response Surface Methodology"

Authors: M. Vishnu Priyan, *et. al.*

Abstract: The present investigation aims to examine the mechanical and durability properties of concrete that has been reinforced with a waste printed circuit board (WPCB) toward a low-carbon-built environment. It assessed the fresh and hardened characteristics of the low-carbon concrete reinforced with WPCB fibers, after a curing period of seven and 28 days. The evaluation was done by quantifying slump, compressive strength, split tensile strength, flexural strength, sorptivity, rapid, and acid tests. It further analyzed 11 discrete concrete mixes with WPCB fibers at a weight percentage ranging from 1 to 5% in the cement mixture. The results indicate that incorporating WPCB fiber into concrete improves its mechanical strength. The results revealed that incorporating 5% WPCB fiber yielded the most favorable outcomes. The properties of WPCB fiber-reinforced concrete have been theoretically validated through response surface methodology (RSM),

which employs various statistical and mathematical tools to analyze the experimental data. The results derived from RSM were compared with the experimental results. The RSM model demonstrated a high level of accuracy ($R2 \geq 0.98$) in validating the mechanical properties of WPCB fiber concrete. The statistical model exhibited no indication of prediction bias and demonstrated a statistically significant outcome, with a p-value below 0.5. (*Scientific Reports,* October 2023, https://doi.org/10.1038/s41598-023-43919-9)

Thermal Management

"Influence of a PCB Layout Design on the Efficiency of Heat Dissipation and Mutual Thermal Couplings between Transistors"

Authors: Krzysztof Górecki and Krzysztof Posobkiewicz

Abstract: This article presents results of investigations concerning the influence of the printed circuit board (PCB) layout design on self and transfer transient thermal impedances characterizing thermal phenomena occurring in the network containing two power Mosfets. The tested devices have the case D2PAK and are soldered to the PCB using surface mount technology (SMT). The measurement method is described. The tested transistors are presented with the PCBs on which they are mounted. Measurement results of the tested transistors operating on all tested PCBs are shown and discussed. The influence of a cooling area of the tested PCBs on the parameters describing self and transfer transient thermal impedances is analyzed. (*Electronics,* October 2023, https://doi.org/10.3390/electronics12194116)

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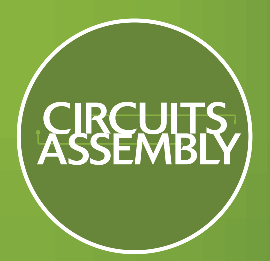

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