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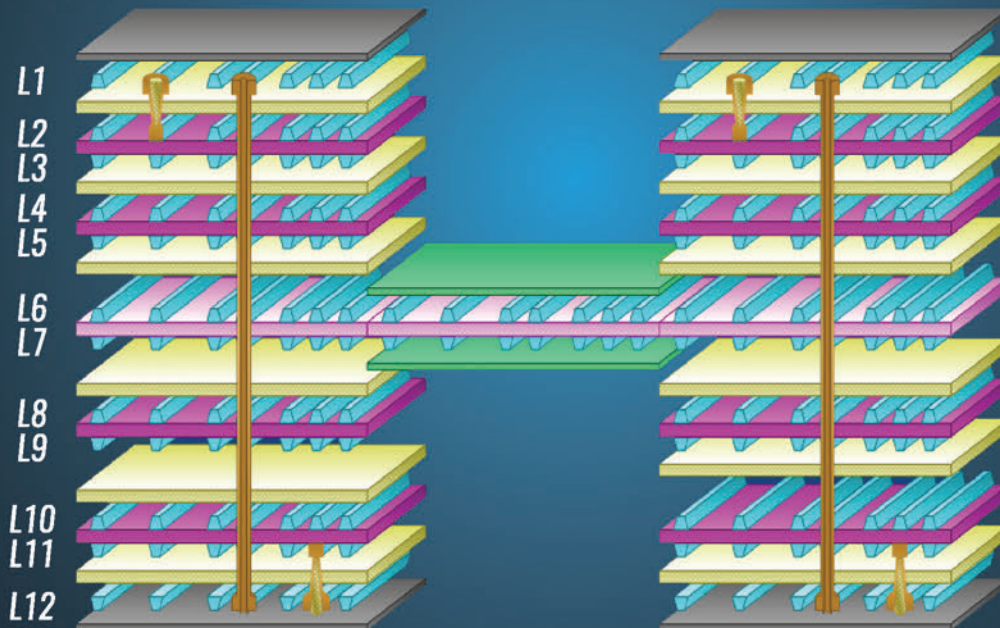


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TECHNICAL ABSTRACTS

DEPARTMENTS

AROUND THE WORLD

PCEA CURRENT EVENTS

MARKET WATCH

OFF THE SHELF

FEATURES

PCB DESIGN

How Many High-Current Vias Do We Need? (Fewer Than You Think)

Conventional wisdom has always been that the conducting cross-sectional area of the via should equal or exceed the conducting cross-sectional area of the trace, but this is not true. A look at a simulated board finds that the industry standard formula could actually triple the number of vias actually required.

by DOUGLAS BROOKS and DR. JOHANNES ADAM

IMPEDANCE (COVER STORY)

Why Making All Transmission Lines in a PCB 50Ω is Good Technological Practice

As many as seven different impedances are called out in various design specifications, and successfully designing a PCB with more than one of these impedances can near impossible. Designing with one impedance can greatly simplify PCB stackups and make other measurements easier.

by LEE RITCHEY

ADVOCACY

'A Good First Step'

With the recent announcements of several new PCB factories being built in the US, the Printed Circuit Board Association of America is looking to continue that momentum and advocate for further domestic production of PCBs and base materials. PCBAA executive director David Schild speaks about some of the latest legislative and industry developments.

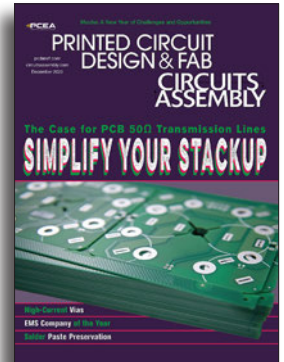
by MIKE BUETOW

EMS

Green Strength

An emphasis on speed – same day turns! – keeps Green Circuits' customers coming back. Inside the CIRCUITS ASSEMBLY EMS Company of the Year.

by MIKE BUETOW



ON PCB CHAT (PCBCHAT.COM)

ROBOTIC SOLDERING

with BOB WILLIS

PCB INDUSTRY LEGISLATION

with DAVID SCHILD

PCB DESIGN

with ROBERT FERENAC

PCB Chat

New Europlacer screen print platform: the foundation of greater productivity, connectivity and service support.

IT'S NO COINCIDENCE that Europlacer has received ten Service Excellence Awards in the screen printing category from Circuits Assembly (PCEA) magazine.

Those top accolades were based on the unmatched support infrastructure and exemplary customer service built around Europlacer's EP700 Series of fully automatic inline stencil printers. Incremental technology developments and productivity improvements throughout that period kept the EP700 and EP710 machines at the top of their game.

But now, Europlacer has raised the bar. The company launched its new ii-P7 screen print platform at Productronica 2023: a premium, state-of-the-art platform and the first machine of an entirely new generation. It is the latest addition to Europlacer's full-line solution portfolio.



The premium, state-of-the-art ii-P7 screen printer, the first machine of a new printer platform generation from Europlacer.

The robust dependability of Europlacer printers allowed the company's multi-award-winning support teams to leverage service delivery to levels unattainable by the competition. But with innovative smart features and advanced engineering technology built into the new ii-P7, those same accomplished teams can take Europlacer's service to new heights. It bodes well for the company's screen printer and full assembly line customers.



Improved productivity thanks to a quick-change cassette system for under-screen cleaning paper rolls.



Machine vision on the ii-P7 look-down camera evaluates the entire paste roll length to guard against insufficient paste volume before a print stroke.

Streamlined productivity & connectivity.

The ii-P7 majors on advanced productivity, ease of use and connectivity. Print cycle times are reduced by over 50% while one-third has been trimmed off under-screen cleaning times. A large 22-inch touchscreen monitor and upgraded Europlacer iiPS operating software improve the operator experience. As a core design goal, factory-wide connectivity is achieved via IPC-CFX and Hermes-compliant protocols.

But of equal importance to Europlacer customers is what's beneath the stylish ii-P7 exterior: critical precision-engineered enhancements designed from the ground up across the platform simplify maintenance and deliver even greater reliability. For instance, the ii-P7 needs no cooling fans. Service and support confidence is clearly demonstrated by Europlacer's industry-best 5-year warranty on spares and two years on labor.



Chris Merow, Director of Sales at Europlacer Americas, accepts two Service Excellence Awards from PCEA President Mike Buetow at SMTAi 2023.

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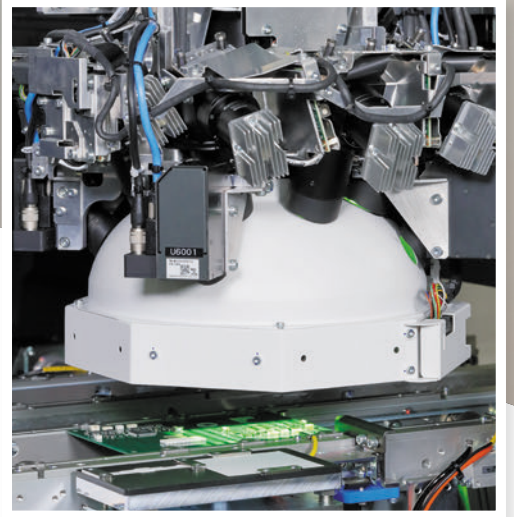
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Supply Chain Security Costs Money. Is Industry Willing to Pay?

IN NOVEMBER I was invited to join the “disruptors” of the industry – also known as Mark Goodwin and Gene Weiner – on a panel to discuss the derisking of the supply chain.

Against the backdrop of the biennial Productronica trade show, the largest of its kind for electronics manufacturing in the West, and hosted by my media colleague Trevor Galbraith, we attempted to delve into the issues at hand when it comes to ensuring supply chain resiliency.

As Goodwin, the chief operating officer of Ventec, correctly framed the situation, the vast majority of materials originate in Asia, particularly China, and while parts of the supply chain are being moved back to the West, a full-scale migration won't happen in our lifetimes. Given that, what needs to happen at the margins to ensure at least a minimal degree of secure chains?

The role of government naturally came up, and it was suggested that legislators are driving reverse migration. I pushed back on that notion, opining instead that commercial businesses lead the way and governments are reacting both to the years-long industry impetus and the post-Covid realization that supply chains are not secure. (For more on that, see [our interview with David Schild](#) of the Printed Circuit Board Association of America in this issue.)

If the problem that must be solved is the derisking of the supply chain, certainly government regulations and incentives can play a huge role. India, Thailand, Vietnam and, yes, China (remember them?) are prime examples of how quickly infrastructure can be established in areas that are open to investment. But what they also have in common are domestic policies that align with domestic goals.

In the West, by contrast, the heavy burden of patchwork environmental laws, credit availability, and

NIMBY-ism (not in my backyard) conspire to constrain even the most ardent supporters of PCB manufacturing. For a new plant to come online, permits are needed at every level from federal down to municipality. There's an inherent incongruity between the expressed desire at the federal or state level for more manufacturing as means to ensure product availability and a source of long-term careers and the near-un-navigable maze of local regulations and hostility many business owners experience when trying to expand. It's not by accident that the most recent board shops to be announced or come online are in mostly rural areas (New Hampshire, Idaho, upstate New York, Michigan) or very business-friendly states (Texas). Factories cannot be built where regulations effectively prohibit them.

Then there's the working capital issue. With dual stocks or multi-sourcing in place, more corporate funds will be tied up in inventory. Are we ready to reset our expectations for what working capital will look like when we have buffer stocks all over the world? That's a finance decision that has nothing to do with government but everything to do with Wall Street and banks and private equity and others who control the money trees.

Furthermore, the industry needs much greater visibility up and down the chain. I recall a conversation in the early 2000s with Viasystems' vice president of supply chain, who told me their goal was to see five layers in either direction; e.g., from the mines to the end-of-life recycler. Twenty years later, do companies have the right tools to manage an increasingly distended supply chain? Do those tools even exist? If the carbon and environmental costs of your product must be tracked in order to do business in a market – as legislation coming to Europe could require – will you be able to do so? (As an aside, the [Responsible Business Alliance](#) has developed a [Scope 3 GHG emissions reporting tool](#) that might help.)

The talent shortage is also at hand. The irony, however, is that regionalizing or localizing supply chains almost invariably means moving infrastructure away from the largest populations, which generally go hand-in-hand with the lowest costs of labor. Are the industry's finances solid enough to withstand double-digit increases in labor expenses?

For the record, the panel laughed when I rhetorically asked if customers are willing to pay for all of this.

I think Goodwin's assessment about the reorienting of the supply chain is correct. (And sorry Mark,

but I hope we are both mistaken!) But I also think that the conversations over what a truly secure chain would look like – and who will pay for it – aren't yet taking place at the level or degree needed to prove us wrong.



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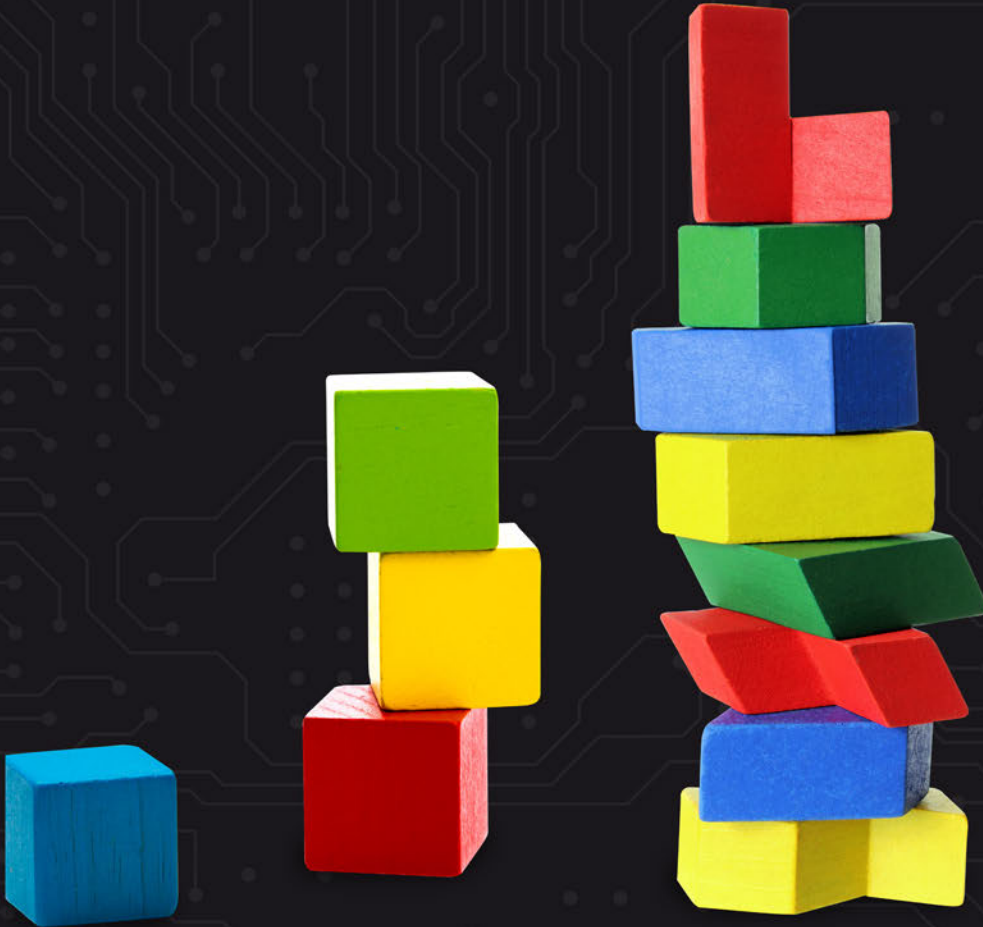
P.S. As 2023 draws to a close, a word of thanks and gratitude to our members, customers, board of directors, and other friends and colleagues, of which there are far too many to cite, for your support this year. Pursuit of the ideals encapsulated in our motto – “Collaborate, Educate, and Inspire” – starts with each of you, and we at PCEA draw from your energy and passion every day. Thank you.

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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TTM Technologies to Build New Plant in NY


DEWITT, NY – TTM Technologies has announced plans to build a PCB manufacturing facility in upstate New York with an investment of up to \$130 million over the next three years.

The proposed facility will be located next to TTM's existing facility on a 24-acre property off Kirkville Road in DeWitt and will either match or exceed that plant's 160,000 square-foot size, TTM said in a release.

The company said the plant will produce high-density interconnected printed circuit boards that will support national security requirements and is expected to create 400 "good-paying" manufacturing and engineering jobs.

The PCBs will primarily be used for US military applications and are critical to the U.S. semiconductor industry, which powers everything from data centers to the power grid to aerospace engineering, Sen. Chuck Schumer said in a statement.

"A global chipmaking hub is rising in Central New York," Gov. Kathy Hochul said in a statement. "Companies like TTM are helping to strengthen New York's reputation as a leader for growth, innovation, and national security."

Groundbreaking on the site is expected in the first half of 2024, and additional expansion is also being considered for future phases of development, TTM said. 


All Flex Solutions Acquires Facility in Minneapolis

NORTHFIELD, MN – All Flex Solutions plans to build a new flexible circuit manufacturing plant in a recently acquired building in Minneapolis.

The planned manufacturing plant will increase the company's capacity to manufacture flexible circuits, flexible heaters, and CatheterFlex circuits – the company's newest product line.

“We are initiating an acceleration this year,” said Kevin Jackson, president and CEO, All Flex Solutions. “Last year we focused on the merger of All Flex Flexible Circuits and Printed Circuits and the integration of two strong teams. Now, with a united All Flex Solutions team poised for growth, we look forward to this expansion.”

The new facility will also accommodate plating and final finishing processes, including ENIG, ENEPIG, EPIG, and hot air solder leveling (HASL), which are currently housed in a nearby facility. The move of these operations along with the new property buildout opens additional manufacturing capacity for the assembly of flexible circuits, rigid-flex circuits and flexible heaters, and CatheterFlex circuits, the company said.


“The investments we're making now in capacity and technology will accelerate our throughput at higher yields and with greater technical capability than we've ever had,” added Jackson. “We are excited about the many ways this increased capacity will help us serve our customers in the years to come.” 

DoD Awards \$40M to Calumet Electronics for HDBU PCBs

WASHINGTON – The US Department of Defense announced an award of \$39.9 million via the Defense Production Act Investment (DPAI) Program to Calumet Electronics to enhance capabilities to produce high-density build-up (HDBU) substrates, which include high-density interconnect printed circuit board (PrCB) cores and HDBU build-up layers.

“The Biden Administration has prioritized the need to support and advance the domestic PrCB and advanced packaging industrial base,” said Dr. Laura Taylor-Kale, Assistant Secretary of Defense for Industrial Base Policy. “These technologies are critical for modern weapons systems and will contribute to maintaining our warfighting edge over potential adversaries.”

The award will enable Calumet to scale up engineering, tooling, and manufacturing operations to establish domestic production capabilities for HDBU substrates. HDBU substrates and advanced packaging are critical enabling technologies for sixth generation systems and applications, including for radar, electronic warfare, processing, and communications. The company is located in Calumet, MI.


In calendar 2023, the DPAI Program has made 22 awards totaling \$714 million. DPAI is overseen by the ASD(IBP)'s Manufacturing Capability Expansion and Investment Program (MCEIP), in the Office of the Deputy Assistant Secretary of Defense for Industrial Base Resilience. For more information on MCEIP, visit: <https://www.businessdefense.gov/ibr/mceip/index.html>. 

Shennan Circuits to Build PCB Plant in Thailand

SHENZHEN – The board of directors of Shennan Circuits has unanimously approved a major investment to build a printed circuit board fabrication facility in Thailand.

The company, through its subsidiary Oboten Co., plans to spend up to RMB1.27 billion (\$183 million) toward the new site in the Rojana Industrial Park in Ayutthaya.

Shenzhen-headquartered Shennan was founded in 1984 and has manufacturing facilities in Shenzhen, Wuxi and Nantong, Jiangsu, China.

About 40% of Shennan's PCB revenue comes from customers outside China, a figure the company aims to increase. 

SP Manufacturing Expands Design Centers to US

SAN DIEGO – SP Manufacturing, a provider of electronics manufacturing services for mission-critical industries, has opened a design and development center here, the company announced.

The center will focus on providing engineering and development services for SP Manufacturing's

global customers. Services provided include product conceptualization, product design and engineering, prototyping, early supplier involvement, NPI, DfX and design for manufacturing, supply chain planning, and transition to mass production.


The company's applications include industrial, medical devices, automotive and IIoT.

The center is led by a veteran engineering team with over 20 years of experience.

“With the capabilities and location of its new center, SP Manufacturing can collaborate more closely than ever with customers onshore in the United States, and support the entire product lifecycle from design to mass production at its global manufacturing sites in Indonesia, Malaysia, China, Germany and Poland,” the company said in a press release.

“We're delighted to expand into the United States, where so many of our leading customers are located. Our new Design and Development Center allows us to collaborate with customers more closely than ever, providing onshore services and support for customers that must operate at unfailing standards of technical performance and delivery,” said Jackson Tan, global business development director, SP Manufacturing.

Philip Ong, CEO, SP Manufacturing, said: “We're happy to unlock the next evolution of SP Manufacturing as a global manufacturing platform for mission-critical industries. We can now deliver our manufacturing expertise in medical, industrial and automotive electronics manufacturing across the entire product lifecycle, around the world.”

SP Manufacturing has mass production sites in Southeast Asia, China and Europe. 

NCAB Group Acquires Spain's Electronic Advanced Circuits


STOCKHOLM – NCAB Group has signed an agreement to acquire 100% of the shares in Electronic Advanced Circuits based in Madrid.

NCAB will pay SEK14 million (\$1.25 million) with a potential earnout capped at a maximum amount of SEK4 million (\$358,000). The transaction is scheduled to close in November.

Electronic Advanced Circuits expects net sales of SEK 19 million (\$1.7 million) in 2023 with an estimated EBITA margin of about 15%. The company has two employees. The majority of sales comes from the telecom and industrial sectors and sourcing is made from manufacturing partners in China.

NCAB Spain had 13 employees and sales of SEK75 million (\$6.7 million) in 2022. The acquisition is expected to be accretive to earnings in 2024. Synergies are expected in the areas of suppliers, payment terms and logistics.

NCAB Group is also establishing an entity in Portugal, NCAB Group Portugal, and two new employees have been recruited, both with extensive experience in the PCB industry.

In a statement, Benjamin Klingenberg, vice president, NCAB Europe, said: “With these two strategic actions, we gain highly skilled and experienced personnel, who will complement our existing capabilities and play a pivotal role in unlocking new growth opportunities and expanding our networks. We are taking steps forward in our expansion plans in Spain and Portugal. The Iberian Peninsula is of growing interest for the electronics market in Europe.” 

EPA Seeks to Fine Fab for Alleged CWA Reporting Violation


WASHINGTON – The US Environmental Protection Agency on Nov. 9 issued notice of a proposed administrative penalty assessment for alleged violations of the Clean Water Act at a printed circuit board fabricator in upstate New York.

The complaint addresses violations of the general pretreatment regulations found at Standard Printed Circuits’ facility in Sherburne, NY. According to the complaint, Standard Printed Circuits failed to comply with reporting requirements in accordance with 40 C.F.R. § 403.12(e).

EPA is seeking a proposed penalty of \$10,000. EPA has provided the respondent with a settlement offer of \$2,000 in an effort to promptly settle this matter.

EPA is also providing notice of opportunity to comment on the proposed administrative complaint filed on Oct. 25 with the Regional Hearing Clerk.


Under 33 U.S.C. § 1319(g), EPA is authorized to issue orders assessing civil penalties for various violations of the CWA. EPA may issue such orders after the commencement of a Class I or Class II penalty proceeding. EPA provides public notice of the proposed assessment pursuant to 33 U.S.C. § 1319(g)(4)(A) and 40 C.F.R. § 22.45.

The deadline for submitting public comment on this administrative penalty proceeding is 40 days after issuance of the public notice. 

Skychem Building Production Facility in Thailand

ZHUHAI, CHINA – Skychem Technology is planning a CNY100 million (\$13.8 million) production plant in Thailand to establish overseas capacity and expand abroad.

The maker of electronic chemicals said nearly 30 companies based in the Chinese mainland, Taiwan and Japan have moved their printed circuit board factories to Thailand in recent years, and most are Skychem's clients or potential customers.

The Zhuhai-based firm said overseas business would focus on Thailand and cover SE Asian regions including Malaysia and Vietnam. 

Kaynes Technology to Build PCB Fab Facility in India

MYSURU, INDIA – Kaynes Technology will invest Rs 750 crore (\$90 million) for a bare board printed circuit board plant here.

Kaynes SemiCon, a Kaynes subsidiary, also announced an investment of Rs 2,850 crore (\$342 million) to develop an OSAT (outsourced semiconductor assembly and testing) facility in Hyderabad. The facility will also have an automatic test equipment (ATE) and reliability testing line.

In November, Kaynes held a groundbreaking ceremony for the facility, which will feature 13 lines for OSAT, one for ATE, and one for reliability testing. Additionally, Kaynes SemiCon will invest Rs

83.3 crore (\$10 million) in a co-packaged optics research and development facility for Silicon Photonics in Mysuru. 

Chinese PCB Fabricator Ordered to Pay \$7.6M in Damages to US Distributor


FORT LAUDERDALE, FL – Jiangmen Benlida Printed Circuit Co., a Chinese PCB manufacturer, was ordered to pay US distributor Circuitronix nearly \$7.6 million in damages after a federal jury found the company in breach of a distribution agreement.

Federal jurors in Florida found that Benlida exploited Circuitronix (CTX) once it hit rough financial straits, costing the distributor millions of dollars, capping off a years-long legal battle that began with Benlida filing its own breach of contract claims against CTX.

In 2012, Benlida and CTX entered into a manufacturing agreement under which CTX would send circuit board designs to Benlida for manufacturing. The finished products were then sent back to the US for distribution. In June 2021, Benlida accused CTX of skipping out on \$13.7 million worth of circuit board invoices. CTX denied Benlida's claims and countersued, arguing that it was Benlida that owed CTX millions of dollars.

In filings to the court, CTX argued that Benlida demanded advance payments for the circuit boards but failed to properly credit payments to its account. Additionally, Benlida had sent out shipments late, incurring late fee penalties that further spiked its outstanding debt, CTX claimed. Before the jury, CTX's attorney, Stephen Rosenthal, argued that the debt stemmed from cash flow problems on Benlida's part, saying the manufacturer had improperly relied on CTX to solve them.

Months before the trial, CTX asked the Florida federal court to dispose of Benlida's suit, arguing that nearly half of the invoices belonged to an affiliate, Circuitronix (Hong Kong) Ltd. CTX claimed responsibility for the remaining invoices but argued that it had already settled those payments in full.

US District Judge Robert Scola Jr. sided with CTX, agreeing with CTX that it couldn't be held accountable for services charged by CTX Hong Kong. 

Israel Aerospace Industries Files for Integrated Circuit Assembly Patent

LOD, ISRAEL – Israel Aerospace Industries has filed a patent for an integrated circuit assembly featuring a base structure with an interposer board and interfacing dies, and a cap structure with an intermediating board and a panel of active elements.

The cap structure is attached to the base structure, allowing the active elements to be electrically coupled to the interfacing dies. The patent also covers a backend circuit board and a method of fabricating it, as well as an array of such tiles in cascade connection.

The patent application describes an integrated circuit assembly that includes a base structure and a cap structure. The base structure consists of an interposer board and a plurality of interfacing dies that are electrically connected to the interposer board. The cap structure includes an intermediating board and a panel of active elements, which form the top side of the integrated circuit assembly. The active elements are electrically connected to the intermediating board. The cap structure is attached to the base structure in a way that ensures each active element is electrically connected to at least one interfacing die.


The integrated circuit assembly also includes electric wiring and/or contact means that connect the interfacing dies to the interposer board. The interposer board has electrical contactors on one side, which are connected to the interfacing dies through the electrical wiring and/or contact means.

The interfacing dies consist of operating components that control the operation of the active elements. Each group of interfacing dies includes at least one control module that controls the operation of the operating components in that group. There is also a main control unit that controls the operation of all the control modules.

The intermediating board has coupling components that electrically connect each active element to at least one interfacing die. The interposer board and the intermediating board are implemented in wafers, and the interfacing dies and the active elements are connected to their respective wafers through wire bonding.

The method of constructing the integrated circuit assembly involves electrically connecting the

interfacing dies to the interposer wafer and the active elements to the intermediating wafer. The cap wafer, which includes the active elements, is then attached to the base wafer, positioning the active elements at the top side of the integrated circuit assembly.

Overall, this patent application describes an integrated circuit assembly that allows for efficient electrical coupling between active elements and interfacing dies, enabling the control and operation of the active elements by the interfacing dies. The construction method outlined in the patent application ensures proper connectivity between the different components of the integrated circuit assembly. 


Jabil Opens New Plant in Mexico

CHIHUAHUA, MEXICO – Jabil has opened a new production facility at its site here, with the 250,000 sq. ft. plant joining the two other factories already onsite.

The new plant will play a critical role in supporting Jabil’s customers across the energy, automotive and transportation, healthcare, digital print, and retail industries, the company said in a release.

“We are thrilled to announce the opening of our third manufacturing building in Chihuahua, which reflects our commitment to excellence and innovation in Latin America,” said Victor Brizuela, Jabil’s vice president of operations for Latin America. “This expansion will allow us to serve our customers better, create more jobs and opportunities for our talented workforce, and contribute to the economic and social development of the region.”

In the past year, Jabil’s Chihuahua workforce has grown from 8,000 to around 10,000 employees.


“This new facility will enhance our operational efficiency and flexibility, as well as our ability to deliver high-quality products and services to our customers across different industries and geographies,” added Sándor Kékesi, operations director at Jabil’s Chihuahua site. 

Northrop Grumman Commits \$200M to New Electronics Site

WAYNESBORO, VA – Northrop Grumman will invest more than \$200 million to establish a new

advanced electronics manufacturing and testing facility here, where more than 300 jobs will be created during the next five years as the state-of-the-art facility is fully established.

“Northrop Grumman’s expanding Virginia footprint sends a powerful message that the Commonwealth is a magnet for investment underpinned by a next-generation workforce,” said Governor Glenn Youngkin. “This global leader’s cutting-edge facility in Waynesboro will provide job opportunities that attract and retain high-quality talent and create a transformational ripple effect for the entire region.”

“This new facility will increase capacity to manufacture and test advanced electronics and mission solutions to meet our customers’ growing needs,” said Kathy Warden, chair, chief executive and president, Northrop Grumman. “We are pleased to expand our technology presence in the Commonwealth and look forward to welcoming more people to our mission-driven team.” 

Jabil Makes Multiple Peripheral Acquisitions

ST. PETERSBURG, FL – Jabil will take over the manufacture and sale of Intel’s current Silicon Photonics-based pluggable optical transceiver product lines and the development of future generations of such modules, one of three deals the EMS/ODM announced in November.

Jabil also announced the acquisition of Retronix, a provider in the reclamation and refurbishment of electronic components, and specialized procurement firm ProcureAbility, giving it a footprint in the procurement sector.


The deal with Intel “better positions Jabil to cater to the needs of customers in the data center industry, including hyperscale, next-wave clouds, and AI cloud data centers,” said Matt Crowley, senior vice president of cloud and enterprise infrastructure, Jabil. “This deal enables Jabil to expand its presence in the data center value chain.”

Through its photonics business unit, Jabil empowers organizations to reduce the complexities of developing and deploying enhanced optical networking solutions by offering complete photonics capabilities, including component design, system assembly, and streamlined supply chain management.

Retronix specializes in component recovery, reballing, retiling and component authenticity testing services, and its acquisition adds exclusive technologies to Jabil's portfolio and also maintains security, quality and certification standards, the company said in a release.

Jabil said the acquisition also adds to its current circular economy services, including reverse supply chain management, medical device reprocessing, recycled packaging and emission reductions.

ProcureAbility offers strategy and procurement transformation services, managed services such as category management support and sourcing execution, and digital solutions including analytics-as-a-service and spend and market intelligence analytics. It also offers staffing and recruiting services to help businesses scale their procurement departments as needed.

"Together we're revolutionizing the procurement landscape and how we deliver solutions to organizations to help them drive transformative change and create value," said Frank McKay, chief supply chain and procurement officer at Jabil. 


Incap Opens 3rd India Factory

TUMKUR, INDIA – Incap India has started full-fledged production at its newest plant here, marking the company's third factory in the country.

The new factory includes two SMT lines with an x-ray machine, two wave soldering machines, a dry heat chamber, stuffing lines, and finished goods storage. Around 300 employees will work in the facility, and combined with the company's other two factories in the country, Incap India now has a total of 26,500 sq. m. of floor space.

"The third factory expansion highlights our commitment to supporting our customers' growth. By increasing our production capacity and integrating advanced technology, we are positioned to deliver even greater value and support to our customers worldwide," said Murthy Munipalli, managing director of Incap India.

Incap India's factories are all located in Tumkur, near Bangalore. In India, Incap specializes in manufacturing electronics and box-build products, having long experience, particularly in power electronics. The factory produces inverters and UPSs, PCBs for fuel and cash dispensers, power supply units, rescue devices, solar inverters, drives, and medical devices, as well as devices for other

electronic industrial products. The company's customers are globally operating electronic device manufacturers who may be established in Europe but have production facilities in Asia. 

Dixon Technologies Acquires 100% Stake in Dixtel Infocom

NOIDA, INDIA – Dixon Technologies has acquired a 100% stake in Dixtel Infocom.

The contract electronics manufacturer bought shares of Dixtel for a cash consideration of Rs 1 lakh (\$1,200), per an exchange filing in early November.

Dixtel has been incorporated as a wholly-owned subsidiary of Dixon Technologies as of Sept. 20, the company said.

“The wholly-owned subsidiary has been incorporated with an object to undertake electronic manufacturing services and wholesale/trading of electronic equipments thereof,” the filing said.



Emerald EMS Takes Shine to Ascentron

SALEM, NH – Emerald EMS, a contract electronics manufacturer, in November announced the acquisition of Ascentron, based near Medford, OR. This strategic move reinforces Emerald EMS' dedication to expanding its capabilities and geographic presence, enabling the company to better serve its customers and foster continued growth.


Ascentron has an extensive customer base within the life sciences and aerospace sectors, and is FDA-registered. This acquisition broadens Emerald EMS' customer base and adds expertise in the specialized fields of life sciences and aerospace.

Emerald named Amanda Brewer to lead the newly acquired operation.

In a statement, Brewer expressed her enthusiasm for this new chapter, saying, “Ascentron has established a strong reputation and a highly regarded team in the Pacific Northwest. I am humbled and honored to be part of this esteemed group and to have this revered team join the Emerald

family. Together, we anticipate exciting opportunities, and I am eager to uphold our tradition of delivering exceptional service and quality to our valued customers.”

Ascentron CEO Hartmut Liebel emphasized, “This addition to the Emerald family of companies expands our geographical footprint through the addition of a facility in southern Oregon, thereby reinforcing our commitment to serving our customers in the western United States.”

Emerald EMS has engineering services and manufacturing facilities in California, Michigan, New Hampshire, Shenzhen and Penang. 

IKT Expands EMS Sites to Bulgaria

CHERNIHIV, UKRAINE – IKT Group has opened a contract electronics assembly factory in Plovdiv, Bulgaria. The new plant is the EMS company’s third in Europe.

The company said it chose the location for its proximity to customers in the European Union and Israel, and to lower risks associated with production in its native Ukraine. After considering several countries in Eastern Europe, Bulgaria was selected for its investment climate, vibrant electronics sector and growing economy.

The company has procured lines from Juki, PBT Works, and Olamef, among others, for the new plant, which is called IKT Electronics.

IKT also has sites in Israel and Ukraine. 

PCD&F

All major DRAM chipmakers have reportedly prioritized DDR5 and high-bandwidth memory (HBM) in anticipation of a surge in demand from generative AI.

AT&S will reportedly start building IC chip substrates for **AMD** at its new plant in Malaysia next year.

Chin Poon Industrial said it will focus on expanding its PCB capacity in Thailand.

Dispelix signed separate agreements with **Foxconn Industrial Internet** and **Pegatron** to develop reference designs for AR glasses.

Eltek received five purchase orders totaling \$3.8 million.


Microchip Technology is expanding its Detroit Automotive Technology Center, which serves as a hub for automotive clients, offering resources and technical expertise to assist in the development and optimization of designs.

NextFlex announced \$6.49 million in funding for seven new projects as part of its Project Call 8.0 to further promote FHE development and adoption throughout the US advanced manufacturing sector.

PCBPit installed a new PCB assembly production line in Shenzhen.

Pengding Holdings has invested 2.5 billion baht (\$69 million) into its newly created Thai subsidiary.

Ventec Giga Solutions, the equipment division of **Ventec International**, has been named

sales agent and distributor for **Yeitek**'s PCB cleaning machines and accessories in EMEA, the United Kingdom, and the Americas, and for **Hi-Print** inkjet-printers in Europe and North America. 

CA

AGS Devices purchased a **Hentec Industries/RPS Automation** Pulsar solderability testing system.

Cisco, Optus and **La Trobe University** are launching the Digital Innovation Hub, a state-of-the-art innovation precinct located at La Trobe's Bundoora campus, which offers technological capability for greater collaboration between students, researchers, business and industry.

Custom Interconnect has completed its transfer of all microelectronics and power device staff and equipment into its semiconductor packaging plant and is adding PCB assembly.

Datalink Electronics, a UK EMS provider, has been acquired in a management takeover with support from **KBS Corporate**.

EMS Solutions adopted **Cetec ERP's** manufacturing software solutions.

Jaltek Systems signed a collaboration agreement with **SG Automotive** to support demand from the European and UK markets.

Luxshare Precision Industry plans to invest an additional \$330 million in a manufacturing plant in the northern Vietnam province of Bac Giang, bringing the EMS company's total investment there to more than \$500 million.

Molex has opened a production manufacturing campus in Katowice, its third in Poland.

Murray Percival will represent **American Beauty** products.

Orel launched Sri Lanka's first professional electronics manufacturing assembly line.

Pemtron opened a new office in Penang, Malaysia.

PVA named **Altus Group** exclusive distributor for Ireland and **ESD-Center** its supplier in the Baltics and Norway.

Rocka Solutions has increased its warehouse capacity in Pharr, TX, and established a new warehouse in El Paso, TX.


SmartTec Nordic will represent **Universal Instruments** in Finland, Norway and the Baltic regions (Lithuania, Estonia and Latvia).

S and Y Industries partnered with **Cetec ERP** for manufacturing operations.

TE Connectivity ordered a **Hentec Industries/RPS Automation** Odyssey 1750 component lead tinning system.

Tempo Automation received notice that its securities will be delisted from the Nasdaq Global Market.

TRI opened a new office in Bangkok, Thailand.

ZTest Electronics has announced agreements to settle a total of \$357,490 owed to two officers and one director of the company, and one other creditor for management fees and directors fees. 

PCB EAST 2024
Conference & Exhibition

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Engineering Tomorrow's Electronics

CONFERENCE: June 4 - 7

EXHIBITION: Wednesday, June 5

Boxboro Regency Hotel & Conference Center, MA

WHO'S EXHIBITING

Accurate Circuit Engineering

All Flex Solutions

Allfavor Technology

Altair

APCT

Archer Circuits Company, Ltd.

Cadence Design Systems

DownStream Technologies

Electronic Interconnect

EMA Design Automation

Fischer Technology Inc.

Freedom CAD Services, Inc.

GS Swiss PCB

Identco

Imagineering, Inc.

PCB Technologies USA

Polar Instruments, Inc.

Printed Circuit Board Association of American (PCBAA)

Printed Circuit Engineering Association (PCEA)

Quantic Ohmega / Ticer Technologies LLC

Screaming Circuits

Sourceability

Surface Mount Technology Association (SMTA)

Sunstone Circuits

SVTronics, Inc.

Trilogy-Net Inc.

Trylene Inc.

Ventec International Group

XDry Corporation

PCBEAST.COM

PCD&F




Trey Adams

Axiom Space named **Enoc Sotelo** PCB designer.

Calumet Electronics appointed **Trey Adams** vice president and general manager.

Millennium Circuits named **Jackie Beauchamp** account manager.

TCLAD named **Steve Taylor** VP of global sales and marketing. 

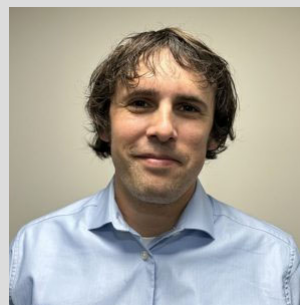
CA



Diego Jiang



Wei Jye Lim



Nick Hurrell



Andy Mackie



Jim McCoy



Rich Fitzgerald



James Doyle



Amy Fredregill



Mary Thornton



Rich Templeton



David Goeckeler



Sy Creed

AIM Solder appointed **Diego Jiang** product manager and **Wei Jye Lim** technical sales engineer.

Altus Group appointed **Nick Hurrell** applications engineer.

Indium promoted **Andy Mackie** to principal engineer – Advanced Materials and **Jim McCoy** to product manager for engineered solder materials.

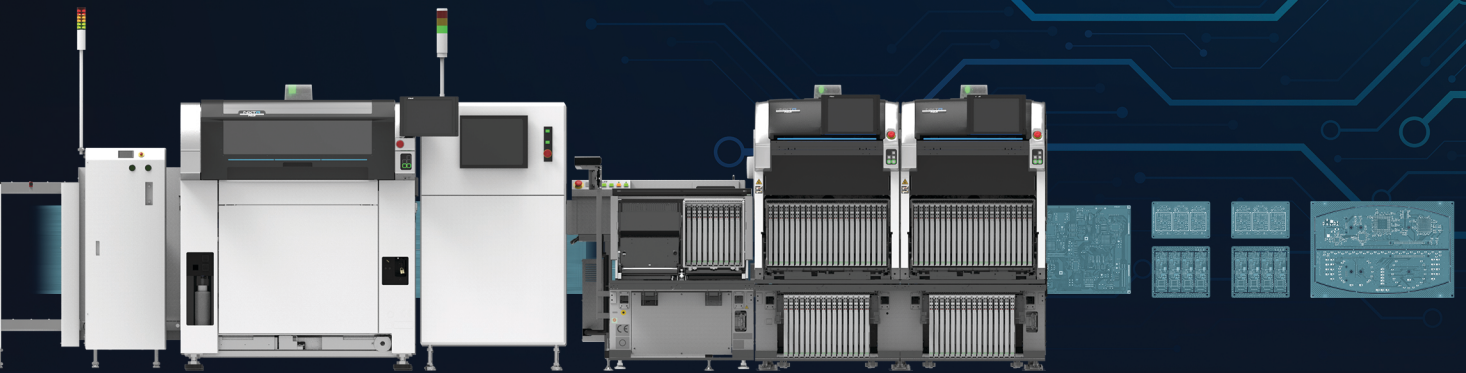
NEOTech appointed **Rich Fitzgerald Jr.** CEO of its industrial & medical division and **James Doyle** CEO of its aerospace & defense division.

Nortech Systems added **Amy Fredregill** and **Jose Peris** to its board of directors.

The Semiconductor Industry Association appointed **Mary Thornton** vice president of global policy, elected **Rich Templeton** chair of its board of directors and elected **David Goeckeler** vice chair.

ViTrox named **Sy Creed** business development director for the USA region. 

QUALITY AUTOMATION ACROSS THE BOARD

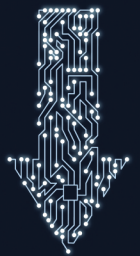


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PCEA Announces Upcoming Technical Webinars

PEACHTREE CITY, GA – Printed Circuit Engineering Association (PCEA) will hold three member webinars in the coming months on PCB materials, PCB thermal management and the impact of artificial intelligence on electronics.

On Dec. 13, Tony Senese and Eriko Yamato of Panasonic will present PCB Material Properties – Consideration for Design and Manufacturing. Engineers use PCB material product charts to reference electrical, mechanical and thermal properties to seek the best solutions for specific applications. It is important to understand the significance of a given property and how it affects PCB design and manufacturing. This presentation will cover key material properties such as Tg and modulus to guide how they can impact PCB design and processing. The presenters will also discuss IPC test methods and why they matter.

On Jan. 17, Doug Brooks and Dr. Johannes Adam will present Via and Trace Currents and Temperatures. Rather than thinking of current density, the presenters say, focus on material parameters and properties that determine the temperature of a trace and how these are calculated. Results of some simulations of vias of varying widths and amps will be shown.

And on Jan. 23, a special panel will debate AI in Electronics. Artificial intelligence has made its way into ECAD and other software used in electronics manufacturing. But what's the actual intelligence in these tools? And in what ways – and how soon – can we expect them to impact our roles? CTOs and related domain experts from a handful of ECAD companies will offer a snapshot of where we are, what's feasible, and the forecasted timeline for implementation.



Tony Senese




Eriko Yamato



Doug Brooks

All webinars will include time for audience questions. To register, visit <https://pcea.net/events>.

PCEA member webinars are free for all PCEA members. Join as an individual member for free at <https://pcea.net/pcea-membership>. 



ANNOUNCEMENT

PCE-EDU, the industry leading PCB designer and design engineer training and certification program, is now **PCEA Training!**

Developed by Mike Creeden, Steph Chavez, Gary Ferrari, Rick Hartley and Susy Webb, the 40-hour live curriculum includes a 400-page handbook containing information on everything from parts libraries to high-speed design.

pceatraining.net

UPCOMING CLASSES:

December 4 - 8

February 5, 12, 20, 26 & March 4

April 5, 12, 19, 26 & May 3

IDC: Semi Market Begins Return to Growth


SAN MATEO, CA – The semiconductor market has hit bottom and has begun a return to growth that will accelerate next year. That’s according to IDC, which in November raised its September revenue outlook to \$526.5 billion from \$518.8 billion. Similarly, the market research firm lifted its 2024 outlook to \$632.8 billion from its previous forecast of \$625.9 billion, citing US market demand resiliency and a recovery in China by the second half of 2024.

IDC sees better semiconductor growth visibility as the long inventory correction subsides in two of the largest market segments: PCs and smartphones. Automotive and Industrials elevated inventory levels are expected to return to normal levels in the second-half 2024 as electrification continues to drive semiconductor content over the next decade. Technology and large flagship product introductions will drive more semiconductor content and value across market segments in 2024 through 2026, including the introduction of AI PCs and AI smartphones next year and a much-needed improvement in memory ASPs and DRAM bit volume.

Wafer capacity pricing will remain flat next year as foundry suppliers gradually improve utilization rates and demand returns from their core fabless customers. CapEx is expected to improve as well as revenue shipments match end demand and regional Chips Act incentives stimulate investment across the supply chain.

Still, 2023 semiconductor revenue will be down 12% year-over-year before rebounding 20.2% in 2024.

“Revenues will continue to recover gradually and accelerate in 2024,” said Mario Morales, group

vice president, IDC. “The semiconductor market reached a bottom and has begun to grow on a quarter-over-quarter basis. ASPs are improving in DRAM, which is a good early indicator and IDC expects suppliers will continue to control capacity additions and utilization rates to drive a sustainable recovery. Accelerating demand for AI servers and AI-enabled end point devices will drive more semiconductor content in 2024-2026 fueling a new upgrade cycle across enterprises. We expect that by the end of our forecast period, AI silicon will account for almost \$200 billion in semiconductor revenues.” 

Peripherals, Front and Center

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	JUL.	AUG. ^r	SEP. ^p	YTD
Computers and electronics products	0.4	0.2	0.5	2.0
Computers	3.9	2.6	-3.1	10.9
Storage devices	13.5	-1.4	-0.9	13.0
Other peripheral equipment	-14.5	9.1	2.6	29.9
Nondefense communications equipment	0.3	-0.5	1.7	-1.7
Defense communications equipment	5.6	-3.8	-2.0	3.0
A/V equipment	44.6	-16.2	-12.3	13.7
Components ¹	-1.6	4.8	2.8	2.0
Nondefense search and navigation equipment	-0.4	-0.9	0.7	1.2
Defense search and navigation equipment	0.6	0.0	0.0	3.9
Electromedical, measurement and control	-0.1	-0.3	-0.5	0.9

^rRevised. ^pPreliminary. ¹Includes semiconductors. Seasonally adjusted.

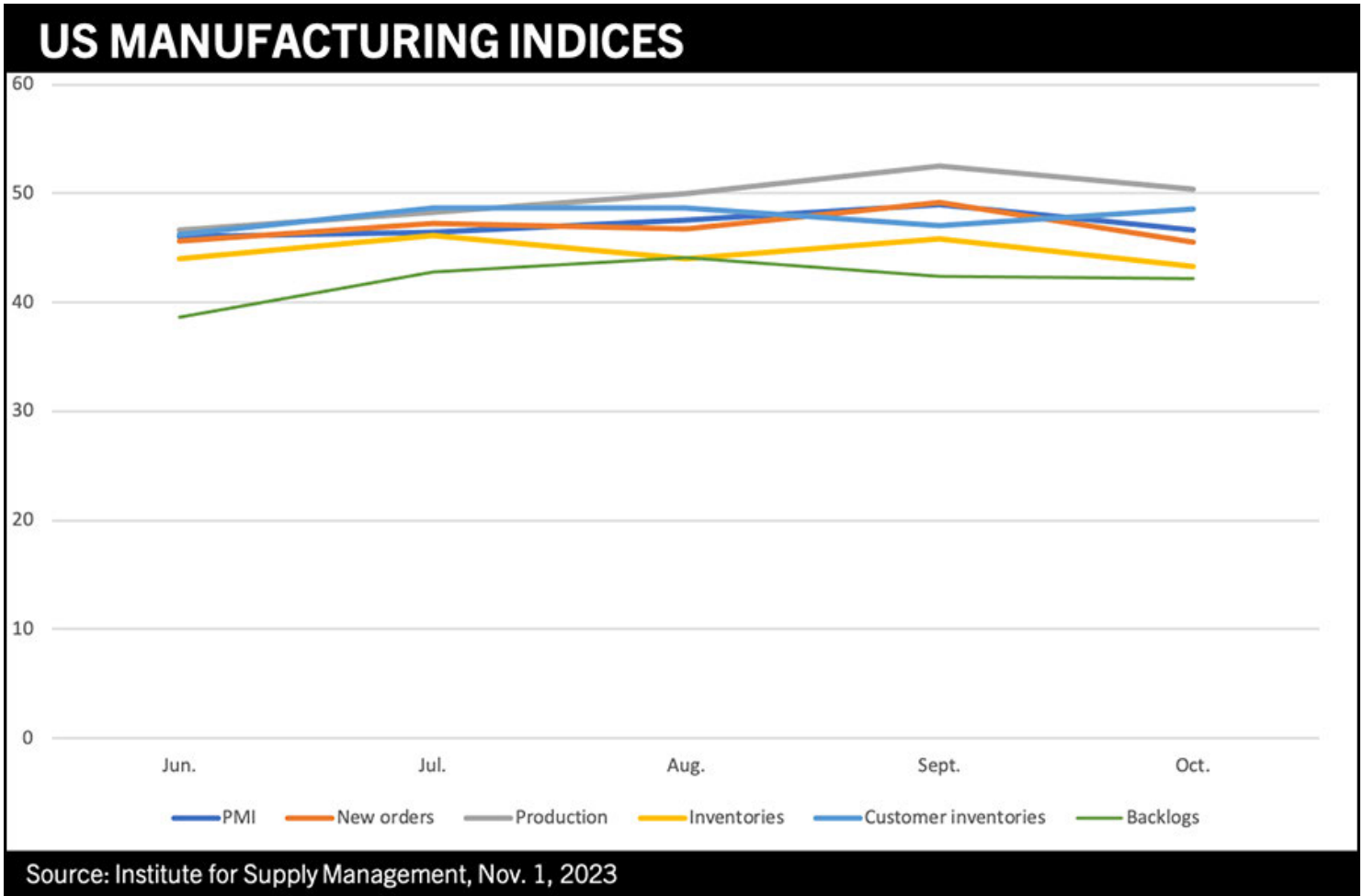
Source: US Department of Commerce Census Bureau, Nov. 2, 2023

Key Components

	JUN.	JUL.	AUG.	SEPT.	OCT.
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EMS book-to-bill ^{1,3}	1.24	1.24	1.27	1.27	TBA
Semiconductors ^{2,3}	-15.7%	-11.8%	-6.8%	-4.5%	TBA
PCB book-to-bill ^{1,3}	0.98	0.98	1.00	1.01	TBA
Component sales sentiment ⁴	76.3%	83.0%	90.3%	86.7%	88.8%

Sources: ¹IPC (N. America), ²SIA, ³3-month moving average, ⁴ECIA



Hot Takes

Japan's PCB output has shrunk for 10 consecutive months and continues to fall into double-digit declines, with August representing the third-largest decline this year. (Japan Electronics Packaging Circuits Association)

Electronic sales are predicted to register a robust 22% quarter-over-quarter increase in the fourth quarter, adding to 7% growth posted in Q3 2023. (SEMI/TechInsights)

Worldwide **tablet shipments** posted a decline of 14.2% year-over-year in the third quarter, totaling 33.2 million units. (IDC)

Taiwanese electronic component manufacturers reported an industrial output of NT\$1.38 trillion in October, declining 11.95% year-on-year, as demand for chips softened and clients digested inventories, limiting business for local suppliers of chips, printed circuit boards and Ajinomoto build-up film, or ABF, substrates. (Taiwan Ministry of Economic Affairs)

Worldwide **silicon wafer shipments** decreased 9.6% quarter-over-quarter to 3.01 billion sq. in. in the third quarter, a 19.5% drop from the 3.74 billion sq. in. recorded during the same quarter last year. (SEMI Silicon Manufacturers Group)

Worldwide **smartphone shipments** declined 0.1% year-over-year to 302.8 million units in the third quarter. (IDC)

Global **shipments of notebooks** are expected to fall 10.2% from a year ago to 167 million units in 2023. With inventory pressures easing, however, shipment volume is forecast to rise 3.2% to 172 million units in 2024. (TrendForce)

Half of **Japan's PCB market** is produced in Japan, followed by the Chinese mainland and Southeast Asia (Thailand, Vietnam). By contrast, just 2% of South Korea's PCB are manufactured domestically, as its major manufacturers switch focus from HDI to BT carrier boards. (TPCA)



Speed Dating on the Job Scene

Stereotypes abound, but don't let first impressions fool you.

YOU NEVER KNOW quite what you may run into when you go looking to hire new staff. Such was certainly the case for me at a local job fair hosted by a state-sponsored regional workforce development organization.

I received the invitation from the local Chamber of Commerce to have a table at this event. The cost was free and the hours were 9 a.m. through 1:30 p.m. Based on the description, I thought the chance was reasonable to find a couple hires to fill openings in our drilling and plating departments. While it has been years since I participated in a job fair, I was familiar with the format and the similarity to the proverbial “speed dating”: quick conversation and move on!

Consistent with my expectations, on the specified day I show up bright and early at a community college, find the massive meeting room, locate my table among the 50 or so others in the room, and set it up with information about the company as well as the industry. All the tables were spoken for, and looking at the plethora of companies in attendance, I noted most were service providers. A good number, however, were manufacturing companies that produced everything from pianos to metal castings, with two of us, an EMS company and my circuit board fabrication company, representing “high technology.”

Set up and ready to go, that is, when reality and my expectations diverged. Attendance was certainly plentiful. There was also a lot of gray and white hair. In fact, I would say the average age of those manning tables for their respective companies was younger than the average age of the attendees looking for a job!

More interesting was talking with the attendees. I really did not expect to hear life stories, or what

prospective hires did *not* want to do. One of the younger folks to stop by was looking for a flexible schedule. When I asked why, the reply was: “Because I like to sleep in some mornings.” It’s no surprise, I suppose, he has worked for eight companies over the past six years. Many were retirees looking for part-time work, which preferably paid cash under the table. Some were looking to make a career change, but those candidates had no interest in manufacturing jobs; only office positions would do.

Possibly the most interesting character I met was an older guy full of personality, very engaging and funny – might be great in a sales role. Yet he was not looking for a job. Instead, he prowls job fairs in search of new swag. I am sure he was disappointed with what I had to offer, but the table next to me – a health club – was giving away beverage tumblers, so he at least scored there.


The gray-and-white-haired folks mostly appeared to be retirees who had had long careers at one place or another. The jobs they were looking for were mostly part-time, and on their terms. They wanted the employer to be flexible, but as employees they were not willing to reciprocate.

Meanwhile, the younger attendees who stopped by my table seemed to be looking for a “gig” versus a “job” or career. I was taken aback by how poorly they communicated, how casually they dressed for this gathering of potential employers, and how little they seemed to understand that jobs of all kinds have structured hours and require commitment.

I was ready to write off the experience and leave early when what felt like a changing of shifts occurred, similar to when the day workers log out and the afternoon shift logs in. Attendees began sauntering out, I presumed because it was approaching noon. However, after no more than five minutes, the room began to fill up again but this time the demographics looked quite different. The average age, and appearance, was decidedly younger. The pace was brisker.

The first person of this second wave who stopped at my table knew about circuit boards and electronics. He was an experienced, mid-career electrical engineer seeking to make a change where there would be upward career mobility. He was followed by a young woman with a degree in microbiology who was interested in finding a position in quality or compliance. Over the next hour, I met some impressive people. While none in either wave of attendees met the needs for the drilling or plating positions I needed to fill, I invited a couple to the plant for a round of interviews, and hired one for a more senior role.

The day did not go as anticipated but was still successful on a couple of levels. First, I did find someone to hire. Maybe not for the position I had planned to recruit for, but nevertheless, I found a solid addition to the team. Second, I was reminded how too many younger people really do not understand the demands of working for a large organization. Too many are living as if they are still in high school waiting for the next school vacation, rather than embracing the fact they now must make decisions, take personal pride in their dress and social skills, and commit to doing something that will provide a livelihood.

Clearly there are some who are career-oriented, looking for a better job and the opportunity to personally grow. Those who took the time to come out on their lunch break demonstrated they were committed and willing to invest their time exploring other jobs. Finally, having been reacquainted with job fairs, it still is a good way to find potential employees. The trick is to keep an open mind. 

PETER BIGELOW is president of FTG Circuits Haverhill; (imipcb.com); pbigelow@imipcb.com. His column appears monthly.

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Mind Your Units

Buyers beware: An ounce of copper is *not* 1 mil.

LONG BEFORE I became part of the PCB industry some 30 years ago, a large study determined that for the typical two-layer printed circuit board, the amount of copper required for a reliable connection in a plated through-hole (PTH) was 0.0007 inches, or 0.7 mils.

Anything less than that could compromise PTH reliability, the study found, and anything more would not make much difference.

Simply put, the 0.001", or 1 mil, as stated on most PCB fabrication drawings is a safety factor. Some corporate fab specs will even state a plating average of 1 mil, with 0.8 mils as the minimum, higher than the originally determined 0.7 mils.

However, even today, some PCB buyers confuse ounces with mils when it comes to the copper plating of a printed circuit board. It is important to know the difference.

The copper weight called out in a PCB is rated in ounces, which is the amount (weight) of the copper covering 1 sq. ft. of bare fiberglass material. In inches, 1 oz. of copper equates to a thickness of 1.34 mils of copper on the PCB – *not* 1 mil – and that is where the confusion lies.

When referring to “thickness,” we are really talking about the weight of copper used in the PCB.

Table 1 shows a helpful conversion chart between copper thickness values in weight, mils and microns.

Table 1. Copper Thickness Conversions

Oz.	Mils	Microns
0.5 oz./sq. ft.	0.67	17.05
1.0 oz./sq. ft.	1.34	34.1
2.0 oz./sq. ft.	2.68	68.1
3.0 oz./sq. ft.	4.02	102.2

The plating of a circuit board is a subtractive and additive process. Unless otherwise specified, the typical plating process most board manufacturers provide is around 1 mil of additional copper plating on top of the existing (or start) material.

PCB buyers must understand the manufacturing process to ensure they meet their customers' true copper weight requirements because the amount of copper plated on the surface means there might not be as much copper in the hole.

Copper is expensive, so to save money on a board that requires a 2 oz. finish, buyers will sometimes mistakenly ask the PCB vendor to "begin with one ounce and plate up to two," thinking that mil of plating is just enough to meet their needs.

Unfortunately, it is quite a bit *less* than required. Two ounces of copper equates to approximately 2.7 mils, and what the buyer just asked of the supplier will yield a PCB that has, at most, 2.4 mils of copper (1.34 mils to start plus the 1 mil plated). That's 10-15% less copper than desired.

Would that difference in thickness cause a problem for a PCB buyer's customer? I can't make that call. But by asking the board manufacturer to begin with 1 oz., the buyer is not getting what was asked for in the fab drawing.

The above computation does not permit the tolerances of the raw material itself. The copper on the clad material received may be on the lighter side, and that will affect overall finished thickness as well.

I don't mean to put all the blame on buyers. Many PCB salespeople confuse mils with ounces. To make their pricing more attractive, they too will offer to begin with 1 oz. and "plate up" to two. But a knowledgeable salesperson should find out the "start" weight up front.

Specifying on your PCB fab specs the copper start or "finished" weight of the designed circuit board is crucial for design or price.

If design, it is best to put what raw material you want your design to begin with, knowing that an additional 1 mil of copper will be applied during the normal manufacturing process.


If cost, then specifying the finished weight gives the board manufacturer the option on what weight to start with, as the amount of copper the raw material requires will dictate the final cost of the PCB.

The most commonly called-out copper weight value is 1 oz. finished, meaning the copper weight will be at least one ounce once completed, whether the PCB manufacturer starts with 0.5 oz. or 1 oz. of raw material that was plated to a higher value.

There is usually no extra charge when 1 oz. finished is called out. For weights above 1 oz., there will be additional cost and lead time for material availability.

PCBs that require heavy copper weight also incur additional process time for etching (the removal of all that extra copper) and to ensure customer-desired trace width and spacing is maintained.

And don't forget about PCB freight costs. Heavy copper means more weight, and thus more in shipping costs and proper packaging to hold those heavy boards in place during transit.

Mixing up ounces and mils can be a costly mistake, both in dollar terms and in maintaining a relationship of trust between PCB buyers and their customers. Don't overlook the details when it comes to the copper plating of a printed circuit board. 

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of DirectPCB and can be reached at greg@directpcb.com.



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Addressing New Challenges in 2024

Tips for adjusting to changing customer forecasts.

THE EMS INDUSTRY is running true to a cycle no one likes: big drops in demand following a period of inventory buildup. The drivers for inventory buildup were material constraints and unpredictable spikes in demand following the Covid lockdown period. OEMs increased both raw materials and finished goods in their desire to stay ahead of parts shortages and customer spending sprees. Unfortunately, our heated economy is finally slowing. While consumer spending has remained strong, they are tightening their belts on big purchases and purchasing fewer discretionary items.

As a result, electronics manufacturing services (EMS) providers are seeing a different set of issues than they have been dealing with the past two years. Material inventories are still high and forecasts are dropping as customers slow down new orders to burn off existing finished goods inventories. How do you counter these challenging trends? There should be three areas of focus:

- Partnering with existing customers on forecasts and orders
- Internal cost control
- New account acquisition.

Partnering with existing customers. When demand drops, a customer's first reaction is to lower excess finished goods inventory. While this improves their balance sheet, it also increases the uncaptured liability that higher-than-usual raw material inventory at an EMS provider represents. Consequently, a strategy that addresses both raw material and finished goods inventory is better than simply pushing out all orders a couple of quarters until finished goods inventory drops. From a program management perspective there are several steps to take:

- Make it easy for your customer to understand their current material liability and the impact any forecast pushout has;
- Discuss new product opportunities that could replace forecast drops and consume excess material;
- Determine options for mitigating inventory liability through liquidation;
- Review the customer contract or any excess material agreements signed during the material shortage period to see if the customer is liable for purchasing excess material or added cost if their forecast drops;
- Work with each customer to develop a plan that helps them continue to draw down excess inventory.

The goal isn't to drop the hammer contractual agreements may represent, but to come up with a workable solution that preserves the relationships built during the worst of the material allocation period. Given the much lower margins that most EMS companies have compared to their customers, excess inventory is a much bigger drag on an EMS provider than on an OEM.

“TRADE SHOWS IMPROVE WHEN THERE IS ECONOMIC UNCERTAINTY BECAUSE PEOPLE SEE BENEFIT IN NETWORKING.”

Internal cost control. Cost cutting in a slowing economy is management 101 and most companies are already doing this. That said, there may be hidden opportunities for cost control that get overlooked.

One of the first areas to review is receivables. Are all customers paying within terms? Have packing list or invoicing errors been slowing payments? Are there opportunities for negotiating more favorable terms to balance the cost of higher inventories?


Another area to consider is human behavior. We've just finished a period where unplanned cost

increases, expedites and schedule changes were the norm. That suspended a lot of cost control checks and balances. Have team members returned to practices more aligned with current conditions or are they still in firefighting mode?

The final area to review is quality. While production quality is a given at most EMS companies, is there equal focus on transaction quality? How much time gets wasted on administrative errors, inefficient processes or customer-driven changes that create uncompensated cost? Do employees consider the cost of inefficiency in their activities? If the answer is no, that may be an area with opportunities for improvement.

New account acquisition. Material allocation issues made customers afraid to change EMS providers. Improvements in material availability are now encouraging companies dissatisfied with their current EMS providers to shop for alternatives. New product development is also coming off the back burner.

Consequently, it's important that your company is easy to find and your sales team is tapping their relationships to identify companies that are looking. Increase educational content on blogs. Highlight innovative processes, capabilities or solutions in industry magazines. Exhibit at trade shows that have been relevant in the past and walk target industry trade shows that aren't a great traffic fit for exhibiting. Trade shows improve when there is economic uncertainty because people see benefit in networking. If budgets allow, consider advertising. While most ads don't generate trackable leads, they are the most efficient way to create brand awareness when the publication's audience and target decision-making audience are aligned. Suppliers can also be a good source of information on which companies are shopping. They are likely sharing that information with every EMS company that asks, however.

This year will bring a different set of challenges, but it will also have better opportunities. Good planning will put you in the best position to mitigate challenges with new opportunities. 

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of "Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services." She can be reached at smucha@powell-muchaconsulting.com.



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
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National Semi Consortium Starts with Next-Gen Workforce Focus

Government-funded organization hopes to knock down barriers to commercialization.

THE AMERICAN VACUUM Society (AVS) held its annual conference in Portland, OR, with roughly 2,000 in attendance for the November meeting. The conference included many technical presentations by students, faculty and industry on cutting-edge issues associated with materials, processing and interfaces.

Among the highlights this year was a special session on the Chips Act. The session on the Chips and Science Act Implementation for Microelectronics (including workforce) was moderated by Dr. Alain Diebold, SUNY Polytechnic Institute, and Dr. Tina Kaarsberg, US Dept. of Energy Advanced Manufacturing Office.

The first invited talk was given by Dr. Jay Lewis, director, National Semiconductor Technology Center (NSTC). NSTC is a public/private consortium authorized and funded by the US government to serve as the focal point for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide US leadership in the industries of the future. Dr. Lewis announced the [incorporation of a new nonprofit](#) entity, [SemiUS](#), to operate the NSTC. SemiUS will work in partnership with the US Department of Commerce to develop and implement a wide variety of programs to fulfill the mission of the NSTC consortium. The focus is on building a strong semiconductor research and development ecosystem in the United States.

Under the Chips for America program, \$39 billion in incentives has been allocated to invest in US production of strategically important semiconductor chips, and ensure a sufficient sustainable and

secure supply of older and current generation chips for national security purposes and critical manufacturing industries. To strengthen US semiconductor R&D leadership to catalyze and capture the next set of critical technologies, applications and industries, \$11 billion is allocated. Funding of \$2 billion for DoD Microelectronics Commons is targeted to establish a national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.” Workforce development initiatives underpin all programs. There is a focus on reducing barriers for the introduction of disruptive technology in the semiconductor industry. Gaps to be addressed include obstacles for startups and disruptive technologies (including chip design, process technology, metrology or materials), access to advanced foundries (often for R&D), and workforce.

Figure 1 illustrates big picture investment categories.

Big Picture – Investment Categories



CHIPS

Figure 1. US Chips Act investment areas. (Source: NIST, US Department of Commerce)


David Anderson, president of the New York Center for Research, Economic Advancement, Technology, Engineering, and Science (NY CREATES), detailed the latest activities in research and workforce development. Global research cooperation includes relationships with Interuniversity Microelectronics Centre (IMEC) in Belgium, the Korean Institute for Advancement of Technology (KIAT), Israel Innovation Authority and Silicon Saxony and Fraunhofer (both Germany). Research areas include neuromorphic computing, integrated photonics, test, assembly and packaging (TAP), quantum technologies, magnetic random access memory (MRAM) technology, advanced process technologies and integration, power electronics, and heterogeneous integration. Industry research partners include large companies such as GlobalFoundries, TEL, Wolfspeed and NXP, as well as startups and small and medium enterprises. Workforce developments include programs with universities, high schools and training programs for veterans.

Intel's Dr. Steve Pawlowski's view on the 1000x Performance Efficiency Goal highlighted architecture changes for future computing, and focused on the importance of, and relationship between, software and hardware.

Dr. Vijay Raghunathan of Purdue University described programs related to workforce development at the university, which successfully increased the number of students entering engineering by creating a course for freshman that introduces them to the industry. Student-run career fairs and industrial roundtable job fairs are among the methods used. The school's goal is a 500% increase in the number of engineering students in five years. Purdue's high school summer camps that introduce technology to potential students is one way to increase the number of students in the pipeline.

Power efficiency. I opened my presentation, "Saving Power with New Designs and and Chiplets in the New Era of Advanced Packaging," with a quote from Dr. Lisa Su, CEO of AMD, who asserts "energy efficiency is the most important challenge of the next decade." A chiplet is not a package, I noted, but rather a new IC design approach with multiple package options including laminate substrate (with and without the use of silicon bridges), silicon interposers and redistribution layer

(RDL) structures (with and without bridges). One of the most dramatic examples of improved power efficiency is 3-D stacking of chiplets using hybrid bonding. TSMC has published data indicating that its hybrid bonding process with 9 μ m pad pitch provides greater power efficiency than side-by-side configurations interposers or 3-D stacking with microbumps. AMD uses TSMC's technology for its 3-D V-Cache memory on logic stacking and reports a 3X interconnect energy efficiency versus 3-D with microbumps. This technology has been deployed in volume production for AMD's server and desktop processors for several product generations, as well as gaming and graphics applications. AMD's new AI product, MI 300, will use logic-on-logic stacking for GPU and CPU chiplets using TSMC's process. It will provide an even greater performance-per-watt improvement.

Many companies, including Intel and IBM, are working to develop 3-D hybrid bonding options. Challenges include the elimination of particles that can cause voids, careful consideration of thermal design and process developments. Co-packaged optics (CPO) is also under development and has the potential to provide 30% or more power savings in the datacenter. Examples of chiplets designs in silicon photonics applications have been demonstrated by Ayar Labs and Intel, Broadcom, Cisco, Marvell and others. TSMC is supporting CPO developments with its Compact Universal Photonic Engine (COUPE) that uses 3-D stacking with TSV in the photonic IC. The ecosystem is being developed and technology advancements are underway to enable deployment of CPO. 

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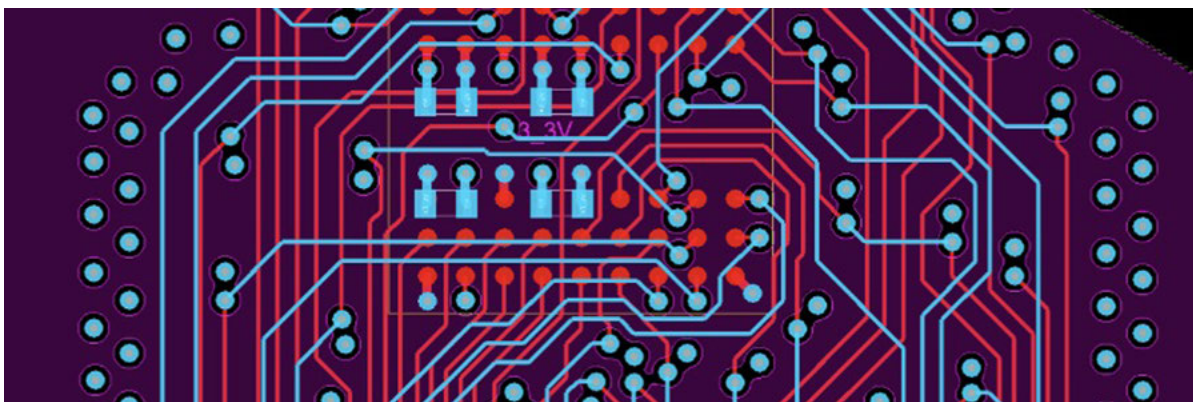
PCB Bus Routing

Fine tuning the timing of net groups.

WHEN FACED WITH a microcontroller and a companion memory chip, to unravel the crossed-over connections while maintaining high quality microstrip and stripline connections can be a daunting task. Add in the requirement around the time of flight for a typical memory bus or other family of high-speed connections, and you can spend considerable time sorting out that nest of interconnections.

As PCB designers, we go to great lengths to meet the requirements for additional air gaps around transmission lines. Isolating one trace from another becomes more important as the overall length of the traces grows. Crosstalk is a function of how far two traces run parallel to each other at a given distance apart. So, ultimately it is more than the minimum air-gap in play. The length of the boundary also matters.

With a number of connections that start in one general area and end at some other location, it's easy to picture a river of traces running from here to there. The variance in length between any of the routes is small compared to their total length. Any traces on the long side get pulled tight to minimize their natural length. From that point, the traces that end up too short get some meanders along the way.



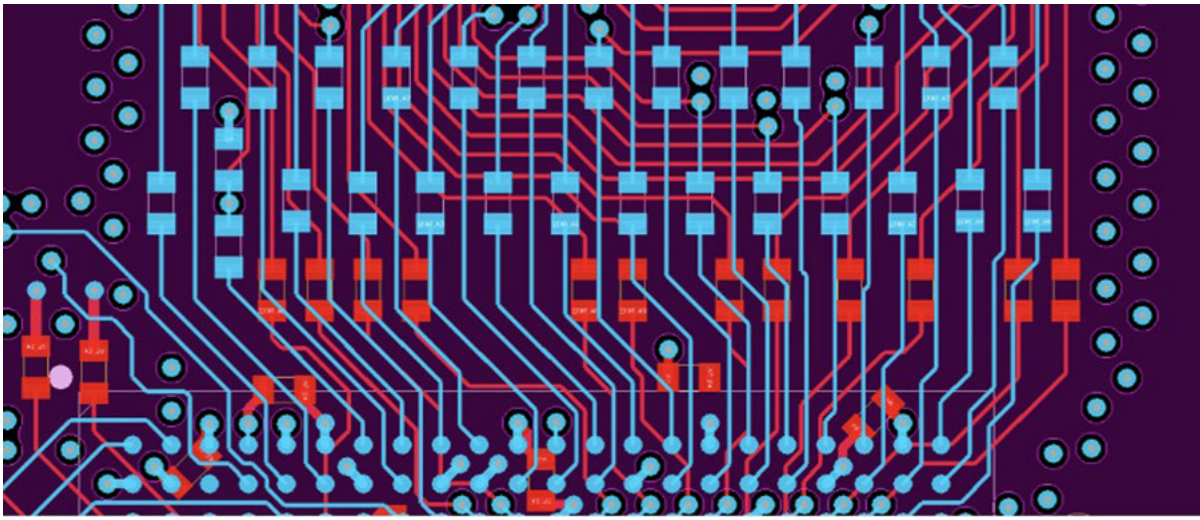


Figure 1. Flash memory data lines with series resistors routed on the top and bottom layers. (Source: John Burkert Jr.)

Differential pairs – A noise abatement program. It takes two to start a group and quite often, that's all it takes to form a group of PCB connections. So-called differential pairs exist when the duty of sending a stream of data is shared between two complementary traces. They generally run side by side as edge-coupled diff-pairs but can also be done using two adjacent layers using broadside coupling.

Either way, they are length-matched as best as possible to bring the two signals to the end of the route at the right moment. Generally, a symmetrical launch from pins and vias helps and is strongly recommended for avoiding an impedance mismatch. The idea behind differential pairs is that any transient noise in the vicinity of the signal shocks both lines during the instant the waveforms are transiting any specific location. Then we can recognize the difference between a high and a low logic state at a higher rate and over a longer distance owing to the noise immunity. That's what makes today's world go around.

Phase matching for differential pairs. Given there are two traces running along together, it's inevitable one will have an inside path through any bend. Depending on the data rate, that may be enough to get the two signals out of sync, especially if a bend to the left is not immediately canceled out by another to the right. In this case, it's not enough to match the total length. We compensate with a small bump on the trace that has the inside line keeping the signals running neck-and-neck the whole distance. When the rise times are that severe, it's best to minimize trace bends in the first place.

The thing about differential pairs is they like company. There's always more than one pair. Once we've solved inter-pair skew, we get to the intra-pair skew between respective data lanes. A general observation is that when there are fewer members to a match-group, the length tolerance budget is tighter. Something with between two and eight pairs is likely to require fine tuning with the data likely being serialized (**Figure 2**).

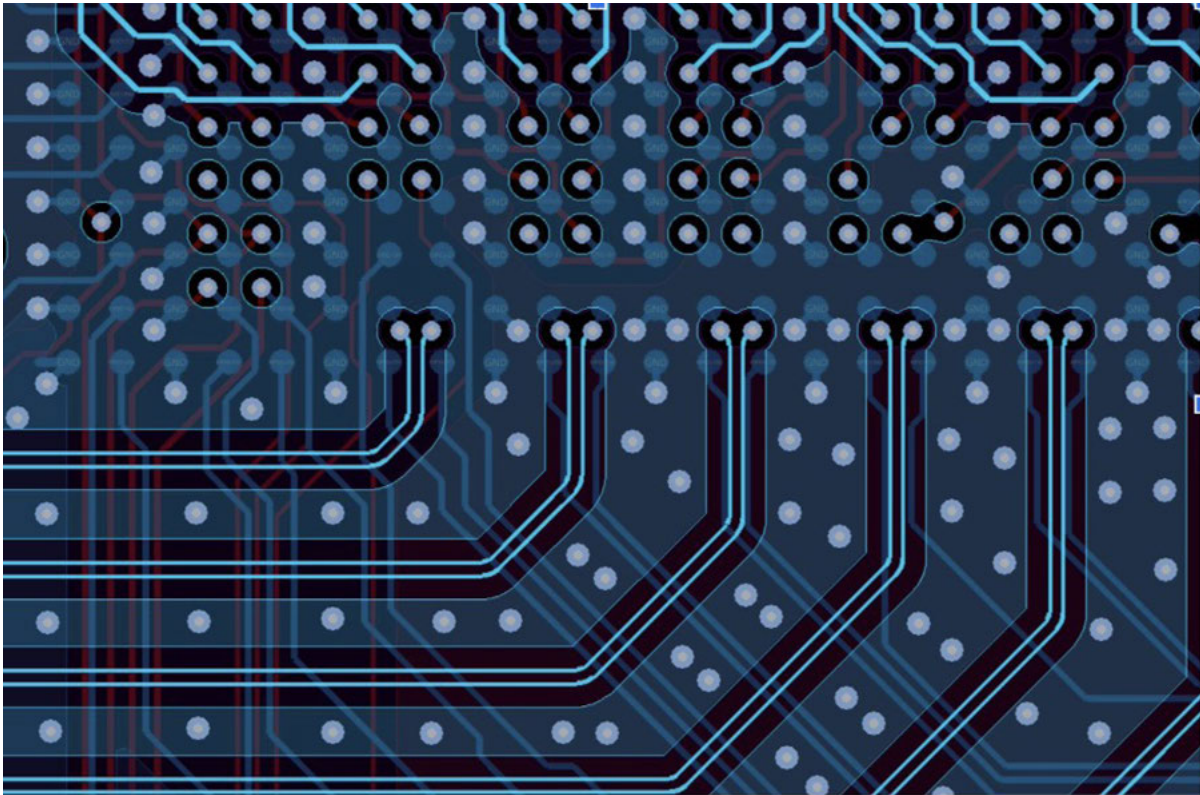


Figure 2. Differential pairs routed in separate channels for isolation. (Source: John Burkert Jr.)

That's not to say that a wide bus is necessarily going to have significant latitude on length matching. In many cases, the large number of group members is subdivided into data lanes of perhaps 8 or 16 bytes that are each under the aegis of a dedicated clock net. There can be a lot of clocks and they all want extra breathing room.

General length matching strategy. My process begins with generous length matching tolerances as a way to get the data lines into the same neighborhood as the clock. Once everything is close, you're not far from finding the length value that all the connections can meet.

Must all the lines in the bus be the exact same length? No, but if you start with that goal, you'll end up with a smaller spread. I try to center-cut the tolerance band to match all lengths if there is

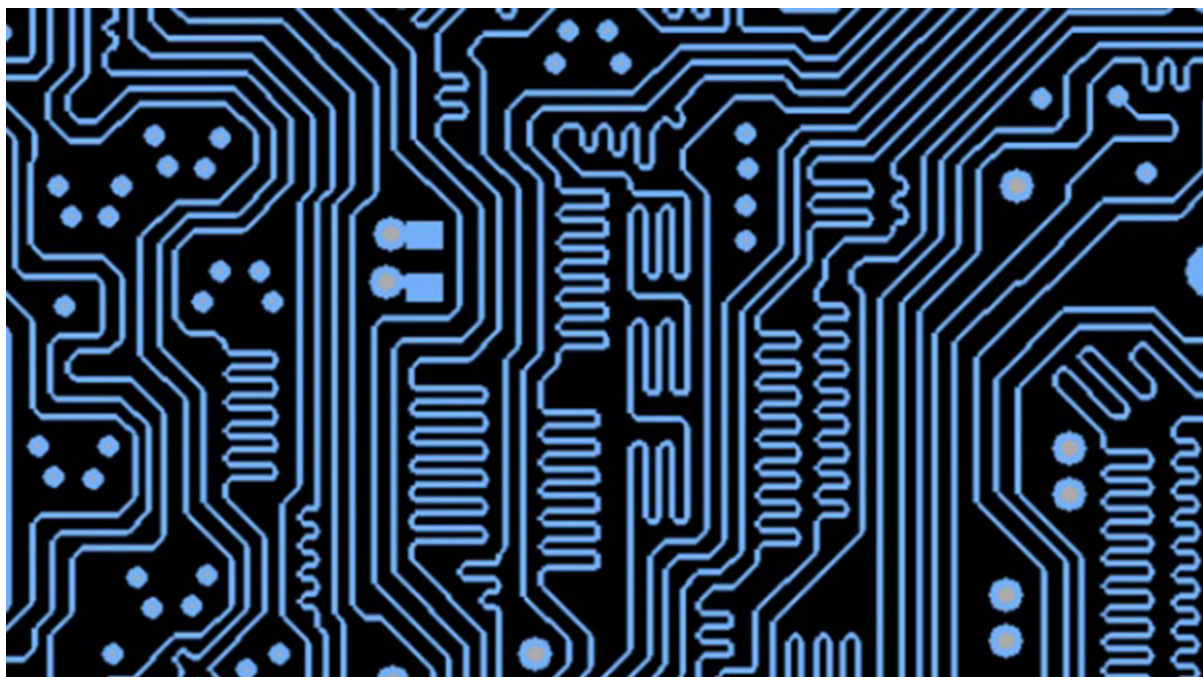
sufficient room. Otherwise, my clock is as short as it can be while just long enough to solve for the longest data line. That would be space efficient but also brittle, as some small bump could throw the length matching out of kilter. Matching them all on the money is more resilient and easier to defend in a design review.

Between LiDAR sensors, AR headsets and sat-comms, the number 128 has come up every time. They all had to convert 128 analog streams into digital representations. One used four big 32 channel ADCs while the others made do with 16 ADCs that had eight channels each. Automotive, defense or space: all had to be hardened for tough environments. In each case, the better we could do in hardware, the less work for the processor. There are applications with two or four times this many lines. Let me know if you've heard of any buses with over 512 members.

In terms of the sensor, the single-ended inputs exited the ADCs as differential outputs and had to be tuned to the point of eliminating variance. Studying the layouts prior to fan-out and coloring the nets that appeared to be the long tentpoles is step one. Giving those long traces priority during routing is the forward-looking strategy.

Other traces to look out for are the ones that run along the outside of the bus. Those lines define the space taken by that particular bus. As much as possible, it pays to create a guard band to separate the group from the outsiders. The space within must permit all the meanders for the present conditions and some wiggle room so that a minor design update with "one more via" doesn't break the design

(Figure 3).



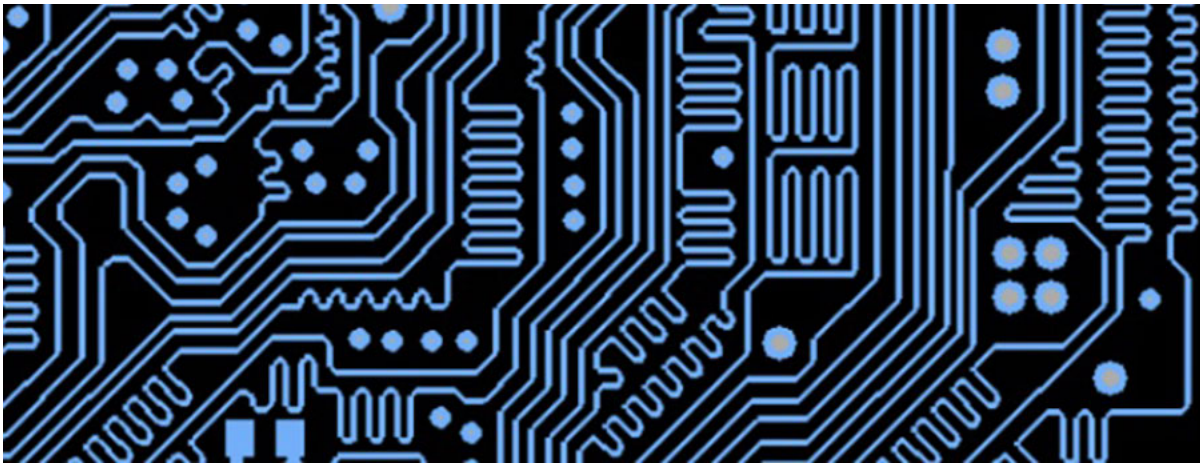



Figure 3. The telltale foursomes of vias (at left) that transition the differential pairs while the right side had the dense meanders that I would caution against if you have any choice. This was a case of severe mismatch. (Source: John Burkert Jr.)

What does success look like? After a routing study or two, the most natural and elegant solution should come into view. Nothing is perfect, and even if it is, there will be reasons to chip away at the board space until it becomes a concern. So, when the traces are escaping the big device or some other pin-field, a few close encounters are unavoidable. Being mindful of the crosstalk; the closer the elements get, the sooner and more they need to diverge.

A clean bus looks undisturbed with an almost hypnotic neural procession of connections. The fan-out may not be symmetrical, but the underlying connections go from station to station with no further crossovers or layer changes. The turns are few and purposeful. The spacing prevents ground pour from getting into recesses where no support via can tie it down. The balance of copper and air across the bus is optimized to isolate the maze of lines. The warts are few and have been considered acceptable.

No plan survives contact with the supply chain. Iterations will come from the development team, so always be ready to rip up your best work. Whether driven by simulation results or the endless supply-chain drama, we often have unscheduled work to do – and on short notice. If you're a player in this game, you should recognize the trend. A board that meets the requirements in the digital realm relies on good routing techniques. Use those and produce acceptable results quickly.

One way to get a leg up on co-development is to dig into the constraint manager and make it do some of the work – and verification – for you. From experience, it gets harder to remember

everything as the years stack up. Memorializing the design rules so you know how much you can alter them and stay within the specification will help the future version of yourself. Do that person a favor; capture the design intent. 

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

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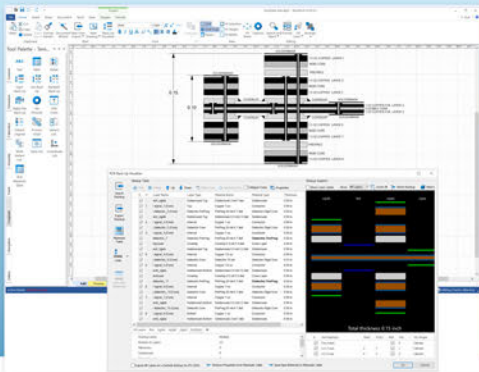
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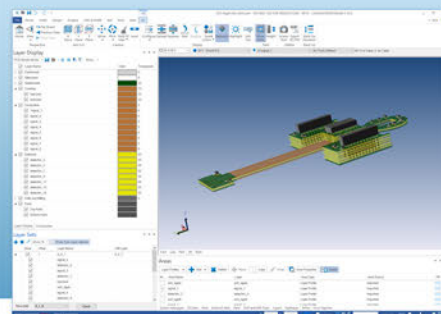
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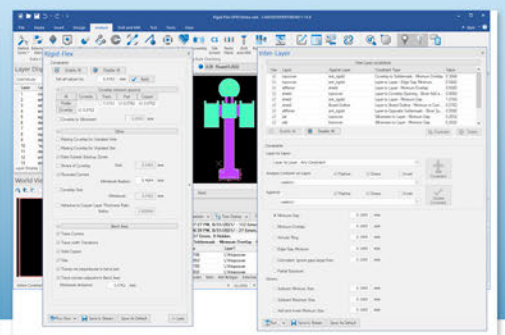
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The Importance of Design Constraints

Create them in the front end and push them into the back.

DESIGNING TODAY'S COMPLEX printed circuit boards is no easy task. Meeting electrical and physical design requirements can be daunting as you attempt to address layout solvability, performance and manufacturability so that version one works. Unraveling the design requirements and successfully inputting them as design constraints is key to achieving success in printed circuit board (PCB) design, as the design constraints are the rules that govern the entire design of the PCB from an electrical and physical perspective. Setting up constraints according to the design requirements as received better enables you to use automation to your advantage during the layout phase. Design constraints enable you to design quality into the PCB rather than checking for quality after the fact – and designing faster with better quality is the ultimate goal.

First, let's understand the power and advantage of establishing and using constraints when designing PCBs. Design constraints can be created and entered either during the creation of the schematics (at the front end) or in the PCB layout (at the back end). The best practice methodology is to create them in the front end and push them into the back end. It's important to note that the flow of how they are governed and annotated is bidirectional between the front and back end. It's up to the designer to establish and control the flow regarding which direction of the annotation has priority over the other.



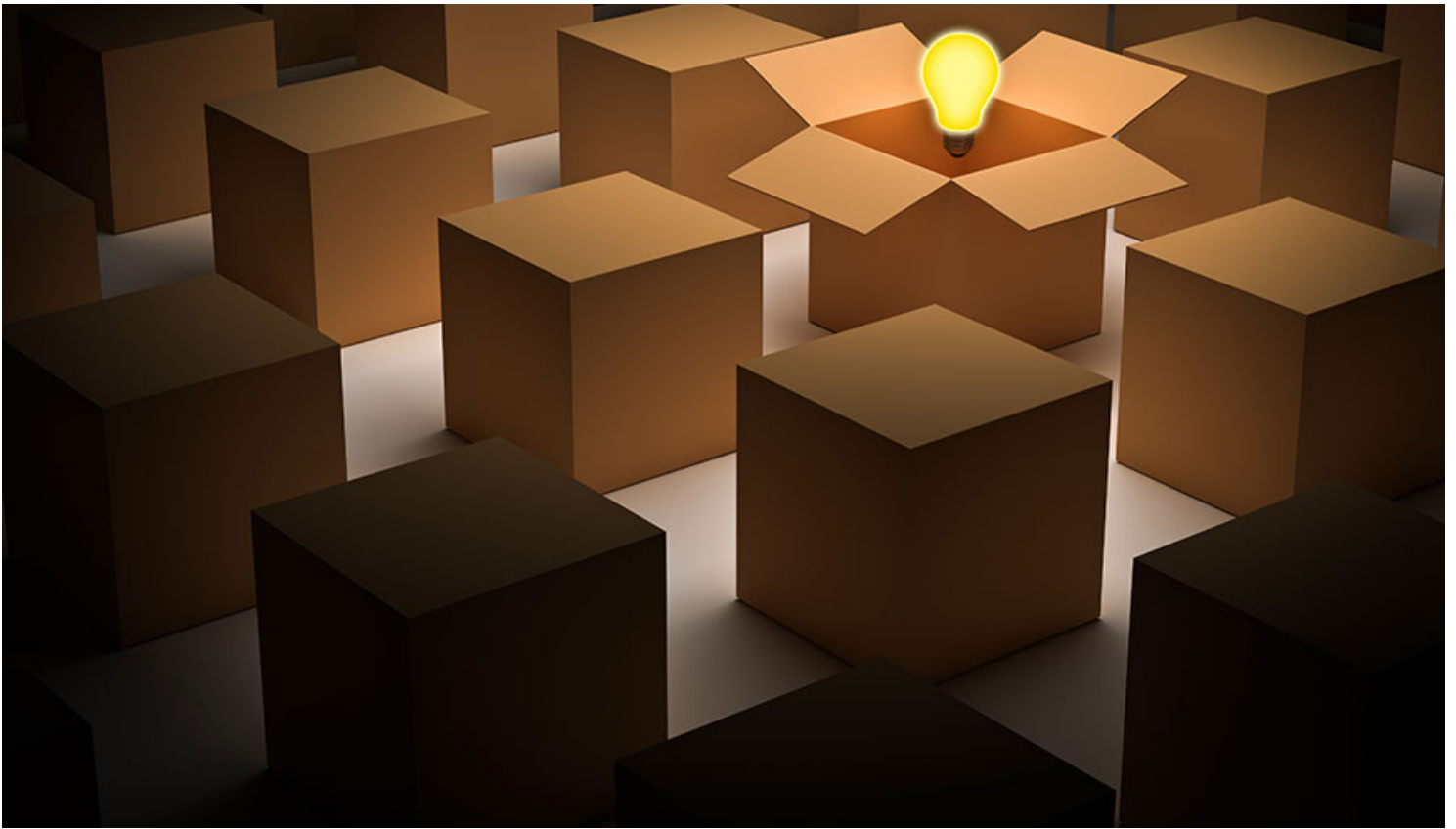


Figure 1. Proper use of constraints won't leave you boxed in.

Setting up design constraints can range from a simple task to a very complex and exhausting task depending on the complexity of the design intent. Knowing the time and diligence spent upfront establishing the design constraints pays off significantly during the actual layout effort. Within the design constraints manager tool, the rules that govern the electrical and physical details of the design can be controlled and established.

A few examples of details that can be controlled are the PCB stackup, trace spacing, trace width, layer trace length/delay matching and differential pair assignments. Once the design constraints are validated and locked in, they can be exported and reused in other designs, similar to other reusable items in the library function. As electronic components become smaller and more sophisticated, PCB design constraints become increasingly crucial. Let's explore the key constraints that designers must understand and employ to ensure success in the PCB design process.


The first key to success in PCB design is designing for layout solvability, especially regarding size and form factor constraints. Miniaturization and sleek designs are the trends in electronic devices. Designers face the challenge of fitting an increasing number of components into smaller spaces while maintaining optimal functionality. Form factor constraints dictate the physical size and shape

of the PCB, impacting the overall dimensions of the end-product. Component placement will dictate the quality of the routing. The arrangement of components on the PCB and the routing of traces plays a crucial role in the overall performance of the circuit. Designers must optimize component placement to minimize signal paths, reduce noise and ensure efficient signal flow.

The second key for success in PCB design is to design for the performance of the PCB, specifically regarding signal integrity, electromagnetic interference (EMI), power integrity and thermal management. Design constraints play a key role in solving for this. Maintaining signal integrity is paramount for the proper functioning of electronic devices. Factors such as impedance matching, signal propagation delay and crosstalk must be carefully managed. Designers need to consider the type of signals, transmission lines and routing techniques to ensure the reliability of data transmission. Adding to this is power distribution. Efficient power distribution is critical for the reliable operation of electronic components. By utilizing design constraints, designers must balance the power requirements of different components, manage power plane distribution and minimize voltage drops to prevent performance issues and ensure stability. Addressing thermal management is a part of this perspective that cannot be overlooked. As electronic components become more powerful, heat dissipation becomes a significant concern. Thermal constraints involve designing effective heat sinks, ensuring proper airflow and placing components strategically to prevent overheating, which can impact performance and lifespan.

The third key to success in PCB design is designing for manufacturability. PCB designs must be manufacturable at scale and within budget constraints. Highest yield at the lowest cost is the goal. When creating and implementing design constraints, designers need to consider factors such as manufacturability of components, assembly processes, and the choice of materials to ensure cost-effective and efficient production. Knowing and understanding the engineering decisions made at the point of design and how they will affect downstream activities in manufacturing is vital in the quest for PCB design success.

Industry regulatory compliance must also be considered when creating design constraints. Compliance with industry standards and regulations is nonnegotiable. Designers must be aware of regulatory requirements related to EMI, electromagnetic compatibility and safety standards to ensure that the final product meets legal and safety guidelines. Industry standards and guidelines such as IPC specifications provide helpful guidelines for PCB design.

In the ever-evolving landscape of electronic design, understanding the importance of PCB design constraints is crucial. Balancing the technical requirements with practical considerations is a continuous challenge for designers. By utilizing design constraints, you're better enabled to design quality into the board rather than simply checking for it after the fact. 

STEPHEN CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience and integrating the design-to-source Intelligence insights from Supplyframe into design for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association ([PCEA](#)); stephen.chavez@siemens.com.

Joined-up Thinking 2.0

AI factories could be the next step for smart manufacturing.

JOINED-UP THINKING is a concept that can deliver a multitude of benefits. Where there are many differing interests to satisfy, bringing together ideas and coordinating actions in a holistic approach can lead to a better outcome for all. Not the least, it can reduce duplication of efforts and resources, making processes more streamlined and cost-effective.

In practice, joined-up thinking is often difficult to achieve. Institutional barriers, differing priorities among stakeholders, and the sheer number and diversity of variables to evaluate and manage can conspire to thwart the best intentions.

Manufacturing is a complex sequence of events that demands substantial joined-up thinking simply to make it happen and see a result coming off the production line. Increasingly, however, this is not enough in the modern world. Numerous related factors must be considered, especially the environmental impact of our activities. Smart manufacturing has enabled us to address some of these issues, connecting the factory and IT domains and bringing manufacturing data into enterprise systems to enhance planning and historical analysis for continuous improvement. This is joined-up thinking 2.0, if you like.

We now have the opportunity to take a further step forward. Arguably, we must move in this direction if we are to answer the challenges we face today, ensure sustainability and address the current geopolitical issues that are likely to reverberate for years to come. It's time to make the leap from smart manufacturing to AI manufacturing. The power to be gained from this transition lies in extending the joined-up thinking, both backward into the supply chain as well as forward through

the entire product lifecycle to disposal and recycling or reclamation of materials at the end of life.



AI can be used to optimize product design, material selection and production processes to minimize environmental impact and promote sustainability.

AI can help us achieve this through its ability to evaluate and manage many more variables than humans or the traditional smart manufacturing applications could ever consider at one time. AI can analyze vast amounts of data in real time, making data-driven decisions to optimize processes at every stage. AI can consider all aspects of the product lifecycle, from supply chain and production processes to end-of-life scenarios. This holistic view allows more comprehensive and efficient optimization. Moreover, it can predict and prevent equipment failures, reducing downtime and maintenance costs, whereas smart manufacturing systems often lack such predictive capabilities.

Moreover, AI can dynamically adjust supply-chain operations based on demand, reducing excess inventory and optimizing transportation routes. Smart manufacturing typically focuses on production processes rather than the entire supply chain. Where smart manufacturing systems tend to focus on optimizing processes individually, AI can consider the entire business strategy to optimize production cost, quality and customer demand simultaneously. And we can use AI to optimize product design, material selection and production processes to minimize environmental

impact and promote sustainability.

It's just as important that AI gives us the power to adapt more rapidly than traditional smart manufacturing systems as political and economic conditions change, new technologies emerge and customer preferences evolve.


Right now, we are in the process of a major transition as companies are moving important manufacturing activities away from China and Taiwan toward alternative destinations. Southeast Asia is among the most popular choices, and Vietnam and Thailand especially. It's an opportunity for a fresh start that gives the chance to leverage AI extensively in designing new factories and shaping the manufacturing world to come.

It's easy to say and complicated to achieve. New tools are emerging, however, that can enable the transition to AI manufacturing. The more sophisticated use of digital twins is one development we can see happening now. I was recently introduced to the work of Elsyca, which is bringing AI-powered innovation into electrochemical processing by creating tools that will deliver benefits all the way from product design to setting up factories, before any product design or process configuration begins. At the EIPC Summer Conference this June, a delegation from Elsyca introduced their tools for copper balancing and electroplating that can increase PCB manufacturing yield, leading to greater efficiency and reduced materials wastage as well as improving electrical performance.

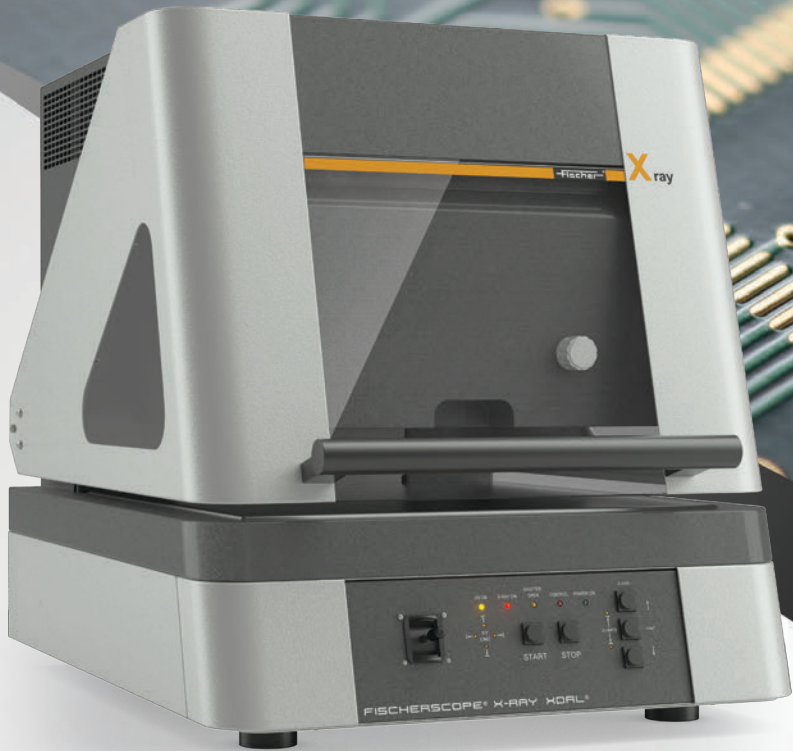
Other exciting developments are in the pipe, such as the work of companies like Nvidia, with its Omniverse platform and Isaac robotics simulator. Foxconn is among the companies that have spotted the opportunities these frameworks can offer to create efficient and adaptable buildings and factories, as well as products and services. Isaac lets you simulate industrial robots, including mobile robots such as AGVs, and use modular 3-D assets to build a working environment and to study and optimize the entire system before committing to a project plan. Last month, Nvidia and Foxconn jointly announced their vision for an AI-powered future encompassing activities from building EVs to setting up AI factories using simulation to optimize workflows and operational efficiency and ensure high production and quality standards can be met before committing to deployment in the physical world.

An approach like this can quickly evolve into a framework that lets companies build and scale

manufacturing and configure supply chains to leverage an established template. They can also design and build new factories quickly and so adapt to changing economic pressures and political and market demands.

It's yet another exciting prospect that AI can offer us as we continue to work out its full power and ability to help us meet our needs. The joined-up thinking we often wish for, in everything from planning services to managing transport infrastructures and distributing energy, could soon become far more pervasive and far-reaching than we ever imagined. 

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Flex Circuits, in Color

White mask is possible, but careful of overexposure.

I AM DESIGNING a flex circuit that will have LEDs in one area. I would like that area to be white in color instead of amber. What is the best way to do that?

Answer: A flex circuit can have a white outer surface, and this can be achieved in several ways. I will cover the different methods with the pros and cons for each.

Screen printing. For a “quick and dirty” solution, simply have that area of the circuit screen-printed with white ink (over the top of the standard amber polyimide covers). The downside to this method is that if you also want screened legend, a separate process using a contrasting ink color is necessary. Any LEDs must have clearance to ensure no ink ends up on the solder pads. This method will produce a white surface, but there may be rough edges and color tone variations. I would not recommend attempting any tight bend radius forming in areas with screen-printed ink. Some inks can crack if bent sharply, and if a crack forms in the ink it can, and probably will, propagate through the underlying polyimide film over time. And even if the cracks do not propagate through the polyimide film, the ink around the cracks will flake off and end up as FOD (foreign object debris) in the system.

Flexible solder mask. Depending on the application, white flexible solder mask may be a good option. Flexible solder mask comes in a wide range of colors, white being one (**Figure 1**). The process to apply white solder mask is exactly as any other color or type of solder mask. There is no learning curve unless very tiny openings in the material are needed. If you *do* have tiny features, the fabricator may have to perform some testing to determine printing parameters. White solder mask is more reflective than the standard green solder mask. This requires a balancing act to stay between fully exposing the solder mask, but not overexposing so that those tiny openings get even smaller or

disappear completely. Several colors of solder mask can require fine-tuning in the printing process to account for how the color pigments impact the UV light interacting with the unexposed mask.

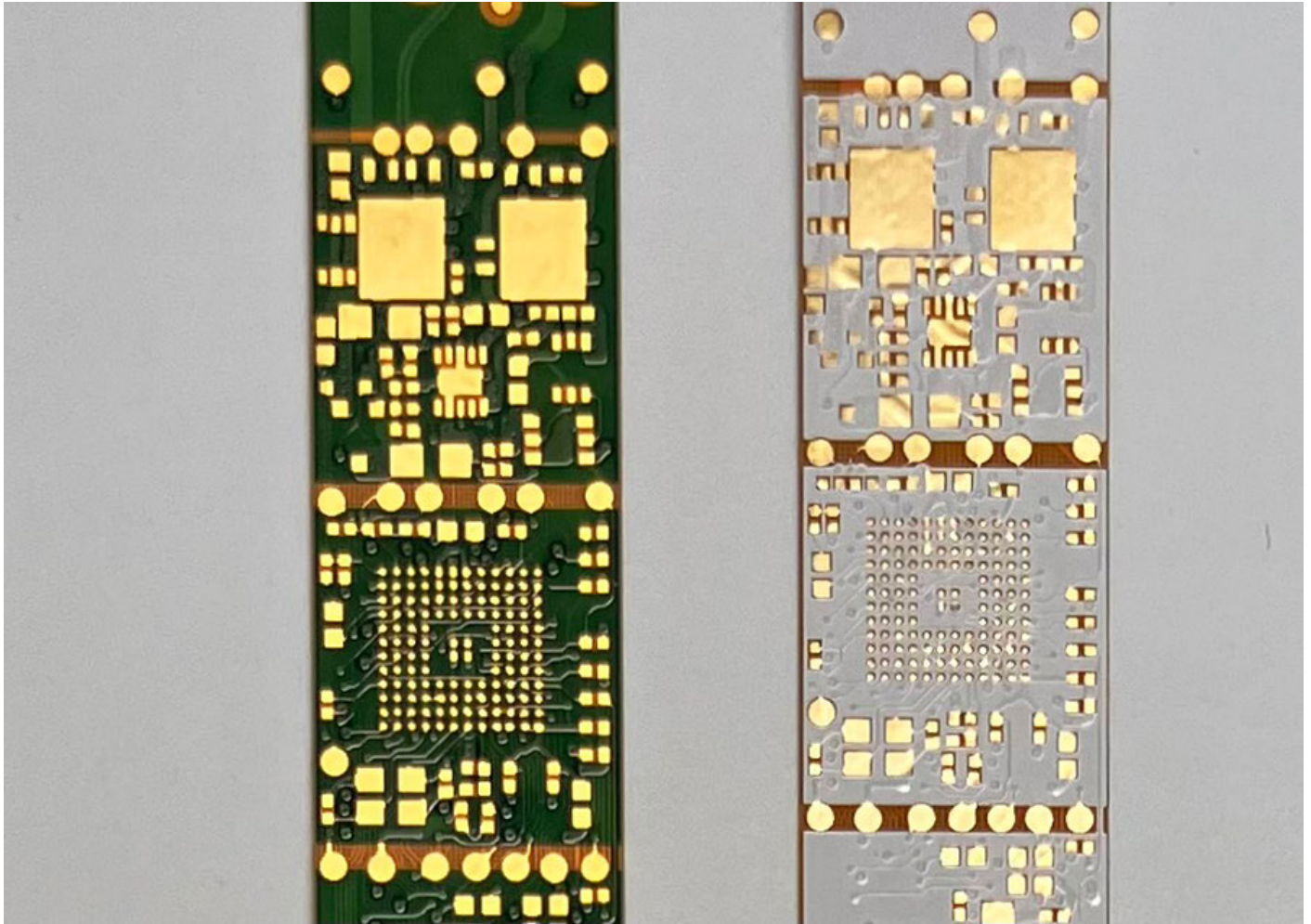



Figure 1. Flexible solder mask is available in a several colors including black, white, amber and green.

It is important to keep in mind that flexible solder mask is more flexible than what is used on rigid PCBs, but not nearly as flexible as a polyimide cover (which is a great segue into the next topic; more on that in a moment). *Do not* rely on minimum bend radius recommendations from IPC-2223, because those guidelines assume polyimide covers. If you try bending a circuit with flexible solder mask to a 10:1 bend ratio as IPC-2223 allows, the solder mask will almost always crack. I personally would like to see 100+:1 as a minimum bend ratio when using flexible mask. An option to avoid the bending issue is to use flexible solder mask *only* in the LED area since that area will most likely have some type of stiffener to keep it from flexing. Standard amber polyimide covers can then be used in the flexing areas. The solder mask/polyimide cover combination method will have a little bit of a cost adder but does give the best of both worlds.

White polyimide film. White (or black) polyimide cover film is available from multiple material suppliers. The downside is that this material is not used as extensively as amber polyimide, so it is a lot more expensive and may have a significant minimum order quantity (the MOQ can be more than 100 sq. m.) and longer lead times to procure it. Since the acrylic or epoxy thermoset adhesive that is clad to the polyimide cover film has a limited shelf life, manufacturers don't typically make a lot of it to put on shelves on the chance that it is needed. If volumes are such that you will be able to consume MOQ material inventories prior to the material expiring, white polyimide is a good option.

Any of the methods above do *not* have to be used on both sides of the circuit unless it is desired. Cost savings can be achieved if colored cover material is only spec'd in the areas that really need it, and is optional over the rest of the circuit. Still confused on the best method for your application? Have a quick chat with your fabricator. They can help you evaluate performance, cost, and lead time to help make the best choice. 

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How Many High-Current Vias Do We Need? (Fewer Than You Think)

The industry standard formula could triple the number actually required.

by DOUGLAS BROOKS, PH.D. and DR. JOHANNES ADAM

If a high-current trace on a board has a via going to another trace segment, the question of via size comes up. Conventional wisdom has always been that the conducting cross-sectional area of the via (or the sum of the vias) should equal or exceed the conducting cross-sectional area of the trace. The IPC standard, IPC-2152¹, formalizes it this way:

The cross-sectional area of a via should have at least the same cross-sectional area as the conductor or be larger than the conductor coming into it. If the via has less cross-sectional area than the conductor, then multiple vias can be used to maintain the same cross-sectional area as the conductor.

According to this wisdom, if the conducting cross-sectional area of a conductor is, for example, 540 mils² and the via *conducting* cross-sectional area is 37 mil², then we would need $540/37 = 14.6$ (almost 15) vias of that size.

Turns out, this is not true.

We performed a simulation² of a 120 x 16mm board with two 200-mil, 2-oz. traces on it carrying 14A. The traces were connected with 10-mil vias, each plated to a 1-oz. thickness. The cross-sectional area of a 200-mil, 2-oz. trace is about 540-mil². The conducting area of a 10-mil diameter,

1-oz. via is about 36.7 mil^2 . So, in this simulation, we would expect to see the need for approximately 15 such vias to have equivalence.

Figure 1 shows thermal images of the first three simulations³ with one, two and three vias. The temperature of the trace (without vias) is about 57°C in each case. The maximum via temperature for the single via case is about 82°C . The two-via case is considerably cooler, about 68°C . The three-via case is cooler yet, with a via temperature around 62°C .

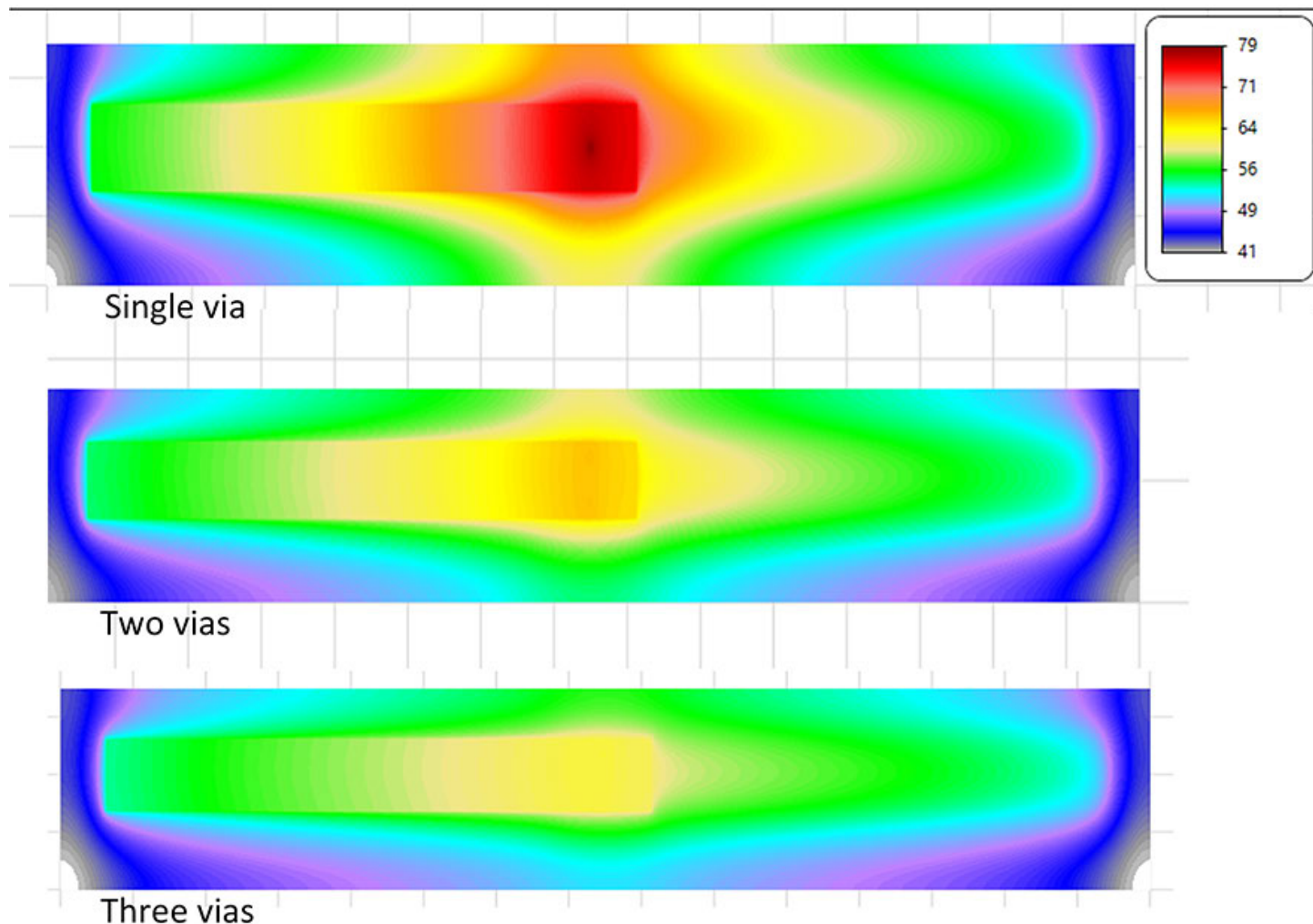


Figure 1. Thermal profiles (top view) of the simulated traces with one, two, or three vias.

Table 1 provides the data for all the simulations. **Figure 2** illustrates the via arrangement for the nine-via case. Via “top” is the top of the via on the top layer of the board. The “midpoint” is the middle of the via, internal to the board. Note the via temperature approaches the trace temperature quite quickly. But in this table is something even more important.

Table 1. Model Temperatures for Each Via Combination

Number of Vias	Via Temperature (°C)		
	Top	Midpoint	Difference
1	78.6	81.7	3.1
2	66.9	67.6	0.7
3	61.6	61.8	0.2
4	59.9	59.9	0
5	59	58.9	-0.1
6	58.6	58.4	-0.2
9	57.9	57.5	-0.4

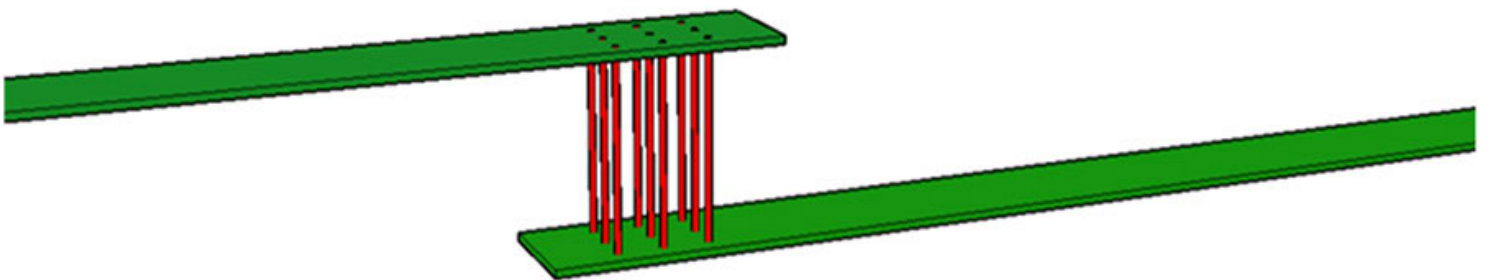


Figure 2. Via arrangement for the nine-via case.

We have noted in our book⁴ that when the cross-sectional area of a single via *equals* the cross-sectional area of the trace, the internal temperature (midpoint) of the via is *cooler* than the trace temperature. That is because the internal part of the via resembles an internal trace (while the traces themselves are external traces.) One unexpected result that IPC-2152 revealed was that internal traces are cooler than external traces because internal traces are surrounded by dielectric (which cools more efficiently than does the air), while only half the external trace area is in contact with the dielectric.

In Table 1, note that via tops are hotter than are via midpoints for up to three vias. From four vias on, via midpoints are cooler than via tops. This is shown in the third column of Table 1 and graphically in **Figure 3**.

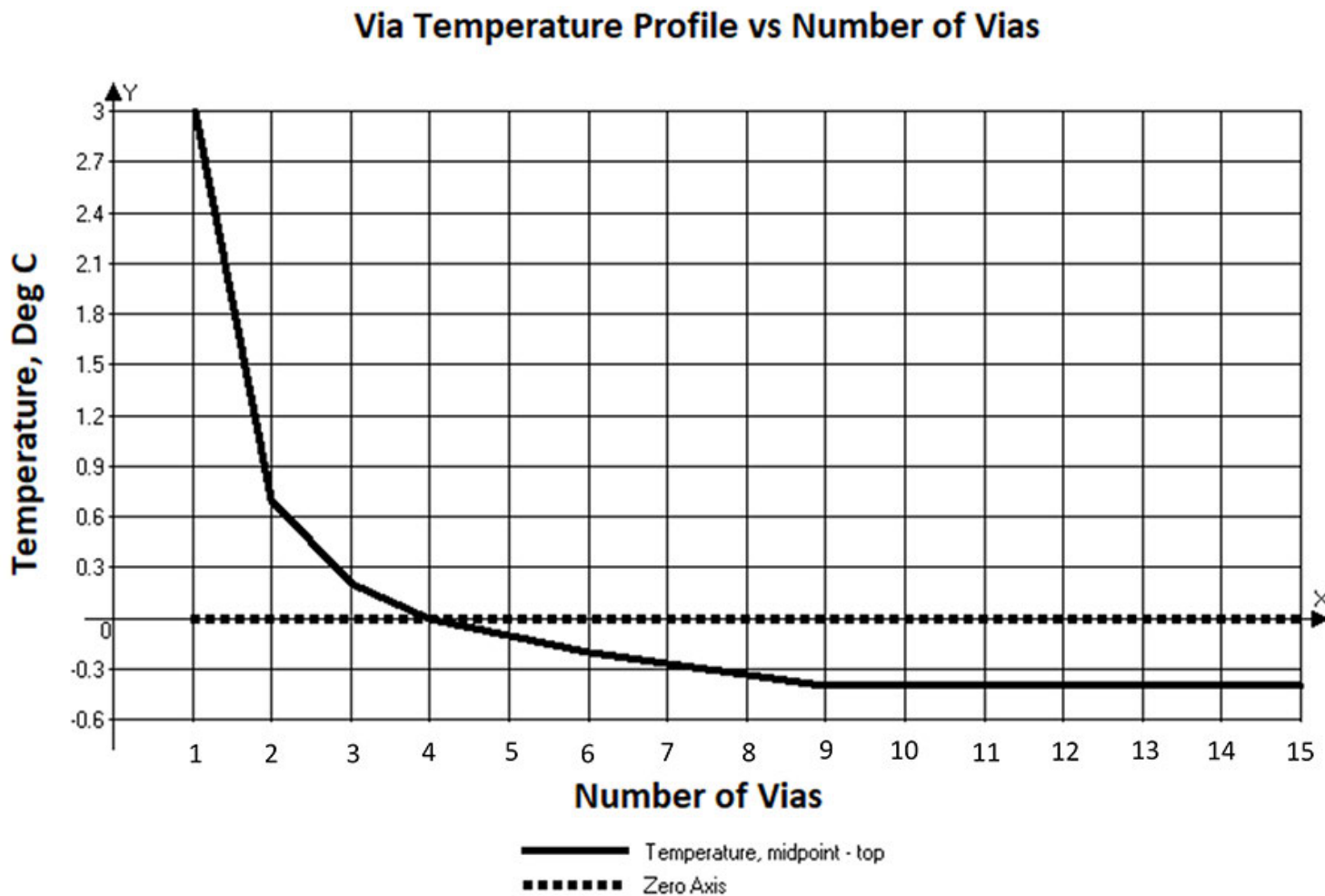


Figure 3. Difference in via top and midpoint temperatures as a function of the number of vias.

The cross-over point, where the via midpoint temperature is cooler than the top temperature, is approximately 3.8 vias. That is, 3.8 vias get us to a via temperature that is about equal to the trace temperature (at the via point).


Bottom line: Conventional wisdom says we need 14.6 vias in this situation. But the model suggests we need only 3.8. It is no coincidence that $3.8 = \text{the square root of } 14.6!$ The current divides approximately equally through equal-sized vias. So, the current through each of n vias will be approximately i/n . But the *power* dissipated in each via is I^2R (current *squared*). If we reduce the current in the via by n , the *power* (and therefore the heat) goes down by n^2 .

General rule: Let A_1 be the conducting cross-sectional area of the current-carrying conductor. Let A_2 be the conducting cross-sectional area of the via we are using. The total number of vias we need for equivalency is

$$\text{Number of vias} = n' = \sqrt{A_1/A_2}$$

Eq. 1

And this is a very conservative number. Recognize that even if we use one or two vias fewer than this, the via temperature will rise, but not necessarily to a dangerous level. This provides the opportunity for a *lot* more routing channels than conventional wisdom allows, saving us (perhaps) very valuable board area.

Technical aside: Do not confuse this model with the one we all learned in EE101 regarding the calculation of parallel resistance. There the relationship was $1/n$. But the parallel resistor model is a constant-voltage model and the resistors are the load. Here the model is a constant-current model and the via resistance is trivial compared to the circuit load. The models are entirely different. 

NOTES

1. IPC-2152, "Standard for Determining Current Carrying Capacity in Printed Circuit Board Design," IPC, August 2009. IPC was not alone in thinking this. Almost everyone in the industry thought the same thing.
2. We used a simulation program called TRM (Thermal Risk Management), originally conceived and designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation. TRM is available at <https://www.adam-research.com>.
3. The maximum "pixel" resolution and density in a simulation is determined by the smallest dimension in the X-Y plane. Via simulations require about one to two orders of magnitude greater resolution than "standard" trace simulations, placing a significantly greater load on the computer CPU and memory. For this reason, modeled board areas for via simulations are typically quite a bit smaller than would be the case for regular trace simulations. This results in a slight upwards bias in model temperatures from what might be otherwise expected. *Relative* temperatures within the model, however, exhibit much smaller upward biases.
4. Douglas Brooks and Dr. Johannes Adam, *PCB Design Guide to Via and Trace Currents and Temperatures*, Artech House,

2021 (available on Amazon.com). Chapters 8 and 9 cover vias.

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The PCB Podcast

Why Making All Transmission Lines in a PCB 50Ω is Good Technological Practice

Simplify the stackups and make impedance and other measurements easier.

by LEE RITCHEY

As many as seven different impedances are called out in various design specifications. Among these are:

- 33Ω for Rambus memory
- 50Ω for most high-speed logic
- 65Ω for the PCI bus
- 72-75Ω for analog circuits
- 85Ω differential for PCIeExpress (42.5Ω single-ended)
- 95Ω differential for USB (47.5Ω single-ended)
- 100Ω differential impedance for most high-speed Internet links (50Ω single-ended)

Successfully designing a PCB with more than one of these impedances can be difficult, if not impossible. The main challenge is designing a PCB stackup that has enough routing room for all the traces of each impedance while maintaining a manufacturable, economical product. A design that is all one impedance would be of great value. If so, what impedance would be the best? Here we

address this topic.

Where did all these impedances come from? It's helpful to have a sense of where the foregoing impedances came from. As seen below, their origins are diverse and the applicability of them are, in some instances, no longer viable. Below is the history of these diverse impedances.

Rambus started out making a memory system that was expected to deliver very-high transfer rates. The architecture was such that it was anticipated that the address and data buses needed to be 33Ω to function properly. The jury is still out on this, as this memory technology did not catch on, so we don't need to worry about designing this kind of transmission line into the stackup.

50Ω impedance. This has been the choice for high-speed computing since the outset since ECL and GaAs logic were employed. It matches the impedance of virtually all test equipment, making accurate measurements easy.

65Ω impedance. This was first specified for transmission lines on four-layer PCB motherboards and most game consoles. It was arrived at more or less by accident by measuring the impedance of a trace on a typical four-layer PC motherboard when it was determined that impedance control would be needed as speeds continued to increase. See Ritchey¹ for a more detailed treatment of this subject.

$72-75\Omega$ impedance. Originally, TV antennas were mounted on rooftops and connected to TVs using 300Ω twin lead transmission lines. This twin lead transmission line was not shielded, so it was susceptible to noise from the surrounding environment. A shielded coaxial cable was needed to solve this problem. Since building a 300Ω coaxial cable was impractical, a 2:1 stepdown transformer was used to "transform" the impedance down to 75Ω . Ever after, this impedance cable has been used by systems that have analog signals.

85Ω differential impedance. This was arrived at by engineers at Intel who determined that the bit error rate would be lower with an 85Ω differential impedance than with a 100Ω differential impedance. This has proved untrue and later in this article we show that differential impedances are not necessary in PCBs.

95Ω differential impedance. This impedance was derived by measuring a number of USB cables

and discovering that their differential impedance centered around 95Ω .

100 Ω differential impedance. The early Internet was connected by twisted pairs that were obtained from phone suppliers. Originally, the twisted pairs already in buildings to connect phones were used to connect PCs and other terminal devices to routers, switches and hubs. Because the differential impedance of these twisted pairs happened to be about 100Ω , this began to be widely used in the industry.

Observations about Differential Pairs Routed on a PCB

When members of a differential pair are routed over a plane on a PCB, the primary partner is the plane over which each signal is routed. In Ritchey,² it is seen that each side of a differential pair is, in fact, a single-ended signal parallel terminated in the single-ended line impedance. From this architecture came the idea that tight coupling is a good idea. The reality is just the opposite.

Tight coupling carries with it a number of negative side effects. Among these is that when one trace is routed very close to another one, each drives down the impedance of the other, requiring that the traces be narrowed to get back to the original target impedance, driving up copper loss. A further negative effect is that the traces cannot be separated to route through a pin field such as a 1mm pitch BGA without suffering very large impedance changes.

For those product developers who remain unconvinced there is no need to route differential pairs with a differential impedance and tight coupling on a PCB, tour any conference and look at the demonstration setups in many of the booths. Differential pairs will be connected with a separate 50Ω coaxial cable, often very far apart. All the energy spent trying to demonstrate some benefit to tight coupling has no real value. Designs we do every day with data rates as high as 32Gb/s are done to the “not closer than” rule to avoid unwanted interaction between the two members of a differential pair.

From the above discussion, it should be clear that each member of a differential pair, when routed on a PCB, is a single-ended signal parallel terminated in the line impedance and there is no benefit to tightly routing them to each other.

Selecting an Impedance

If it is possible to route all the signals on a PCB to only one impedance, what would be the best impedance to choose? From the above discussion, all signals routed on a PCB are, in fact, single-ended, even if their use is for differential signaling. Since all the test equipment we have available to make measurements is designed with input and output impedances of 50Ω and their connecting cables are 50Ω , it turns out to be a good target impedance.

Figure 1 depicts the simulation of a typical PCI driver connected to a 50Ω transmission line. **Figure 2** is a simulation of the same typical PCI driver connected to a 65Ω transmission line. As can be seen, there is very little difference in the signal, so designing PCI buses with 50Ω transmission lines is acceptable.

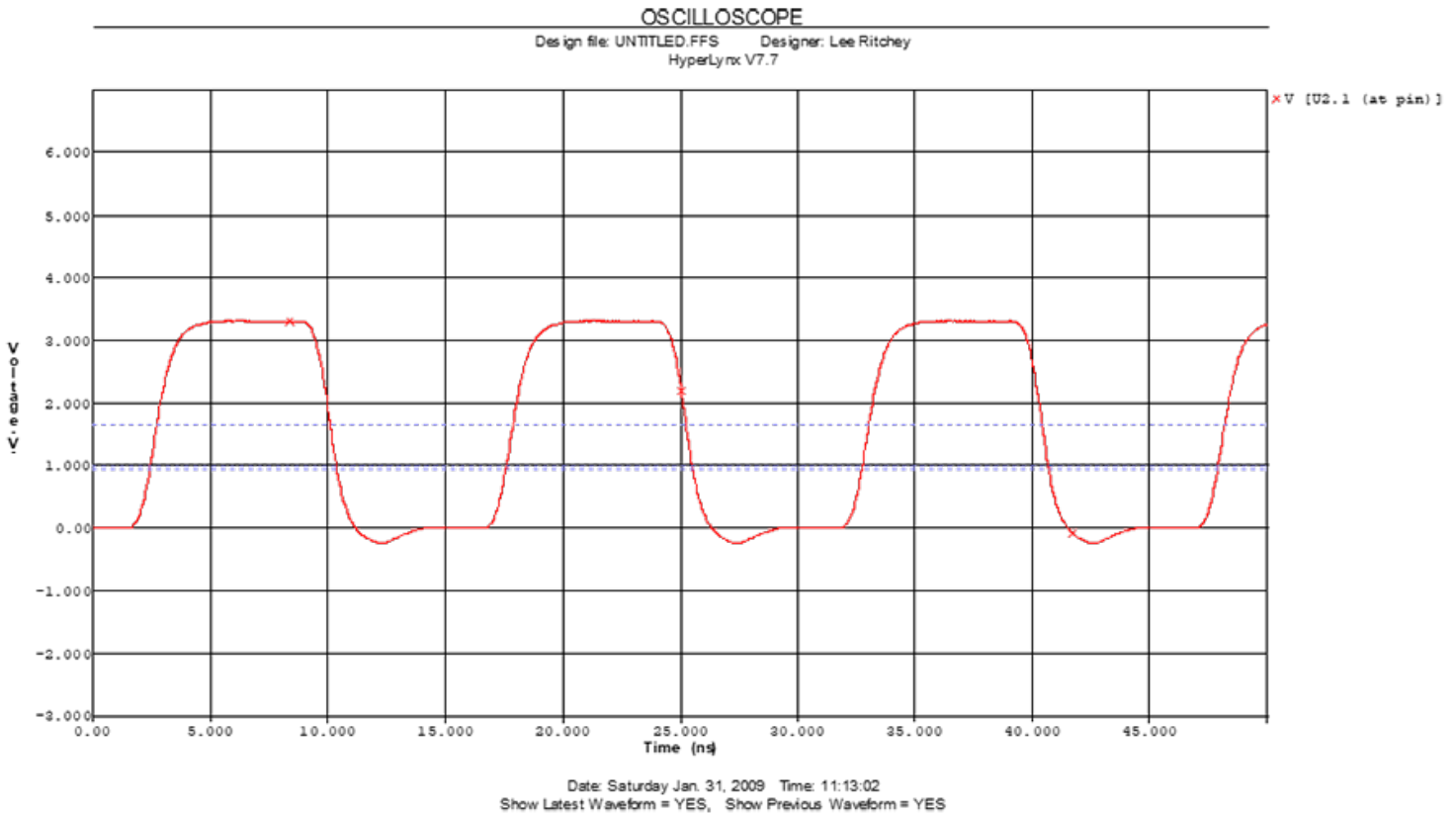
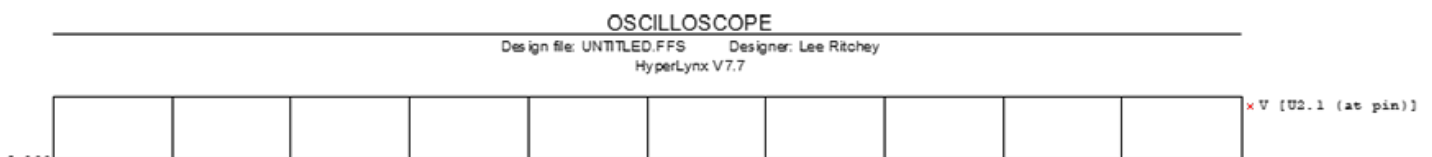


Figure 1. PCI driver simulation driving a 50Ω transmission line.



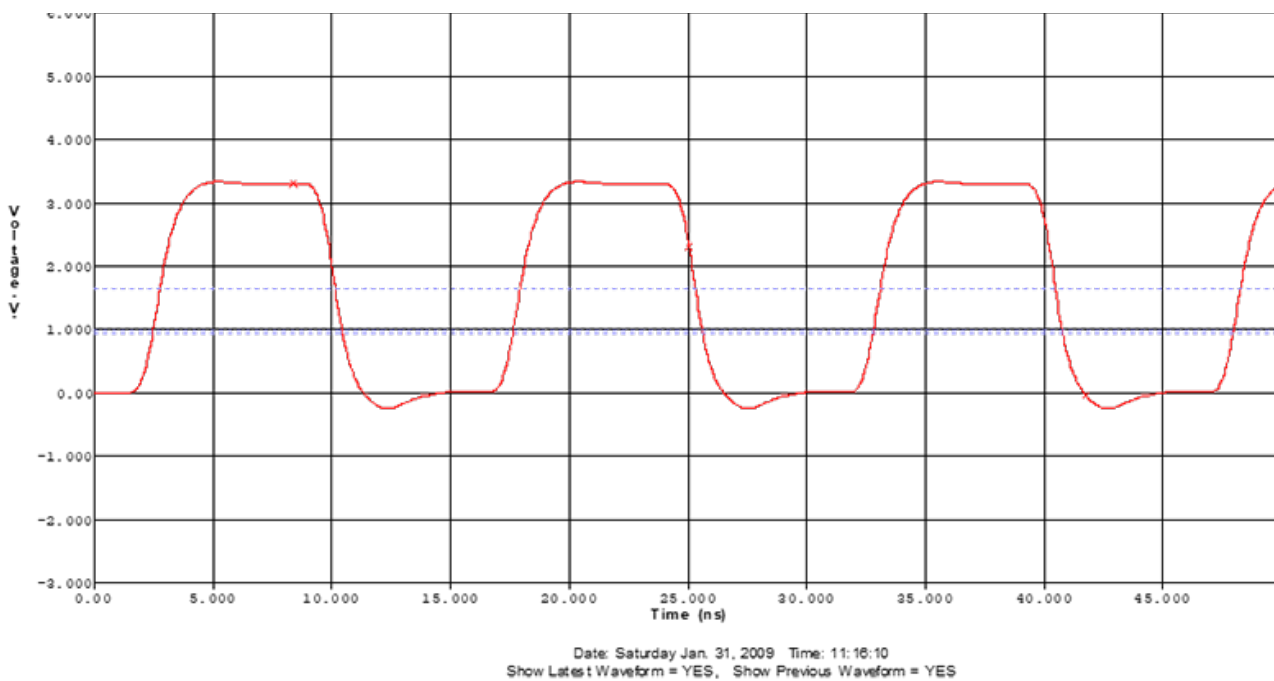


Figure 2. PCI driver simulation driving a 65Ω transmission line.


The primary application of 72-75Ω transmission lines is driving or receiving signals from an outside signal source such as a TV or some antenna. These signals are nearly always terminated on a device at the edge of the PCB. The length of the connection is short. If this connection is done with a 50Ω trace, there will be an impedance discontinuity. Rarely will this short discontinuity result in a significant degradation of the signal. If there is concern that this discontinuity will be a problem, simulation of the signal path with the two different impedances can be done. Rarely will this turn out to be a problem. As a result, 72-75Ω traces are not necessary.

The 85Ω differential impedance is really two 42.5Ω single-ended transmission lines. As noted earlier, this odd impedance is of no benefit, so routing these nets as two 50Ω lines is acceptable and, in essence, preferred.

The 95Ω differential impedance, which is two 47.5Ω single-ended lines in the USB standard, has a tolerance of +/-15%. Using this tolerance, the single-ended impedance can range from 40.375 to 54.625Ω, so a 50Ω transmission line will satisfy the standard.

Earlier it was pointed out that a 100Ω differential impedance is achieved by using two 50Ω single-ended transmission lines. Designing a PCB stackup using only 50Ω transmission lines greatly simplifies the process and also ensures that verifying the impedance is correct at the end of the PCB production line.

Conclusion

All the high-speed protocols listed in this article, except Rambus, can be successfully implemented using 50Ω transmission lines. This greatly simplifies designing PCB stackups and makes impedance and other measurements easier. 

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3. Lee Ritchey, "Is Tight or Loose Coupling Best for Differential Signaling?" PCD&F, March 2020.

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'A Good First Step'

PCBAA's executive director lauds recent funding wins but says the heavy lifting remains.

by MIKE BUETOW

Year-end is typically not the time when big announcements are made, but the news came fast and furious in November as [TTM Technologies](#) and [Calumet Electronics](#) both announced plans for new factories. Coupled with the opening of [Schweitzer Engineering Laboratories' new fab in Idaho](#) and the not-so-secret plant [Starlink is building in Austin](#), one would have to return to early 2001 to see this level of PCB construction in the US.

All this new activity happily coincides with the efforts of the Printed Circuit Board Association of America. The fledgling trade group, which was founded in 2021 to advance US domestic production of PCBs and base materials, has been rallying federal legislators for attention – and funding – to ensure an onshore supply chain for domestic electronics.

We spoke with PCBAA executive director David Schild in late November on the [PCB Chat podcast](#) on the latest legislative and industry developments. Excerpts:





Mike Buetow: Much has happened since we last spoke in July. The big news this month is a couple of major investment announcements by your members, one in Michigan and one in New York.

David Schild: Absolutely. Our industry continues to demonstrate an ability to invest in itself and to lead in innovation. We know that in addition to the next-generation semiconductors that are going to be made with Chips Act money in places like Ohio and Arizona, we're going to need next-generation PCBs and next-generation substrates to form a next-generation electronics stack. There's been some really good announcements in recent weeks demonstrating our industry's commitment to the technologies we'll need to power the future, to borrow a phrase. You mentioned a couple of them: first in Calumet, Michigan, Calumet Electronics partnered with the Michigan Economic Development Corporation to expand their capacity in the field of organic substrates. It's going to mean millions of dollars – I think about \$7 million in capital expenditures – 80 new jobs in the Upper Peninsula, and certainly a critical capability when you talk about organic substrates. Also, we see from TTM an announcement that in the state of New York they're going to spend nearly \$130 million to expand their Syracuse facility and the ability to produce ultra-high-density interconnect PCBs, another next-generation technology that we critically need. Finally, going back to Calumet, an exciting announcement that the US Defense Department, under the Defense Production Act accounts, is going to contribute almost \$40 million for defense-specific printed circuit boards to be built at Calumet.





PCBAA executive director David Schild

So what you see there is investment by the government, the Department of Defense, and the state of Michigan understanding that we have to build out the entire microelectronics stack. But you also see private sector commitment. You see these companies stepping up and saying we will break ground, we will engage in greenfield initiatives, we will invest in next-generation technology, and I think it demonstrates that the PCB and substrate industries in America are not sitting still. This is great news. Of course, I have to caveat that while this is a good first step, as the Chips Act was, this does not go far enough to reverse the slide we've seen over the past 30 years. (The US) used to have 2,200 board companies and now we have something like 150. We used to have 30% global market share. Now we have something like 4%. To reverse that slide and build truly resilient and secure supply chains, it's going to require government policy and investment to the tune of billions of dollars. While the millions we saw (in November) are a great first step, we need things like the PCBs Act, increases in funding for the Defense Production Act accounts and those appropriations. I think we need to see more tax incentives to buy American when it comes to microelectronics.

MB: When we spoke last, industry had just sent a letter asking for \$100 million in the next budget toward onshore PCB and IC substrates technology development. And they were specifically targeting the Defense Appropriations Subcommittee, if I remember right. As you noted, the Calumet award was, in fact, provided by the Defense Production Act. Can we say that approach worked?

DS: I would say the DPA account has been used to a limited extent to support the industry. If you look at the amount of money allocated versus the expenditures, they don't match up. My view is that one of the reasons that the appropriations committees cut the DPA account this year is because their feeling was perhaps the money was not being spent fast and efficiently enough. A great team of people at the Pentagon are committed to the supply chains that power everything that our men and women in uniform use. They understand the critical role of microelectronics. We have folks on Capitol Hill who similarly want to fund the DPA account. I think there's a little bit of a mismatch and that's why we've been on Capitol Hill consistently this year with the partnership of IPC to say, "Don't cut the DPA accounts." That's our message to Congress and the Pentagon: Spend more

robustly and more quickly inside of the accounts because the need is now.

MB: Does that suggest that some funds remain on the table to be allocated in the right situation, or was the Calumet award essentially the entirety of what was available for the current fiscal year?

DS: There's still money on the table and obviously these are not simply blanket awards; they're targeted at specific technology sets and specific programs and specific critical needs that the Department of Defense has identified. You need to have a specific plan and you need to be meeting a specific DoD requirement to seek out these funds. That's what Calumet did. I don't think this is the last domestic PCB or substrate company you're going to see receiving an award, and of course there's a whole microelectronics ecosystem beyond boards and substrates that the DPA can be used to fund, but I think many more companies that could contribute to that ecosystem could apply for funds, and I think that demand signal would probably overwhelm the amount of money that's currently available. We need to work out this disconnect between Congress and the Pentagon first to make sure these accounts are funded at the appropriate levels and consistently year-over-year. Then I think we can pivot and engage with our customer at the Pentagon and say, "OK, how do we make sure that this is getting out the door quickly getting to industry quickly as you know these are not technologies that get developed overnight, right?" There are months or sometimes years of lead time to build circuit boards and substrates that will work with next-generation chips but also in the very dynamic environments that you find in the national security arena, so I think the time to act is probably now and you know we're talking to both the executive and legislative branch about what needs to be done.

MB: Is it within the realm of possibility that monies allocated by the Chips Act could be used almost on a pass-through basis to help support supply-chain companies that are trying to build products that then would be part of the chips ecosystem? For example, an Intel or a Micron could receive funding that then would be used to help boost technology development at the IC substrate level with a partner company?

DS: Mike, this is such a great line of discussion because obviously our association launched in the midst of the fight for the Chips Act. The semiconductor industry has been well-organized, well-funded and focused on the goal of government support for a number of years. The Chips Act took

almost five years from the time it was conceived to the time it was signed on the President's desk, and the money still has not begun flowing. There is money from the Chips Act that goes to the Department of Defense. A great deal of money – almost \$52 billion – is designed to be allocated. We are just starting to see funding guidance from the Department of Commerce and we are just starting to see some of the initial awards.

The way Congress wrote (the Chips Act), the language is interpreted to mean semiconductors. I think you are seeing a recognition at the Department of Commerce under Secretary (Gina) Raimondo that we need an ecosystem. She uses the term “manufacturing nodes,” and I think what she is envisioning is a chip fab surrounded by a test facility surrounded by raw material suppliers surrounded by board and substrate manufacturers. It has not been articulated exactly that way, and we have let them know that we're part of the ecosystem. My sense is that this money will be allocated over the better part of a decade and that the first people to (benefit) be the world's largest semiconductor manufacturers – the Intels, the Microns, the TSMCs.

At some point we think that a reinterpretation or another look at the Chips Act and where the money is going would be a good idea by both Congress and the administration. But right now, when you look at the guidance documents that detail how you can apply for Chips funds, they do not seem to carve out a space for board and substrate manufacturers.

MB: The TTM announcement in New York looks more like a partnership between the company and the state rather than the federal government. Does PCBAA get involved at the state level?

DS: We are primarily federally focused at the moment. My view is that eventually we have to start getting the message out into the states, and we've talked with economic development corporations and even mayors all over the country about what increased manufacturing of PCBs and substrates would mean. You are seeing states move very quickly on the heels of the Chips Act; New York, Arizona, Texas, California, Ohio, Illinois: these all come to mind when it comes to incentives. New York and Michigan are partnering with some of our member companies to say, “How can we speed the process of construction? How can we help you with workforce issues? You know what incentives are available on the ground?” That's what the Michigan Economic Development Corporation did with Calumet. And TTM and the state of New York have a very positive

relationship.

The remedies we're looking for, the billions of dollars of direct funding and tax credits, are being sought at the federal level. We want them to apply across the country to anybody within the contiguous borders of the United States who is doing this sort of work. Our 44 members come from all over the country. Once we have run that process, and it's probably a process that will continue to run for many years, we will have to branch out and start thinking about state initiatives. But don't sleep on what state and local governments might be offering as well.

MB: Along those federal lines then, the Protecting Printed Circuit Boards and Substrates Act of 2023 is in committee and has seven cosponsors.

DS: I'm glad you brought this up. There's really three major policy initiatives that we're tracking. The first is this idea that the Defense Production Act is a hunting license, and that we have to have bullets in the gun in the form of appropriations funding. I mentioned the fact that the DPA account was cut for fiscal 2024. We are trying to get those cuts reversed, and have money added to the DPA account. We talked about how just in the last few weeks you've seen almost \$40 million flow into Calumet from that account. There's more that could be done, so that's one policy priority.

The second would be the continued defense of provisions in the National Defense Authorization Act, or NDAA, that calls on the Pentagon to look inside its commercial off the-shelf supply chain – its COTS technologies – and (locate) microelectronics from restricted countries that we do not want to do business within the defense arena. The Pentagon has agreed that by 2027 they will have a plan to look inside those supply chains and make sure everything is trusted and sourced accordingly. I think that's a great opportunity for American manufacturers beyond the ITAR market, where we obviously provide critical technologies today. Because it's a 2027 implementation, we have to keep it sold. We have to play defense and make sure that is in every successive NDAA for the next several years.

Finally, there's the Printed Circuit Boards and Substrates Act. Now we have a House version of that bill championed by Congresswoman Anna Eshoo and Congressman Blake Moore, with bipartisan support growing on both sides, we need a Senate companion, and I have spent a lot of the last few months going directly to the US Senate and doing a lot of education. What are PCBs and substrates? Why do we depend on them? Why has this supply chain gotten a little fragile and a little thin and

what can we do to reverse it? We need a similar bipartisan bill in the Senate. Most probably don't realize there was a Chips bill in the House and there was a Chips bill in the Senate. They reconcile those differences in what's called the Conference Committee. It eventually goes to the President's desk. Legislation is a long road. We have our House bill. We need our Senate bill. So that's really our third leg of the legislative stool.

MB: Any early indications as to who might be a co-sponsor on the Senate side?

DS: I'm going to reveal that when we feel like we have commitments. I will say we've gotten very positive feedback from Democratic and Republican senators. Both sides of the aisle seem to understand this is a real issue related to economic security and national security. Nobody's ready to put their name on the bill quite yet, but I can tell you they're looking at the House legislation. They're looking at where their constituent interests lie, the states where we manufacture these technologies and have a vested interest, and I'm optimistic that very soon we will have a Senate companion bill. We will move forward then to advance both in both chambers.

MB: What would you recommend the industry do insofar as trying to directly encourage their legislators in favor of restoring the cuts to the DPA, signing on to the Printed Circuit Board and Substrates Act, getting on board with getting one introduced in the Senate and so forth?

DS: There's two things that industry can do. The first is to assist us in our educate part of the "Educate, Advocate, Legislate" mission. What I mean by that is, engage with your local Chambers of Commerce, engage with your state economic development authorities. Invite your local Member of Congress, invite your governor, invite your state representative to tour your PCB or substrate facility, to come look at your microelectronics manufacturing line. Get in there and explain to your elected officials what your contribution is to the economy and to the technologies that we depend on for modern life, because the response we often get on Capitol Hill is, what is a printed circuit board? What is a substrate? Why are they so important? The educate mission is something that everyone can service, and if you are struggling with how to make that happen, please contact the PCBAA and join our team because it's one of the things that we can help facilitate the advocacy mission is being advanced every day by a team including both PCBAA and IPC. In Washington DC, we are calling on the executive branch, we are calling on the legislative branch, we are doing the

briefings, we are advancing legislation. I think that that mission is best serviced by our trade association representatives and the committed advocates and lobbyists that are doing that work.

You've probably seen a lot of the public affairs work in the form of interviews, op-eds and educational programs. But I don't think (the industry) can sit on the sidelines. The call to action is to engage with your lawmakers because I guarantee if you are running a manufacturing facility anywhere in the country, right down the road the corn growers, the steel workers, the folks who design and introduce software, the retail chains are all engaged in this kind of education advocacy and legislative outcomes. It is not unusual in Washington to be going into a meeting and someone is walking right out the door. They had their concern. We have ours. It is a competitive political environment. You're competing for the attention of lawmakers and their staff, so the more involved our industry is by supporting our trade associations and letting lawmakers know "I am out here; I am a contributor to the economy; this is my economic footprint; these are the jobs I represent; these are the critical technologies" – that is so critically important to understanding an education is the first step on the road to policy change and we've got to have that.

MB: The notion that a printed circuit board manufacturer or assembler might be pushing on their local Chamber of Commerce for support seems, perhaps, a little unusual in most circles. I wonder whether part of the strategy there is because permitting in the United States is a big issue and for the last 40-plus years a lot of barriers have been put up when it comes to printed circuit fabrication. We have water issues. We have toxic chemical issues. We have land issues. There's a host of things that have to be dealt with in order to put a shovel in the ground. Of those companies building new fabrication plants, most of them are building in out-of-the-way places. They're not building in California. Is the idea here that the local Chambers can help pave the way to understanding why these types of businesses are actually good long-term investments in a community? Manufacturing jobs tend to be long-range careers and when it comes to community stability there's a lot these types of businesses can offer.


DS: You are mirroring the sentiment that the Department of Commerce is expressing when it puts out these funding documents. For the Chips Act – and these are 75-page documents – when you get into the language, when you apply for these federal funds they want to see the partnerships, the

agreements, the permitting process that you've already gone through with the state and with the city. The federal government is reflecting what you're saying, that simply having federal money or federal tax incentives is not enough. You can have the funds to put up a building. You need the permit to put up the building. You need to have cleared regulatory approval.

Now the federal government can't do very much to relax the rules or speed the process at the state and local level. But I think there's a recognition that there is a partnership with state and local government and the federal government, right? The federal government providing the funding; state and local governments in many cases providing either incentives or speeding regulatory processes to get us where we need to go. The industry for a long time has faced challenges in that arena, and I would say to state lawmakers, "Federal money is now available. Look to your local communities and ask if there could be a new greenfield initiative." In the case of New York and Michigan, I think they've shown a lot of vision in expanding domestic capacity and in making it easier to do business. Not every state is going to take the same attitude. We certainly see this in any number of manufacturing sectors. It's easier to do business in certain states and that's sort of a competitive environment that we're going to have to operate in. I think there are enough municipalities, enough localities, enough states that see the economic potential. They see careers in microelectronics manufacturing. They see jobs for college graduates with degrees like engineering. They see significant economic impact because everything in the modern world relies on microelectronics. It isn't just vacuum cleaners. It isn't just automobiles. It's electric vehicle chargers. It's windmills. It's solar panels. It's every satellite flying to space. Any community is going to look at this and go, "Yeah, there's a market. Why don't we make this here?" This isn't the kind of manufacturing like textiles, for example, where it's gone overseas and it's not coming back. We were the leader in this at one time and I think we can be in a very strong position again.

MB: In summary PCBAA has a very aggressive – and I mean that in a positive way – legislative calendar coming up over the next 12 or 18 months.

DS: Yes, 2024 of course is an election year, which in some ways provides incentive to move legislation and in other ways it distracts from lawmakers' focus. The second session of the 118th Congress is starting in January, and as I said, we have a number of different priorities. There's things that we have to keep sold for a number of years. There's new initiatives that we need to advance, and I want to get to a place just like where we are with semiconductors where any

lawmaker you speak to says, “I know what printed circuit boards are. I know what substrates are. I understand the technology stack. I get the sense that we led in one era and we have contracted and I want to right that ship. I want to turn that around.” We have dozens of lawmakers today who understand that argument. I want to make it hundreds of lawmakers at the federal and the state level. I think we can do it. 

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Green Strength

An emphasis on speed – same day turns! – keeps Green Circuits' customers coming back.

by MIKE BUETOW

WHEN WE LAST visited Green Circuits, in late 2018, the company was just coming off its merger with Power Design Services. **As we reported at the time**, it was a \$50 million entity with over 200 staff, and had just doubled its SMT capacity.

Much has changed in the ensuing five years: size (bigger), staffing (smaller), management (new). What hasn't, however, is the emphasis on speed and high-complexity board assembly. Indeed, the EMS has leaned into those challenges and is now perhaps as good as anyone in North America in that regard.





Green Circuits occupies a bustling 60,000 sq. ft. site in San Jose.

After Joe O'Neil adeptly managed PDS and Green Circuits through its merger, the private equity firm behind the company turned over the reins to chief executive officer Michael Hinshaw, a seasoned veteran with a background in supply chain management in the specialty chemicals unit at Honeywell and Allied-Signal, and later as a management consultant in McKinsey's semiconductor practice.



Chief executive officer Michael Hinshaw

At the helm of operations is COO Mark Evans, armed with a degree in electrical engineering and a wealth of experience from nearly 20 years in operations and management at Flex, Creation Technologies, Sparton and Hunter Technology. Together, they have cultivated a team built on previous connections, supported by CFO Richard Dutton and vice president of sales and marketing Adam Szychowski.

On the shop floor of the 60,000 sq. ft. plant, the SMT lines are set up so that 90% of kits can run on any of them. The company's array of equipment includes five SMT lines: DEK Horizon stencil printers, Juki FX and KE placement machines, SPI on two lines, BTU convection reflow ovens (four

with nitrogen), and a new JT wave. A new ERP with an MES module for traceability is planned for mid-January.

The smallest parts placed are 01005 and 0.3 μ m BGAs. AOI programming is performed offline but in-house. About 80% of the bare boards used are US-made (“We’ve never seen so much flex and rigid-flex,” says Evans.) The company averages seven inventory turns, and is approaching eight on an annualized basis.



The leadership team, including Michael Hinshaw and Mark Evans, pictured, has added an intense dose of Lean manufacturing to Green Circuits’ operations.

Post-reflow x-ray is performed on Nordson Dage XD7600NT and ViTech 5DX AXI machines, and the company is demoing a Scionscope Xspection 3000. Every product is x-rayed, the company says.

An Anda conformal coating machine is being added because, as Evans says, “Having it in-house was a major issue for customers. For a quickturn shop, we have to be quick.”

Three Takaya flying probe testers are set up in U-cell so one operator can run multiple machines.



The Takaya flying probe testers are set up in U-cell so one operator can run multiple machines.

Cleaning is performed using DI water on an Aqua Kleen Typhoon aqueous washer. Rounding out the SMT area are two BGA rework machines.

Rounding out the capabilities are box-build cells – also in U-cells, and designed and built by the respective operators because, as Evans says, “They know what they need and how they use it best” – and a failure analysis lab.

One interesting technology example we observed while touring the plant in September was double-stacked 0402 ceramic chips. The chips sit in a pocket where the bottom cap is in the recess and the top cap is above the surface. Other complex boards we saw included a 96-layer board Green Circuits builds for a semiconductor test application, and an assembly with more than 12,000 component placements.

Sweet Spots

Operational excellence is a hallmark of Green Circuits. Its sweet spot is five-day turns, but quickturns can be delivered in 1 to 3 days – and even same-day, at a premium. (We confirmed this twice to be sure we heard correctly.) Quotes are turned in 2 to 4 hours.

The typical lot size is 30 to 40 pieces. Low- to medium-volume orders number about 100 to 200 pieces. Green Circuits' averages three changeovers per shift per line, with Evans noting: "We are running the next board almost as last board of previous order is exiting."

Among the efficiencies Hinshaw's team has implemented include training staff in different areas to increase flexibility. The firm conducts "all-hands" meetings on the first of each month to communicate its vision and spread customer feedback throughout the entire organization. Routine Kaizen events involve three to four layers of management. And Evans teaches a one-day class every month to sales, program managers and operators, which "helps break down barriers."

Explains Evans: "We empower everybody. We want people at every level to make decisions. We are not afraid to admit mistakes. (If you don't), you don't find out what really happened."

"We look for people who are speed-focused," Hinshaw adds.

The emphasis has allowed Green Circuits to reduce its staff over the past years to 150, including seven process engineers and two Quality engineers, while more than doubling revenue. The single shift runs from 6 a.m. to 2:30 p.m., but some lines run until 5 p.m. Still, turnover has been slashed from 40% in 2019 to below 8% today.

Anonymous Clients

The end-market focus is familiar for US EMS companies: aerospace, medical, defense, satellite, automotive, semiconductor, robotics. Among the applications are EV and battery charging systems, air taxis, semiconductor equipment, satellite and rocket components, and solar and high-power boards. Certifications include ISO 9001:2015, ISO 13485:2016 and AS9100:2016.

Green Circuits targets customers that have high-complexity and high-speed demands. "They want

quality and speed,” Hinshaw said. “If we can manage that, they tend to stay.” It currently serves hundreds of diverse customers globally.

“We can bring customers through early challenges, technical or supply chain,” says Evans. “We get them to a place we can support them to get them on their way.” Echoes Hinshaw: “We can take a customer from design to prototype to pilot production volumes, and help work out manufacturing issues before helping them transition to larger-scale production elsewhere.”

Future Plans

As it continues to grow in the Silicon Valley, Green Circuits is also casting its eyes elsewhere. Half of its specialty customers are based outside California, and when their calling card is extremely quick turns, proximity begins to matter.

Yet there’s “no urgency” to do an acquisition, says Hinshaw, but the possibilities of strategic regional investments are under consideration. Most important, he adds, is not the size of the target but its culture.

“When making an acquisition, traditionally you look at assets, customers, and talent. We start with culture first. Insofar as regions, it’s wide open. We look for market fit, for a balanced portfolio. It might be a service set that is compatible with ours, such as engineering.”

It’s not easy being Green, but it’s even harder being Green’s competitors. For setting a high bar for turns and capability, Green Circuits is the 2023 CIRCUITS ASSEMBLY EMS Company of the Year.



MIKE BUETOW is president of the PCEA (pcea.net); mike@pcea.net.

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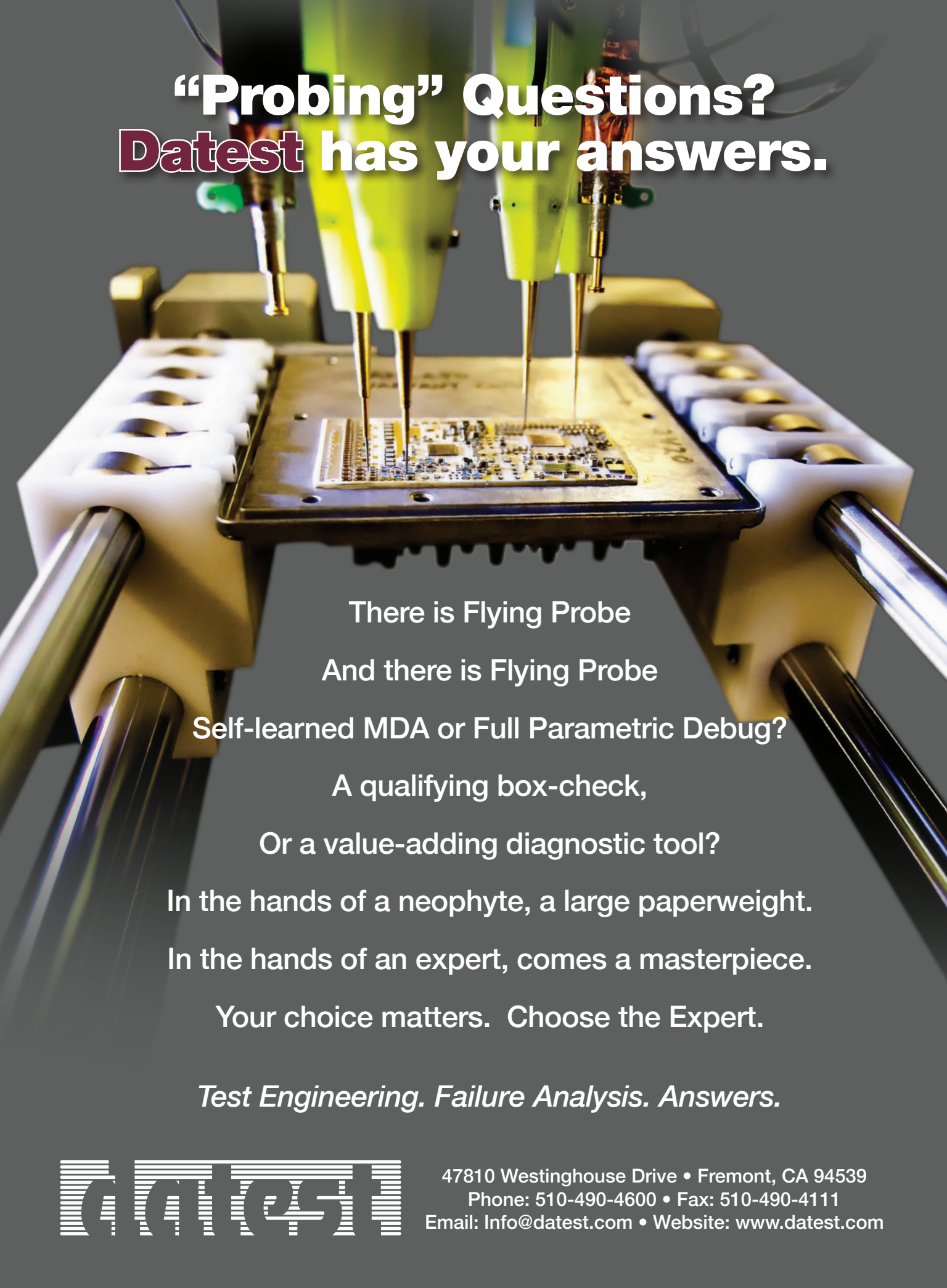
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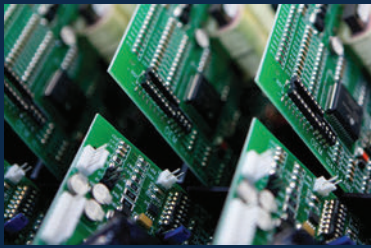
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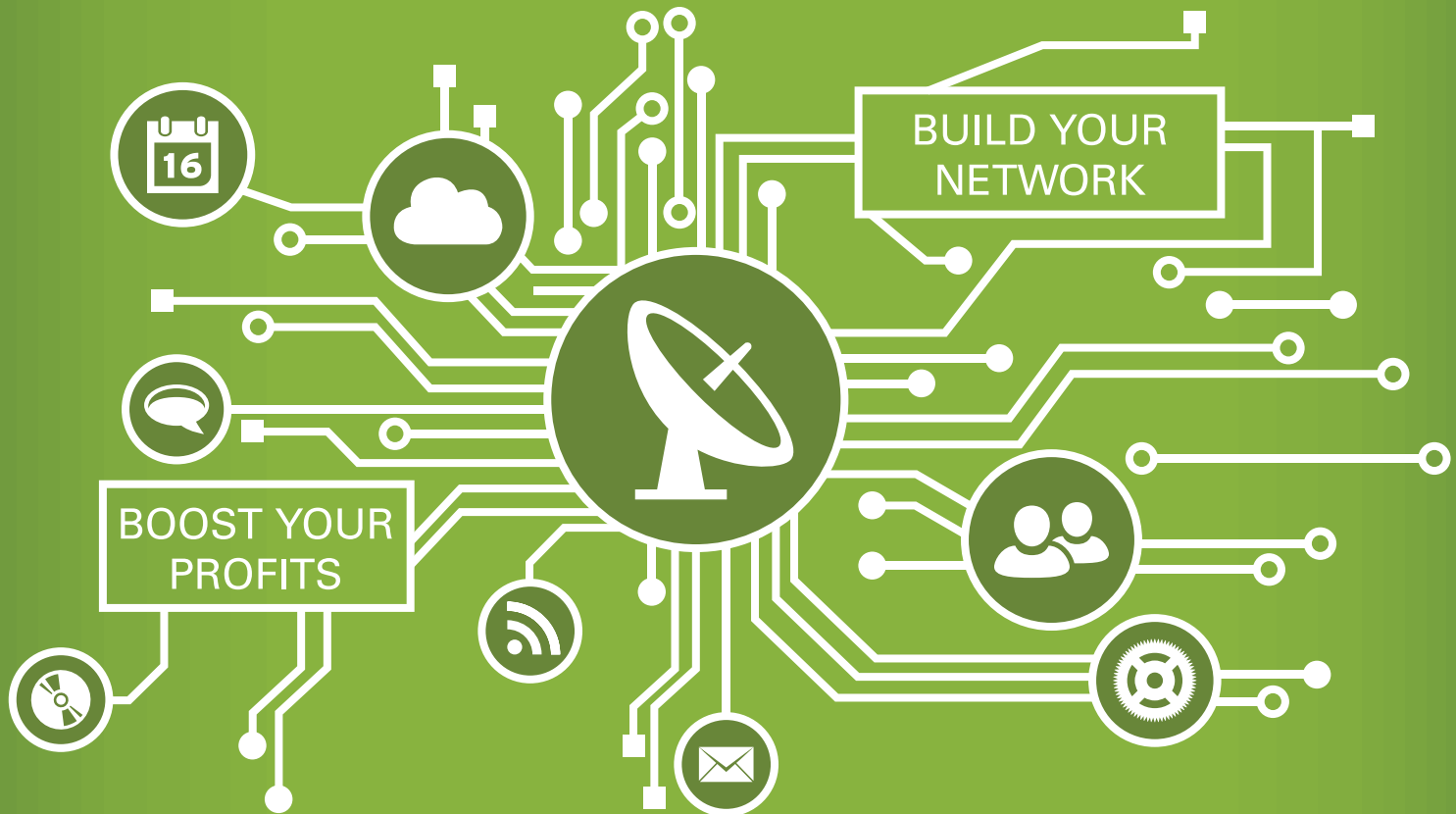
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Transforming Material Exchange

Another changeover task gets an Industry 4.0 makeover.

“**WORK SMARTER, NOT HARDER**” is a phrase that – perhaps surprisingly to some – originated in the 1930s. For nearly a century, this well-known mantra has challenged workers to manage tasks with intelligence and available resources to deliver more effective results. Today, we have significant technological advances and software capability to thank for helping analyze and automate processes for maximum efficiency. For the stencil printing operation, one of the most output-limiting tasks is product or stencil changeover. Changeover is necessary, but there is still room for efficiency improvement to minimize downtime.

It’s true that for many stencil printing changeover activities, engineering solutions have already been developed. There are more mechanically complex remedies, such as universal automatic board support tooling innovations, which have significantly reduced downtime. Software-controlled mechanics have also transformed procedures like stencil loading into the correct position, automatic rail width adjustments, alignment routines, and many other previously manual tasks. One action that hasn’t been successfully tackled, however, is material exchange. So, our company decided to take it on.

Solder paste preservation during changeover. Generally, there are three types of printing changeovers: full product, scheduled stencil interchange and error correction. The first occurs when a completely new product (including a different stencil) is put into rotation. The second may be less well known. In some high-volume manufacturing operations, as part of a preventative approach, stencils for the same product may be changed out every four hours, on average, even if the SPI indicates an in-control process. It’s just standard protocol. Finally, changeover may be indicated if errors are appearing in SPI. In all cases, solder paste material must first be removed from the stencil on the printer, set aside, and then put onto the newly loaded stencil. The only exception is if a total


product changeover requires a different solder paste material (which is uncommon but does happen).

If you've ever managed a stencil printing operation and had to remove paste from the stencil prior to a changeover, you know that solder paste can be challenging to corral; it likes to migrate. Getting the remaining paste off a stencil is a bit like trying to scrape jelly off a plate in an orderly fashion. It is and always has been an essential part of the stencil printing changeover routine, however. And an entirely manual task.

To further improve product and stencil changeover and move toward operator-free, Industry 4.0 methodologies, a new solder paste transfer concept has been developed. With this option and the push of a button in the operating software, solder paste is mechanically moved off the current stencil and positioned for reintroduction once the new stencil is loaded.

Here's how it works: The printer's squeegee pushes the material off the stencil into a customized tray that is attached to the print carriage. The tray is then moved to the back of the stencil printing machine and out of the way of the print nest. The transfer tray is held there until all other changeover elements are completed. Once the new stencil is loaded and production is ready to begin again, the other squeegee drives the material off the tray and onto the stencil into the correct position. If a new product has been introduced during changeover (and it's not just a like-for-like stencil exchange) and the solder paste needs to be in a different position, the system knows where to deposit it. Then, the tray returns to its home position until the next changeover. The stainless-steel tray is detachable and easily removed for cleaning, if necessary.

This novel solution replaces the manual clearing of solder paste, eliminating the operator time associated with the task, and more thoroughly captures and preserves material until production resumes. Working smarter, indeed!

Caveat: As mentioned, some complete product changeovers require different solder paste materials. If this is the case, and a new solder brand or type (moving to Type 5 from Type 4, for example) is required as part of the changeover, the system wouldn't be helpful for that product mix. 

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UCAMCO LEVINA DIRECT IMAGER

LeVina direct imager combines imaging heads equipped with Screen's proprietary GLVTM optical engine and laser control technologies. Is specifically designed for mass production and enables direct imaging of substrates at $2/2\mu\text{m}$ L/S resolution. Reported throughput is 100 substrates per hour with L/S of $5/5\mu\text{m}$. Multi-head system and stage capable of moving at up to 480mm/sec. Alignment marks are read during scanning, for high speed regardless of the number of marks in the scanning direction (can also be automated). Light source uses laser diodes to reduce operating costs. Sources of particle generation have been blocked and system is equipped with airflow control technologies to reduce internal contamination, helping to improve yields.

Ucamco NV

ucamco.com



UNITECH UC-250M-CV PCB CLEANER

UC-250M-CV PCB cleaner offers three-stage cleaning process. Comprises vacuum brush, sticky roller, and ionized air knife, working in harmony to eliminate dust or debris from the PCB surface.

Unitech

unitechkk.co.jp



VISHAY STH WET TANTALUM CAPACITORS

STH series wet tantalum capacitors feature hermetic glass-to-metal seals. Are said to provide advantages of Vishay's SuperTan extended series devices while offering a higher reliability design

for improved military H-level shock (500g) and vibration (sine: 80g; random: 54g) capabilities and increased thermal shock up to 300 cycles. Optimized for energy storage in power supplies, actuators, transponders, and radio, radar, and missile systems, in addition to oil drilling and underwater equipment. Feature high capacitances from 470 μ F to 1500 μ F in the D case code and capacitance tolerances of \pm 20% standard at 120Hz and +25°C, with tolerances of \pm 10% available. Operate over a temperature range of -55° to +85°C, to +125°C with voltage derating, and provide low ESR down to 0.50 Ω at 120Hz and + 25°C. Feature standard tin/lead terminations with RoHS-compliant 100% tin terminations available.

Vishay Intertechnology

vishay.com



CA



EUROPLACER II-P7 SCREEN PRINTER

ii-P7 printer introduces a range of productivity enhancements that include a maintenance-free printhead offering active closed-loop squeegee pressure and zero squeegee calibration. Accommodates stencil sizes from 584mm to 736mm (23 to 29") without an adaptor, reducing setup and changeover times in high-mix assembly environments. print cycle time performance in standard mode is shortened by 25% compared to Europlacer's EP710 printer and is reduced by more than 50% with special motor technology available as an option. Also features an underside component clearance of 30mm, improved cover support ergonomics and a 22" touchscreen monitor. Runs upgraded Europlacer OS (iiPS) software that delivers step-and-repeat functions for

inspection, dispensing and label placement processes, improved processing of low-contrast fiducials as well as a faster commissioning procedure. Also introduces enhancements to the underscreen cleaning process including an external solvent tank and an optional single-pass wet-dry-vacuum under screen cleaner. Fully re-engineered printhead deploys new EuroGlide contoured premium squeegee blades that provide integrated paste containment and easy blade swap and setup, and has IPC-CFX and Hermes-compliant protocols built in, along with remote machine status monitoring and predictive consumable replenishment functions fitted as standard.

Europlacer

europlacer.com

IKEUCHI DRY FOG HUMIDITY CONTROL SYSTEM

Humidity control systems effectively mitigate static electricity issues in surface-mount technology processes while also significantly reducing CO₂ emissions and energy costs. Use “Dry Fog” technology generated by specialized spray nozzles, which consists of ultrafine water droplets, each measuring 10µm or less in diameter, that don’t burst upon contact with objects; instead, they bounce off, keeping products and equipment completely dry. Ensure an optimal humidity environment, even in spacious manufacturing facilities, preventing problems arising from dryness and static electricity in the SMT processes.

Ikeuchi

ikeuchi.eu

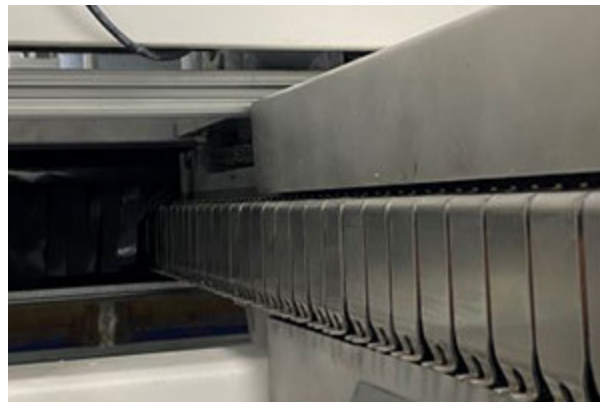


ITW EAE EDISON II ACT STENCIL PRINTER

Edison II ACT stencil printer is integrated with automated changeover technology that is fast and consistent with reduced operator requirement resulting in error-free changeover, and increased yield and throughput. Is said to be the industry's most accurate printer on the market with advanced technology needed for ultra-fine pitch and micro aperture printing processes, for advanced semiconductor stencil printing applications. Has a proven print process capability greater than 2Cpk for 0201 metric components. Features a built-in $\pm 8\mu\text{m}$ machine alignment and $\pm 15\mu\text{m}$ wet print accuracy ($\geq 2\text{Cpk}$ @ 6σ). Has a transfer efficiency that exceeds requirements for the smallest apertures and features a single high precision load-cell with closed-loop pressure control and motor driven system to enable precise and consistent squeegee force control across the entire print stroke in both directions. Innovative machine design achieves ultra-tight coplanarity between stencil and substrate, enabling yield improvement for ultra-thin stencil printing.

ITW EAE

itweae.com



ITW EAE ELECTROVERT HEAVY DUTY CONVEYOR

Electrovert Heavy Duty Conveyor is designed to handle loads of up to 91kg (200lb.) while maintaining the benefits of a single continuous conveyor. Titanium universal V/L fingers with a choice of 3mm or 6mm L, along with precision linear bearing support cross shafts and fine-pitch screw shafts are robust and provide excellent parallelism for the conveyor. High-strength hard-coat anodized aluminum extrusion used in the rail and tunnel support structure are said to be field-

proven in demanding production environments for its durability and stability.

ITW EAE

itweae.com

JARO JARO-343 DIELECTRIC COATING

JARO-343 dielectric coating isolates up to 2,000V of power. Resists most chemicals for short time exposure, and is designed for coating printed circuit boards – particularly heat sink assemblies. Helps distribute heat throughout the entire coated surface and comes in thicknesses ranging from 1 to 6 mils that can be applied in one coat and it meets MIL-E-5272. Coating is said to not peel or blister when exposed for 240 hr. at 50°C and 96% relative humidity and is opaque to offer hiding power, dimple-free curing and edge coverage.

Jaro

jarocorp.com



KEYSIGHT I3070 HIGH-DENSITY ICT

i3070 Series 7i automated inline in-circuit tester offers increased capacity and throughput to meet the complex test demands of larger node count PCBAs. Provides an automated testing process that substantially reduces overall test time and increases capacity up to 5760 nodes on a slim inline footprint to meet complex testing requirements and enable the processing of larger panels.

Enhanced Shorts Test algorithm consisting of two phases – a detection phase and an isolation phase – makes testing procedure 50% faster compared to traditional methods. Enables testing of supercapacitors up to 100 farads through an available integration solution that eliminates the need for individual fixture electronics, and resolves issues often associated with long-wire fixturing, like noise that affects test stability.

Keysight Technologies

[keysight.com](https://www.keysight.com)

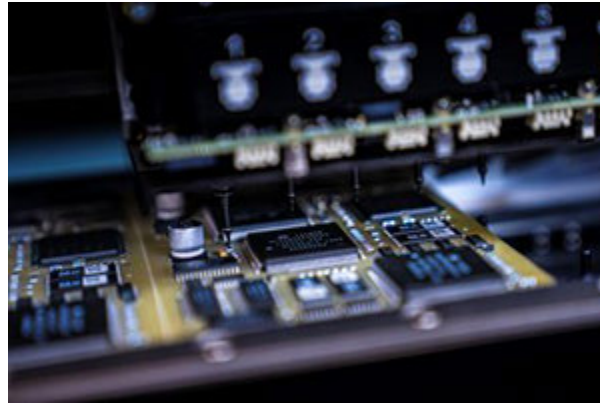


MASTER BOND MASTERSIL 711MED RTV SILICONE

MasterSil 711Med is a one-part, flowable, room-temperature vulcanizing silicone that needs no mixing and can be used for bonding, sealing, coating and form-in-place gasketing applications. Passes ISO 10993-5 testing and withstands many sterilization methods, including liquid sterilants, gamma radiation and EtO. Cures very quickly upon exposure to humidity or moisture, with curing speed influenced by the humidity level. Tack-free time at 75°F and over 50% humidity is 2-5 min. Once cured, delivers high temperature resistance up to 400°F. Is electrically insulative, with a volume resistivity greater than 10^{14} ohm-cm at room temperature. Features superior flexibility and is able to withstand thermal cycling, vibration and shock, with an elongation measuring between 300-400%. Also features Shore A hardness of 25-35. Bonds to a variety of substrates including metals, glass, ceramics, many plastics and cured silicone rubber.

Master Bond

[masterbond.com](https://www.masterbond.com)



MYCRONIC MYPRO A40 PLACEMENT MACHINE

MYPro A40 pick-and-place platform increases top placement speeds by 48% while handling a significantly wider range of component types and sizes. Features high-speed MX7 mounthead technology, which places components up to six times larger than previous high-speed heads. Also features a top speed of 59,000cph, compared to 40,000cph for the MYPro MY300DX. Integrates seven independent placement nozzles steered by 14 individual Z and theta motors, and an advanced motion control system that updates at a rate of 80,000 times per second to ensure control and speed by optimizing every movement across up to 224 interchangeable feeder positions and 640x510mm board placement area. Enables placement of components as large as 45x45x15mm or 150x40x15mm and as small as 0.4x0.2mm (01005). Also features a newly designed graphical user interface to simplify both training and pick-and-place operations for even novice operators.

Mycronic

mycronic.com

PVA PATHMASTER X SOFTWARE

PathMaster X programming software, for Direct Series Delta dispensers. Features gaming-style machine pendant and modern touchscreen monitor for intuitive control over dispenser, and eliminate need to toggle between software and controller. Features enhanced offline programming, allowing programming from anywhere, at any time. Amplifies programming through intuitive drag-

and-drop functionality, and custom overlays for nozzle size and pattern width offer further flexibility and precision. Combines features and functions of PVA Portal and PathMaster into a single application, which allows control of all machine functions and programs in one place and accommodates a variety of applications, from conformal coating to dispensing and custom processes.

PVA

pva.net



SAYAKA CT34XJ PCB ROUTER

CT34XJ router offers a host of features that significantly enhance the PCB routing process. Functions inline and offline. Comes with an interface for robot integration, slide table for rapid loading and unloading of PCBs, and easy programming facilitated by a color CCD camera. Key features include broken/slip bit detection, extended bit life with automatic bit position control, repeatability within ± 0.01 mm and minimal maintenance requirements, automatic QR code reading and program uploading, automatic fiducial marks reading, and optional automatic router bit changer.

Sayaka

sayaka.co.jp

Seika Machinery

seikausa.com



VITROX V9I ARV XL

V9i ARV XL features a six-axis cobot design to enable adjustable angle inspections up to 90° and accommodates PCB dimensions up to 840mm x 620mm. Novel learning algorithm detects a wide range of conformal coating defects and also performs comprehensive inspections for screw, cosmetic, connector, and label defects in final assembly, all achieved without needing CAD information. Is engineered with multi-focal vision capabilities, allowing inspections spanning from 5mm to 200 mm resulting in high-resolution images with clarity down to 14µm/px. Can also be integrated into production line for inline operation using SMEMA connection and can be placed for offline applications with existing conveyor. Offers extended inspection capabilities with two configuration options: the V95i, featuring a rotator function, and the V97i, equipped with a flipped conveyor.

ViTrox

vitrox.com





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In Case You Missed It

Characteristic Impedance

“Identifying and Modeling Resonance-Related Fluctuations on the Experimental Characteristic Impedance for PCB and On-Chip Transmission Lines”

Authors: Yojanes Rodríguez-Velásquez, *et. al.*

Abstract: It is well known that the fluctuations in experimentally obtained characteristic impedance versus frequency curves are associated with resonances originated by standing waves bouncing back and forth between the transitions at the transmission line terminations. In fact, microwave engineers are aware of the difficulty to completely remove the parasitic effect of these transitions, which makes obtaining smooth and physically expected frequency-dependent curves for the characteristic impedance a tough task. Here, the authors point out for the first time that these curves exhibit additional fluctuations within the microwave range due to standing waves taking place within the transition itself. Experimental verification was carried out by extracting this fundamental parameter from measurements performed on on-chip and printed circuit board (PCB) lines using probe pad adapters and coaxial connectors. The authors demonstrate that the lumped circuit approach to represent the transitions lacks validity when the additional fluctuations due to the connectors become apparent, and they propose a new model including transmission line effects within the transition. (*Electronics*, July 2023, <https://doi.org/10.3390/electronics12132994>)

Solder Fatigue

“Low-Cycle Fatigue Life Assessment of SAC Solder Alloy Through a FEM-Data Driven Machine

Learning Approach”

Authors: Vicente-Segundo Ruiz-Jacinto, *et. al.*

Abstract: This paper aims to present the novel stacked machine learning approach (SMLA) to estimate low-cycle fatigue (LCF) life of SAC 305 solder across structural parts. Using the finite element simulation (FEM) and continuous damage mechanics (CDM) model, a fatigue life database is built. The stacked machine learning (ML) model’s iterative optimization during training enables precise fatigue predictions (2.41% root mean square error [RMSE], $R^2 = 0.975$) for diverse structural components. Outliers are found in regression analysis, indicating potential overestimation for thickness transition specimens with extended lifetimes and underestimation for open-hole specimens. Correlations between fatigue life, stress factors, nominal stress and temperature are unveiled, enriching comprehension of LCF, thus enhancing solder behavior predictions. (*Soldering & Surface Mount Technology*, September 2023, <https://doi.org/10.1108/SSMT-08-2023-0045>)

Sustainability

“Functional Composites by Programming Entropy-Driven Nanosheet Growth”

Authors: Emma Vargo, *et. al.*

Abstract: Nanomaterials must be systematically designed to be technologically viable. Driven by optimizing intermolecular interactions, current designs are too rigid to plug in new chemical functionalities and cannot mitigate condition differences during integration. Despite extensive optimization of building blocks and treatments, accessing nanostructures with the required feature sizes and chemistries is difficult. Programming their growth across the nano-to-macro hierarchy also remains challenging, if not impossible. To address these limitations, researchers should shift to entropy-driven assemblies to gain design flexibility, as seen in high-entropy alloys, and program nanomaterial growth to kinetically match target feature sizes to the mobility of the system during processing. Here, following a micro-then-nano growth sequence in ternary composite blends composed of block-copolymer-based supramolecules, small molecules and nanoparticles, the authors successfully fabricate high-performance barrier materials composed of more than 200

stacked nanosheets (125nm sheet thickness) with a defect density less than $0.056\mu\text{m}^{-2}$ and about 98% efficiency in controlling the defect type. Contrary to common perception, polymer-chain entanglements are advantageous to realize long-range order, accelerate the fabrication process (<30 min.) and satisfy specific requirements to advance multilayered film technology. This study showcases the feasibility, necessity and unlimited opportunities to transform laboratory nanoscience into nanotechnology through systems engineering of self-assembly. (*Nature*, November 2023, <https://doi.org/10.1038/s41586-023-06660-x>)

Thermal Transistors

“Electrically Gated Molecular Thermal Switch”

Authors: Man Li, *et. al.*

Abstract: Controlling heat flow is a key challenge for applications ranging from thermal management in electronics to energy systems, industrial processing and thermal therapy. Progress has generally been limited, however, by slow response times and low tunability in thermal conductance. In this work, the authors demonstrate an electronically gated solid-state thermal switch using self-assembled molecular junctions to achieve excellent performance at room temperature. In this three-terminal device, heat flow is continuously and reversibly modulated by an electric field through carefully controlled chemical bonding and charge distributions within the molecular interface. The devices have ultrahigh switching speeds above 1MHz, have on/off ratios in thermal conductance greater than 1300%, and can be switched more than 1 million times. The authors anticipate that these advances will generate opportunities in molecular engineering for thermal management systems and thermal circuit design. (*Science*, Nov. 2, 2023, <https://www.science.org/doi/10.1126/science.abo4297>) 