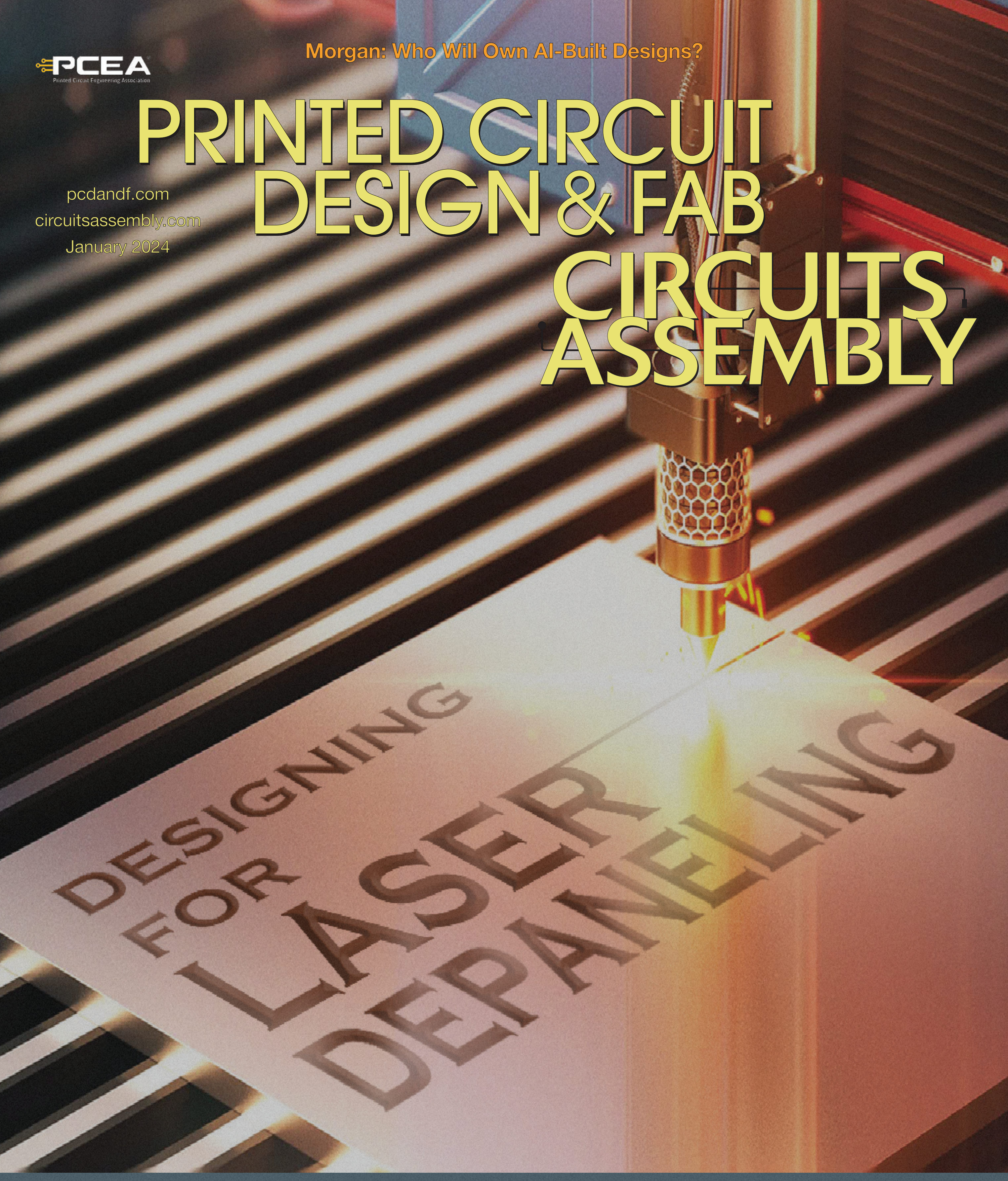

Transmission Line Impedance

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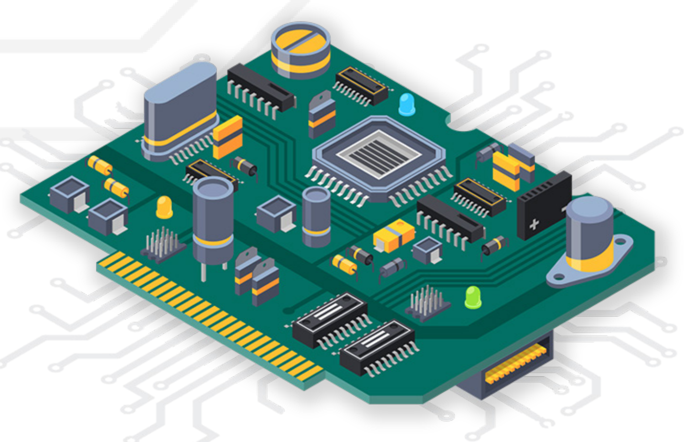

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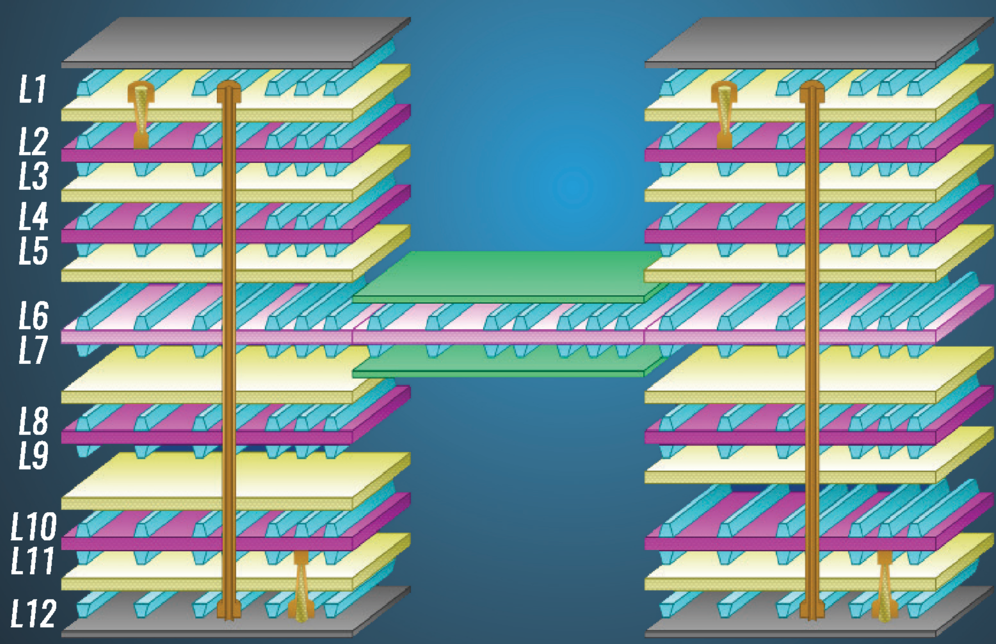

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CIRCUITS ASSEMBLY

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Electrical and Thermodynamic Parallels
Most designers have exposure to the fundamentals of electrical engineering principles, but most have almost no exposure to thermodynamic fundamentals, which can be just as important. A presentation of parallel information on the two disciplines that board designers can use to understand the basic principles of thermodynamics that they often must deal with.
by DOUGLAS BROOKS and DR. JOHANNES ADAM

SIGNAL INTEGRITY
How to Calculate Transmission Line Impedance with Dispersion and Roughness, No Field Solver Needed!
Some advanced fast field solvers can provide full S-parameters, but it is also possible to calculate S-parameters using the lossy characteristic impedance and propagation constant. How to compute transmission line impedance using only a Microsoft Excel spreadsheet and no field solver.
by ZACHARIAH PETERSON

INDUSTRY TRENDS
Nothing Soft about PCB Design Tools Market
Now up in 21 of the past 24 quarters, sales of PCB design software have more room to grow, according to a host of industry executives.
by MIKE BUETOW

DEPANELING (COVER STORY)
Establishing Design Rules for Laser Depaneling of Printed Circuit Boards
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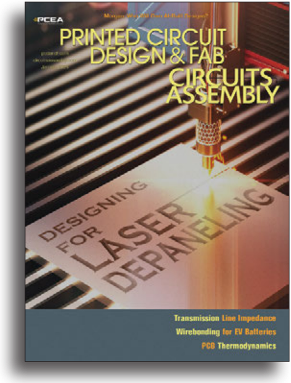
by PATRICK STOCKBRÜGGER and STEPHAN SCHMIDT



ULTRASONIC WIREBONDING
Vibration Resistance and Durability of Wirebond for EV Batteries
Wirebond technology's flexibility gives it a major advantage as an interconnect method, but its durability is lost in open-air applications. Here, the authors look at ultrasonic wirebonding as currently used in EV battery packs, where they are vulnerable to breakage due to vibration in part because they are not encapsulated.
by DODGIE CALPITO, SHUICHI MITOMA, SHIZU MATSUNAGA, KOSUKE ONO and TSUKASA ICHIKAWA

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NOVEL WIRELESS / WEARABLE ESD MONITORING
with DR. DAAN STEVENSON and DR. JONATHAN TAPSON

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AROUND THE WORLD

PCEA CURRENT EVENTS

MARKET WATCH

OFF THE SHELF

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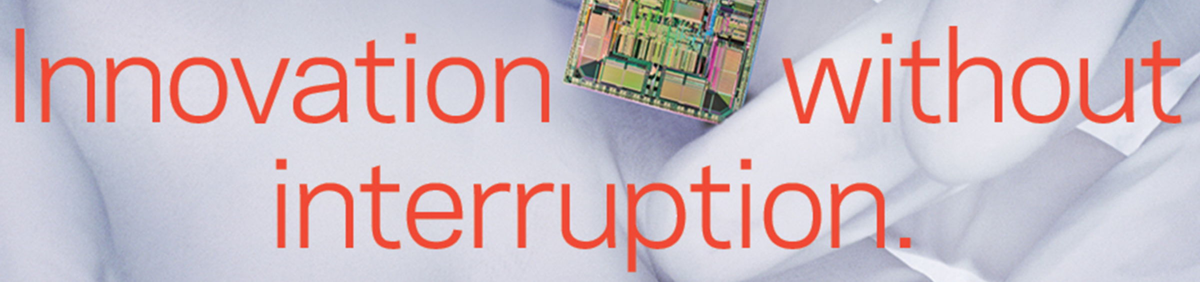

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MANAGEMENT

PRESIDENT
Mike Buetow 617-327-4702 | mike@pcea.net

VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

PCD&F/CIRCUITS ASSEMBLY EDITORIAL

MANAGING EDITOR
Tyler Hanes 205-258-0067 | tyler@pcea.net

COLUMNISTS AND ADVISORS

Clive Ashmore, Peter Bigelow, Robert Boguski, John D. Borneman, John Burkhert, Jr., Stephen Chavez, Geoffrey Hazelett, Mark Finstad, Nick Koop, Geoffrey Leeds, Alun Morgan, Susan Mucha, Greg Papandrew, Chrys Shea, Jan Vardaman, Gene Weiner

PRODUCTION

ART DIRECTOR & PRODUCTION
blueprint4MARKETING, Inc. | production@pcea.net
Nathan Hoeller | nathan@pcea.net

SALES

VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

SENIOR SALES EXECUTIVE
Will Bruwer 404-313-1539 | will@pcea.net

REPRINTS

sales@pcea.net

EVENTS/TRADE SHOWS

EXHIBIT SALES
Frances Stewart 770-361-7826 | frances@pcea.net

TECHNICAL CONFERENCE
Mike Buetow 617-327-4702 | mike@pcea.net

EVENTS MANAGEMENT
Jacqueline Bress 404-955-7675 | jacqueline@pcea.net

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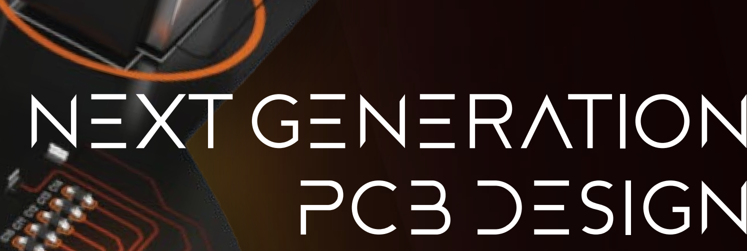

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THE ROUTE

Shows Remind Us Why People Matter

IT WAS GRATIFYING to see the throngs return for Productronica in November. To the tune of 42,000 visitors, the crowds showed up for the granddaddy of shows in the Western world. (Nepcon Japan is roughly twice as big.)

And there was plenty to see. One of the improvements that jumped out was the increase in speeds, especially on the assembly line. Machine speeds are rising at remarkable rates, with placement machines hitting their fastest speeds ever, even while many of them add multifunctional heads for more flexible line setups.

Yamaha's YRM20 placement machine allows nonstop cart and feeder changes. Fuji's AIMEXR SMT placement machine, for NPI runs, relies on linear motors for its fastest speeds yet. So what if the semiconductor market is predicted to rise by double-digits this year? These machines can take the pressure.

In many cases, the machine is telling the operator what to do, instead of vice versa. Juki's LX-8 SMT platform, for instance, walks users step-by-step through the head exchange process, and then the automatic calibration kicks in.

Innovations that made machines more operator-proof, such as the stencil auto changeover on the Panasonic NPM G/L printer, or in somewhat similar fashion, ITW's Edison II printer, which automates changeovers by first wiping the solder from the stencil and saving it in a reservoir, then automatically loading everything – tooling plate, stencil and blade holders – in the correct orientation from a cart prepped by the operator. Europlacer's new ii-P7 printer is said to have a maintenance-free printhead and cuts cycle times in standard mode by 25%, and by more than 50% with an optional special motor.

BTU's new Aurora convection reflow oven has 16 (!) heating zones, and if that wasn't enough, features dual lanes for high-volume production. Viscom's i56059 AOI performs two-sided inspection for higher speed.

That's just a few of the enhancements from the assembly side. We could go on and on, but you get the idea. Speed is in.

And yeah, there was that crowd which, even spread over four days, felt busy and engaged. All in all, it felt like the trade shows of the past, and in a good way.

Time was, trade shows weren't just for the frontline workers. They were also a place companies would send their benches. They did so for a multitude of reasons: to get their eyes (and in some cases, hands) on the latest technology; to network; and sometimes just to reward them for the work they did (or would have to do).

But most of all, they did so to prepare them to become the next group of lead engineers, Quality Assurance directors, business development directors, and so forth. It was a low-cost way to expose valued staff to the world outside the factory.

Then at some point, they stopped. In some cases, it was economics: Business in North America and Europe fell off its 2001 peaks, and justifying travel became a chore. Many manufacturers reduced their headcounts, leaving their engineering benches a shallow fraction of what they once were. Still others pulled workers in out of fear of losing them to competitors.

While I see evidence that the next generation is joining the industry, in many cases their employers aren't letting them out of the factories. The concern over losing a highly trained worker is real, but in my experience artificially holding them back retards their professional growth and only works for so long. A better strategy is to engage as much as possible with the rest of the industry so that your best employees act as a recruiting and sales tool for your business.

At the PCEA events like PCB West and, coming this spring to the Boston area, PCB East, one of the aspects that stands out is how excited engineers are to be there. And in our post-show

surveys and conversations, they repeatedly bring up the desire to meet others in their chosen disciplines, to the degree that we've been asked to spread out the classes so attendees have more time to pick each other's brains. (We are fiddling with the schedule to accommodate these requests.) We see this firsthand at PCEA, where offering new employees the chance to travel has been a huge plus in talent acquisition.

Remember when perks mattered? I think they still do. And while "perk" to some is synonymous with "expense" and "waste," encouraging and supporting workers who engage in their industry is the kind of perk that keeps valued workers from bolting.

mike@pcea.net
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MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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SPI, ZDT to Build PCB Plant in Thailand

BANGKOK – SPI has closed a 10 billion baht ($279.4 million) deal to partner with Zhen Deng Tech to build a PCB manufacturing plant in Thailand.

The investment will establish a plant in Saha Group Industrial Park in Thailand's Prachinburi Province, with a goal to propel Thailand as a key PCB production base in the ASEAN region, SPI said in a release. The company expects an initial investment of 10 billion baht for the first phase and additional investments of more than 50 billion baht ($1.4 billion) by 2030.

"Saha Group is fully prepared to cooperate with all partners and investors. Our land availability and well-established network in Thailand can help our partner's businesses grow quickly and comprehensively in all aspects," said SPI CEO Vichai Kulsomphob. "Currently, Saha Group Industrial Parks cover four strategic locations across Thailand: 1. Kabin Buri in Prachinburi Province, 2. Si Racha in Chonburi Province, 3. Lamphun in Lamphun Province, and 4. Mae Sot in Tak Province. This investment collaboration with Zhen Ding Tech Group utilizes over 300 rai of land, marking a significant move for the future of Saha Group under the era of technology transformation. This will create over a thousand job opportunities in engineering fields to Thailand. We believe that expanding investment under the concept of Eco-Tech Industrial Park will not only benefit the community directly but also enhance the level of market competitiveness for the overall industry of the country."

5G/6G MAESTRO Publishes Materials Development and Electrical Test Roadmap

MORRISVILLE, NC – The International Electronics Manufacturing Initiative (iNEMI) has released the Materials Development and Electrical Test Roadmap, which is part of the 5G/6G mmWave Materials and Electrical Test Technology Roadmap (5G/6G MAESTRO).

MAESTRO, managed by iNEMI, is a joint industry/academia project sponsored by the National Institute of Standards and Technology (NIST) Office of Advance Manufacturing's Advanced Manufacturing Technology (MfgTech) Roadmap Program. This is the second of two roadmap documents that provide a comprehensive 10-year hardware roadmap for mmWave materials development, characterization and electrical test. The first document – Low Loss Dielectric Materials Characterization Roadmap – was published earlier this year.

"This roadmap gives industry an idea of where the technology currently is and where we need to be in the next 10 years to support the development and manufacture of competitive leading edge 5G and 6G networks in the US," says Shekhar Chandrashekhar, CEO of iNEMI.

The substantial information compiled to create the MAESTRO reports and roadmap documents is the result of significant collaboration among individuals in approximately 30 industry and academic settings.

"When teams across the private sector come together around technology roadmapping, their collaborative work creates that optimal R&D plan to achieve real breakthroughs," said Mike Molnar, director of the NIST Office of Advanced Manufacturing. "These technology roadmaps have proved invaluable to advancing US competitiveness and future leadership in building the industries of tomorrow."

This latest chapter of the roadmap focuses on material development needs for several applications and is divided into the following sections: devices (semiconductor technologies), package integration and assembly, antennas and antenna subsystems, thermal management, co-design and multi-physics analysis, and radio frequency (RF) photonics. It also addresses electrical test, identifying gaps, challenges and potential solutions for the electrical testing-related issues of next-generation communication systems.

"It is important for the technical community at 3M and other companies to have access to this kind of roadmap," says Charles Hill, senior research physicist, 3M. "It helps industry identify research and development priorities and know where we can best focus our efforts for our

respective businesses."

"Roadmap elements can provide the direction for driving future research and collaboration that are synergistic with emerging applications. The teams contributing to MAESTRO have helped set the stage for creating a pre-competitive environment for 6G systems development," says Professor Madhavan Swaminathan, department head of electrical engineering and the William E. Leonhard endowed chair at Penn State University, and director for the Center for Heterogeneous Integration of Micro Electronic Systems (CHIMES).

Implementation strategy. The MAESTRO team was also tasked with developing an implementation strategy to execute the vision of the roadmap and promote the growth of a strong US workforce in RF and mmWave communication technologies. Download a copy of the MAESTRO implementation strategy here.

Several partnerships focused on key findings of the roadmap are currently underway. Examples include:

Standard Reference Material Development

- iNEMI mmWave Permittivity Reference Material Development Project team – developing a permittivity standard reference material (SRM) that will be handed off to NIST in 2024.

Packaging and Integration (including Antenna Subsystems)

- ASIC (American Semiconductor Innovation Coalition) Advanced Packaging team – developing a white paper for RF system-in-package (SiP) technical elements to help guide the vision for an advanced packaging manufacturing program.
- Mid Atlantic Semiconductor Hub (MASH) – preparing proposals to create regional hubs focused on promoting research, development, and commercialization of semiconductor technologies . This group will also work toward driving strategies in the mmWave space.

Amphenol Acquires Trackwise Designs

STONEHOUSE, UK – Amphenol has acquired Trackwise Designs, a UK-based flex circuit manufacturer that was in financial distress. Terms of the deal weren't initially disclosed.

The new Amphenol Trackwise Designs is a wholly owned subsidiary of Amphenol Sincere, and will support the company's goal to become the leading cell connection system production company in Europe, Amphenol said in a release.

"Trackwise Designs, together with the continuous expansion of the factory in Hungary and the increase of flex printed circuit production capacity in Europe will result in achieving this vision," Amphenol said.

In July, Trackwise announced a delay in the release of its annual financial results after it had failed to secure a contract to supply cell connection system FPCAs to a Tier-1 supplier, and later announced that it was up for sale after its board reviewed future options for the company.

Dongwei Plans Thai Production Facility

SUZHOU, CHINA – Dongwei Technology, a supplier of vertical plating and surface treatment equipment, has announced plans to build a production base in Thailand, with an investment of RMB61 million ($8.6 million).

The investment includes the establishment of a new Thai company, purchase of land, construction of factories, purchase and construction of fixed assets and other related matters. The project is located in the Logana Ayutthaya Industrial Park and is subject to approval of the local registration authority.

The company said the investment will help enhance its global sales capabilities, increase penetration in key overseas areas, enhance its global influence and popularity, and strengthen its position in the field of global electroplating equipment.

UK PCB Supplier Goes Out of Business

WASHINGTON, ENGLAND – Faraday Printed Circuits, a UK-based PCB supplier that operated for more than 35 years, has closed its doors after a drop in orders amid challenging trading conditions.

The company, which was established in 1987 and had expanded from a 4,000 sq. ft. operation to a 22,300 sq. ft. site, fell into administration under FRP Advisory, but the firm was unable to find a buyer for the company.

"Unfortunately, like many other businesses in the manufacturing industry, Faraday Printed Circuits was not immune to a significant fall in demand and mounting external pressures, most notably rising costs, made the business financially unviable," said joint administrator and FRP Restructuring advisory partner Allan Kelly.

The administrators are now preparing to sell the company's assets and have urged interested parties to get in touch. In the company's accounts to the year ending May 31, 2023, its fixed assets were valued at around £737,000 ($930,000), while liabilities amounted to approximately £1.2 million ($1.5 million).

Icape Acquires German Parts Supplier

FONTENAY-AUX-ROSES, FRANCE – Icape Group has acquired 100% of the assets of Bordan Electronic Consult, a German company specializing in the design of custom-made

technical parts.

Since 2002, Bordan Electronic Consult has been developing a range of services focused on the distribution of technical parts to some 30 customers, mainly based in Germany, and offers a wide spectrum of products, of which almost 80% are custom-made. In 2022, the company generated €0.9 million in revenue and a gross margin of over 35%.

With the acquisition, Icape has established its CIPEM operation in Germany, dedicated to the distribution of "custom-made" technical parts. The long-term partnerships forged by Bordan will enable the company to diversify its sourcing with suppliers based in Germany, Japan and Taiwan, while also generating potential purchasing, cost and sales synergies in the short and medium term, Icape said in a release.

"We are delighted to be able to integrate Bordan Electronics Consult's assets into Icape Group," said Yann Duigou, CEO, Icape Group. "This well-known German player in the distribution of custom-made technical parts reinforces our position as a technological expert at the service of our industrial customers. This new operation should also generate synergies by pooling our respective know-how. The objective of this acquisition, in line with our external growth strategy and our previous operations in this high-stake territory, will be to participate in the improvement of our local subsidiary's organic growth and profitability."

Foxconn to Invest $1.5B in India

TAIPEI – Foxconn will invest more than $1.5 billion in an Indian construction project to fulfill its "operational needs," the company announced in Taiwanese security filings.

The $1.54 billion investment was made through a Foxconn subsidiary, Hon Hai Technology India Mega Development, which has been registered in India's Maharashtra state since 2015. A concurrent filing said the same subsidiary would budget the equivalent amount in Indian rupees for a construction project to fulfill "operational needs." The company did not disclose any additional information about the project.

Post-Covid, Foxconn has looked at different strategies for better supply chain resiliency.

Considerations include moving some of its production outside China. Among the pending projects in India are a $600 million project in Karnataka state and a $500 million factory in Telangana state.

VDL Acquires Rena Electronica

EINDHOVEN, NETHERLANDS – VDL Groep has announced the acquisition of Rena Electronica, a Dutch manufacturer of smart electronics and LED lighting.

The addition of Rena's specialists and machines will boost VDL's production capacity, particularly with its subsidiary, VDL TBP Electronics, which specializes in printed circuit board assemblies, VDL said in a release.

Rena has a turnover of €12 million ($15.2 million) and more than 50 employees.

"Our ambition is to be a one-stop-shop industrial partner. Besides our competencies in mechanics and software, with VDL TBP Electronics in our ranks, we've taken a big step forward in electronics," said Willem van der Leegte, president and CEO, VDL. "With Rena's skilled employees and high-quality machines, we're further expanding our production capacity, enabling us to better fulfill the increasing demands of our clients."

"By becoming part of VDL, we'll be able to grow further in added-value innovative solutions together," said Jochem Winkelman, general manager, Rena Electronica. "This acquisition ensures long-term continuity for our clients and employees."

Hanza Acquires EMS Firm Orbit One

STOCKHOLM – Hanza will acquire all shares in Orbit One, a Swedish contract manufacturer of electronics and electromechanics. Hanza will pay an estimated SEK367 million ($35.1 million) for Orbit One, plus potential adders based on the company's performance in 2024, up to a maximum of SEK91 million ($8.7 million).

Closing is subject to regulatory approvals, which are expected to be received by early January 2024 at the latest.

Orbit One has annual sales of approximately SEK1.1 billion ($105 million) with an operating profit (EBITA) of approximately SEK70 million ($6.7 million). It operates two production facilities in Sweden and one in Poland and has a total of approximately 620 employees, of which approximately 65 are engineers.

Orbit One holds a strong position in the Nordic EMS market and has a stable and diversified customer base, and its acquisition strengthens Hanza's manufacturing cluster in Sweden and Central Europe, adds capacity and expertise in electronics manufacturing and contributes to increased earnings per share, Hanza said in a release.

"Hanza is a good and long-term new owner with the strength and ability to continue developing Orbit One," said Orbit One board member and co-owner Mats Johansson. "We complement each other in an excellent way and the merger creates one of the Nordic region's most competitive contract manufacturers. Furthermore, Hanza, like Orbit One, places great emphasis on creating a good corporate culture with sustainable and sound values. This has been an important factor in the choice of a new owner."

"Orbit One is a respected colleague in the industry that has positioned itself as one of the leading electronics manufacturers," said Hanza CEO Erik Stenfors. "It is therefore with pride that we announce this acquisition that further develops Hanza's manufacturing cluster in Sweden and Central Europe in a very good way. The acquisition is also fully in line with our communicated strategy Hanza 2025."

"Hanza's unique manufacturing concept together with Orbit One's leading position in electronics manufacturing is a perfect combination," added Orbit One CEO Mattias Lindhe. "Together we will be able to develop and expand our businesses and become even stronger in our industry. This deal is good for both our customers and our employees."

US DoD Awards Nearly $10M to 7 Microelectronics Firms

WASHINGTON – Seven microelectronics firms received nearly $10 million in combined funding to commercialize technologies of interest to the US military services as winners of the Defense Business Accelerator (DBX) Microelectronics Challenge. The initiative is funded by the Department of Defense (DoD) and led by the US Partnership for Assured Electronics (USPAE).

The challenge aims to revolutionize how the DoD drives the development of dual-use technology, which can be used for both civilian and military applications. The challenge is testing the hypothesis that the DoD can accelerate growth of a robust domestic industrial base by focusing its resources on commercialization of early-stage, hardware-intensive technologies and then scaling them into resilient businesses in partnership with private capital.

The DBX Microelectronics Challenge offered an opportunity for advanced technology innovators to vie for funding of up to $2 million each to further commercialize their emerging technologies. The winning companies also will receive commercialization support through an ongoing accelerator program, which includes one-on-one coaching, access to resources and more. The accelerator program's goal is to not only mature the technology but also scale the domestic business to fill critical gaps in the microelectronics supply chain.

After evaluation of 279 submissions received via an open solicitation, 25 finalists pitched their ideas at the Defense TechConnect Innovation Summit on Nov. 28. A panel of industry experts, investors and a DoD representative judged the presentations, selecting the following seven challenge winners for a combined $9.6 million in funding:

- Freedom Photonics LLC ($1,500,000)
- Gigantor Technologies ($2,000,000)
- Momentum Optics ($1,675,000)
- Mosaic Microsystems ($1,000,000)
- PseudolithIC, Inc. ($1,000,000)
- SiliconCore Technology, Inc. ($1,675,000)
- Soctera, Inc. ($750,000)

"Typically, the timeline from selection to contract award and receipt of funding is several months. DBX leverages the flexibility of Other Transactions Authority (OTA), along with some innovative structuring of the OTA agreement, to enable awardees to receive funding within 48 hours of their selection at the pitch event," said Christopher Zember, senior fellow for Industrial Base Resilience who is supporting DoD as the architect and lead for this project.

The collaboration between USPAE, a nonprofit organization with members spanning the electronics ecosystem, and the DoD's Manufacturing Capability Expansion & Investment Prioritization Directorate (MCEIP) has been instrumental in driving this initiative forward. Tactical support from Advanced Technology International (ATI), and specifically its TechConnect division, has further fortified the success of the DBX Microelectronics Challenge.

"We're honored to move the area of microelectronics forward with this funding and the ongoing accelerator program that we'll make available to the winners over the next eighteen months," said Nathan Edwards, executive director of USPAE. "The outcome will be faster access to dual-use technologies for which the military services already have a validated interest."

Commerce Department Announces First CHIPS Act Incentives

WASHINGTON – BAE Systems' New Hampshire-based operations will receive a $35 million grant to quadruple its production of a chip used in F-15 and F-35 fighter jets in the first CHIPS Act funds to be distributed by the US Department of Commerce.

The award is the first of several expected in the coming months, as the Commerce Department begins distributing the $39 billion in federal funding that Congress authorized under the 2022 CHIPS and Science Act. The money is intended to incentivize the construction of chip factories in the United States and lure back a key type of manufacturing that has slipped offshore in recent decades.

Commerce Secretary Gina Raimondo said that the decision to select a defense contractor for the first award, rather than a commercial semiconductor facility, was meant to emphasize the administration's focus on national security.

"We have been clear since day one that the CHIPS for America Program is about advancing our national security and strengthening domestic supply chains, all while creating good jobs supporting long-term US economic growth," she said in a statement. "As national security becomes as much about the chips inside of our weapons systems as the weapons systems themselves, this first CHIPS announcement shows how central semiconductors are to our national defense."

SEMI and SIA both released statements applauding the first distribution of funding from the CHIPS Act.

The announcement "represents an important milestone on the path to fulfilling the tremendous promise of the CHIPS and Science Act and reinforcing America's national security, critical supply chains, and the economy," said SIA president and CEO John Neuffer. "We applaud Secretary Raimondo and the CHIPS Program Office team for working diligently to begin getting CHIPS incentives out the door. We look forward to additional projects being funded and stand ready to continue working with Commerce Department leaders to ensure the CHIPS and Science Act reinvigorates US semiconductor production and innovation for years to come."

"We commend the thoughtful approach the US Department of Commerce has taken in awarding incentives and are pleased to see the advancement of incentives to bolster the resiliency of the domestic semiconductor supply chain," said Joe Stockunas, president, SEMI Americas. "In order for the global semiconductor industry to support the push for digitalization and a diverse range of smart applications over the coming years, we must go beyond elevating just one facet of the supply chain and pursue a fortified ecosystem encompassing equipment, materials and advanced packaging. SEMI has advocated with the US Chips Program Office to distribute incentives with this goal in mind, and we are confident in their understanding of the industry's needs."

The CHIPS and Science Act provides a 25% tax credit for US facilities that produce semiconductors or chipmaking equipment and $52 billion in funding for new or updated

semiconductor-related manufacturing programs. The funding includes $39 billion for grants available to semiconductor manufacturers as well as equipment and materials suppliers and $11 billion for federal semiconductor research programs.

Ag Express Electronics Establishes Wire Harness Division

DES MOINES, IA – Ag Express Electronics, a provider of solutions, sales, service and support for electronic devices for farmers, agriculture dealers and OEMs, announced the establishment of Integrated Circuit Works, a dedicated division focused on wire harness manufacturing that will expand to include electronics assembly and printed circuit board manufacturing.

The Integrated Circuit Works division, formerly Alliance Group Technologies in Warren, IN, was awarded ISO 9001:2015 by National Quality Assurance (NQA) in August 2023.

“Today, we are focused on wire harness manufacturing and box builds, but in the very near future, the division will expand to feature repair services and printed circuit board manufacturing in an ISO 9001:2015 environment,” said COO Eric Randolph.

“Ag Express has always been at the forefront of innovation in the agricultural industry. Our new Integrated Circuit Works division is a natural progression that empowers the company to contribute meaningfully to the success of our clients,” added Jim Steinke, chief growth officer. “Achieving this certification reflects the world-class manufacturing culture nurtured at Ag Express and the overall commitment to quality and reliability that runs deep in our company’s DNA. As the Integrated Circuit Works division scales, we expect to expand into other industries such as construction, public works, forestry, and more.”

PCD&F

Chin Poon Industrial will expand its PCB manufacturing capacity in Thailand.

Eltek received five purchase orders totaling $3.8 million for PCBs.

Jiangxi Hangde's 5 billion yuan copper foil project began operation in the Xiaolan (China) Economic Development Zone.

RS Group selected **Siemens** as its strategic EDA provider for its DesignSpark Circuit Simulator tool.

Japanese chip materials maker **Resonac** plans to set up a research and development center for advanced semiconductor packaging and materials in Silicon Valley. The former **Showa Denko**, a manufacturer of packaging materials for PCBs, plans to begin operations at its new center in 2025.

Shennan Circuits will build a printed circuit board fabrication facility in Thailand.

Ventec expanded its manufacturing capabilities at its Taiwan facility to produce its VT-901/VT-90H polyimide laminates and prepregs.

CA

Aegis Software and **Arch Systems** announced a partnership toward digitizing continuous improvement of factory operations.

Amkor Technology will build a $2 billion advanced packaging and test facility in

Peoria, AZ.

Altus will distribute **Asscon's** VP810 vapor phase soldering system.

Aoxin Semiconductor Technology is planning a 5 billion yuan IC packaging substrate facility in Huzhou, China.

Apple is reportedly allocating product development resources for the iPad to Vietnam.

Astranis Space Technologies purchased a **Hentec Industries/RPS Automation** Odyssey component lead tinning system.

Ciena is expected to begin production of the industry's first pluggable optical line terminals, as well as its optical network units, at a **Flex** factory in the US in mid-2024.

Cursey Technology installed a **Europlacer** SMT line.

Cyient DLM announced the inauguration of a new precision machining facility in Bangalore.

Delo Industrial Adhesives has begun its foray into medical electronics applications.

Dixon Technologies subsidiary **Padget Electronics** received a manufacturing contract from **Lenovo** to produce laptops and notebooks.

Element Solutions placed on Newsweek's list of America's Most Responsible Companies and earned an EcoVadis silver medal for its sustainability efforts.

Foxconn was approved to collect $6.3 million in Wisconsin state tax credits for reaching 1,029 jobs and spending about $26.7 million on buildings and manufacturing equipment in 2022.

Huawei will move its smart car operations to a new joint company with **Changan**.

HyRel Technologies named **EQC Southeast** as its manufacturers' representative.

India's Ministry of Electronics and Information Technology is developing a new scheme to bolster electronics component manufacturing within the country.

Inovaxe was named distributor for **VisiConsult's** x-ray counter solutions in the US.

Jaltek Systems and **SG Automotive** signed a collaboration agreement to support demand from the European and UK markets.

Kasdon Electronics will supply 180,000 PCB assemblies for the SKA-Low radio telescope to be built in Australia.

PE firm **LFM Capital** announced an investment in **SisTech Manufacturing**.

MAG Capital Partners acquired a Michigan industrial property in a sale leaseback with EMS firm **MARA Technologies**.

Offshore Electronics has invested more than £400,000 into its manufacturing headquarters in St Peter Port, Guernsey.

OSI Systems announced new orders totaling approximately $5 million to provide electronic assemblies to a leading technology OEM.

Plexus implemented **Arch Systems'** ArchFX's platform across its SMT lines within its production facilities, and joined the United Nations Global Compact, a voluntary leadership platform for the development, implementation and disclosure of socially responsible business practices.

Porotech and **Foxconn** are partnering to advance MicroLED microdisplays for augmented reality applications.

Rocka Solutions appointed **PIT Equipment Services** as its representative for the

eastern US.

Supplyframe and **Jabil** announced a collaboration to leverage AI and automation for enhanced operations and decision-making in the electronics industry.

SVI Public Co. established a Chinese subsidiary.

Syrma SGS Technology has formed a semiconductor-focused subsidiary, Syrma Semico, as well as an electronics and communication-focused subsidiary, Syrma Strategic Electronics.

Transition Automation received a large order for advanced holder and blade assemblies from **Rotec BV** in Belgium.

TRI announced the expansion of its Malaysian office.

Variosystems opened a plant expansion in Sri Lanka, doubling its wire harness and assembly production capacity in the country.

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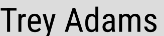
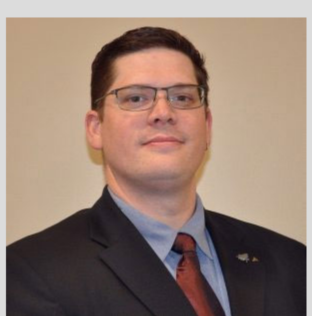
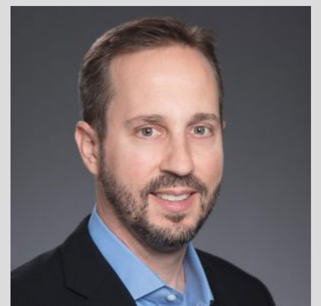

Trey Adams


Justin Fleming

Sean Hill

Cameron Stouder


Jon Faust

Calumet Electronics appointed **Trey Adams** vice president and general manager.

Fresh Consulting named **Justin Fleming** component engineer.

IEC hired **Sean Hill** for sales and service for dry film, chemicals, laminates and phototools.

L3Harris Technologies named **Cameron Stouder** senior specialist PCB design.

Millennium Circuits welcomed **John Waite** as quality assurance manager.

Sanmina appointed **Jon Faust** CFO.

Siemens EDA named **Marina Hamdy Zaky** customer training engineer.

CA

Xuan Tung Le

Ramon Hernandez

Nicolas Denis

Doug Edwards

Charles-Alexandre Albin

David Kalaidjian

Andre Kundert

Brian Kady

Steve Foster

Giuseppe Zanni

Jenny Taymon

Gary Kakos

Charles Freeman

AIM appointed **Xuan Tung Le** technical sales engineer.

ASMPT appointed **Ramon Hernandez** country manager for Mexico.

Asteelflash appointed **Nicolas Denis** CEO.

Celsia named **Doug Edwards** director of business development.

Escatec appointed **Charles-Alexandre Albin** CEO, effective Mar. 31, 2024.

Goepel Electronics named **David Kalaidjian** national sales development manager for the US.

Horizon Sales hired **Andre Kundert** as sales representative for Florida.

Identco named **Brian Kady** vice president of global sales.

Indium promoted **Steve Foster** to associate director.

Seica Deutschland appointed **Giuseppe Zanni** branch manager.

STI Electronics added **Jenny Taymon** to its training team.

Universal Instruments named **Curt Anderson** general manager, USA and Canada.

Vision Engineering hired **Gary Kakos** distributor sales executive.

Zentech appointed **Charles Freeman** GM of Zentech Dallas.

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PCEA Training Announces 2024 PCB Design Classes

PEACHTREE CITY, GA – PCEA Training is offering three five-day training classes next year for printed circuit engineers, layout professionals, and other individuals currently serving in the design engineering industry or seeking to get into it.

Class dates include:

- Class 1: February 5, 12, 20, 26, and March 4
- Class 2: April 5, 12, 19, 26, and May 3
- Class 3: June 14, 17, 21, 24, 28

These instructor-led classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

There are no prerequisite requirements to enroll. Upcoming classes will be held online. All courses are led by experienced instructors.

Registration fees include the 400-page handbook, *Printed Circuit Engineering Professional,* authored by Michael Creeden, Stephen Chavez, Rick Hartley, Susy Webb and

Gary Ferrari.

The course includes an optional certification exam recognized by PCEA.

For information about the instructors of the course and authors of the course material, visit pceatraining.net/instructors-authors.

For information about the course overview, class format, and materials to prepare in advance for the class, visit pceatraining.net/course-overview.

To apply, visit pceatraining.net/registration for the next available class or contact Mike Buetow at pceatraining@pcea.net for additional information.

AI, Containing Heat Focus of Upcoming Technical Webinars

PEACHTREE CITY, GA – Among the member webinars in the coming months are talks on PCB thermal management, the impact of artificial intelligence on electronics, and additive manufacturing.

On Jan. 17, Doug Brooks and Dr. Johannes Adam will present Via and Trace Currents and Temperatures. Rather than thinking of current density, the presenters say, focus on material parameters and properties that determine the temperature of a trace and how these are calculated. Results of some simulations of vias of varying widths and amps will be shown.

On Jan. 23, a panel made up of experts from Siemens, Zuken, CircuitMind and Luminovo, among others, will debate AI in Electronics.

On Feb. 27, Ventec will present on thermal management in materials.

All webinars will include time for audience questions. To register, visit https://pcea.net/events.

PCEA member webinars are free for all PCEA members. Join as an individual member for free at https://pcea.net/pcea-membership.

Abstracts Sought for PCB West

PEACHTREE CITY, GA – Abstracts are now being accepted for the PCB West 2024 technical conference. The conference, the largest of its kind in Silicon Valley, focuses on training and best practices for printed circuit board design engineers, electronics design engineers, fabricators and assemblers.

The four-day technical conference will take place Oct. 8-11 at the Santa Clara (CA) Convention Center. The event includes a one-day exhibition on Oct. 9.

Papers and presentations of the following durations are sought for the technical conference: one-hour lectures and presentations; two-hour workshops; and half-day (3.5-hour) and full-day seminars.

Preference is given to presentations of two hours in length or more, and no presentations of less than one hour will be considered.

Abstracts of 100-500 words and speaker biographies should be submitted to PCEA. Papers and presentations must be noncommercial in nature and should focus on technology, techniques or methodologies related to printed circuit board design, fabrication, assembly, test, components or packaging, and additive manufacturing.

Submit abstracts at pcbwest.com by Jan. 26. No emailed abstracts will be accepted. Submitters will be notified by early April if their abstract has been accepted. Presentations are due Sept. 6.

Presenters of accepted abstract(s) for the 2024 program receive a complimentary pass to the full technical conference, complimentary access to the online proceedings, and an invitation to the speaker reception.

For more information about PCB West, visit pcbwest.com or contact Conference Director Mike Buetow at 617-327-4702; mike@pcea.net.

PCEA CURRENT EVENTS

CHAPTER NEWS

Portland. The next chapter meeting is scheduled for Jan. 11 at 12 noon and will take place online. The technical presentation is on design rules for laser depaneling of printed circuit boards, presented by Stephan Schmidt. Contact stschmidt@outlook.com for a meeting invitation. Our goal is to continue to have one piece of technical content or discussion at each future meeting to provide more value for all chapter members participating.

Support For Flex, Rigid Flex and Embedded Component Designs Now Available.

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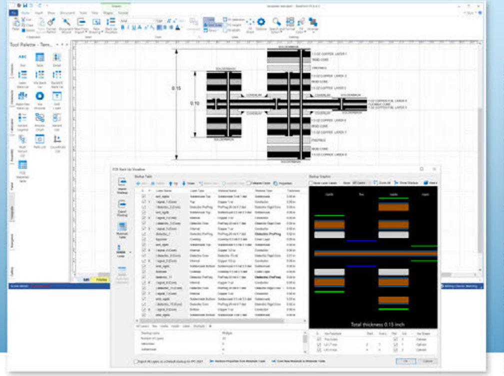
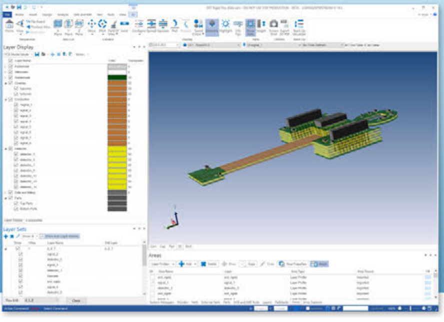
DownStream's CAM350 and BluePrint-PCB support importation and visualization of PCB designs containing Flex, Rigid Flex or Embedded components. Visualize designs in both 2D and 3D, and easily document complex Flex or Rigid- Flex Stack-Ups for submission to PCB Fabricators.

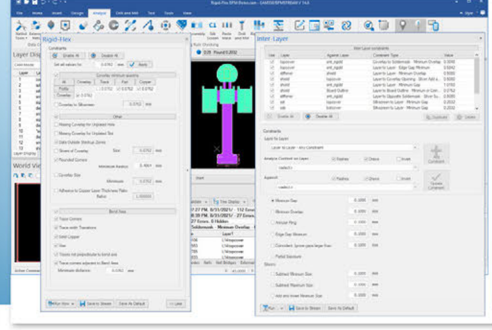
- **Import and Visualize Flex, Rigid-Flex and Embedded Component Designs**
- **3D Visualization to Validate PCB Construction and Component Assembly**
- **Manage Variable Stackup Zones for Rigid-Flex Designs**
- **Easily Create Custom Flex or Rigid-Flex Fabrication and Assembly Documentation**
- **Use DFM analysis to analyze a flex or rigid-flex design for potential fabrication or bend related defects**



Use Stack Up Visualizer and Blueprint's Rigid-Flex Stackup template to easily manage and document rigid-flex stackups.



A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



Use Rigid-Flex and Inter-layer DFM analysis to analyze flex and rigid-flex designs.

For more information visit downstreamtech.com or call (508) 970-0670

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MARKET **WATCH**

Reshoring Job Announcements on Record Pace in 2023

SARASOTA, FL – Reshoring and foreign direct investment job announcements continued their record-breaking run in the first half of 2023, according to the Reshoring Initiative's "1H 2023 Report."

The Initiative expects to see roughly 300,000 jobs announced by year-end, with EV battery and chip investments, along with other essential product industries, accounting for the bulk of the announcements.

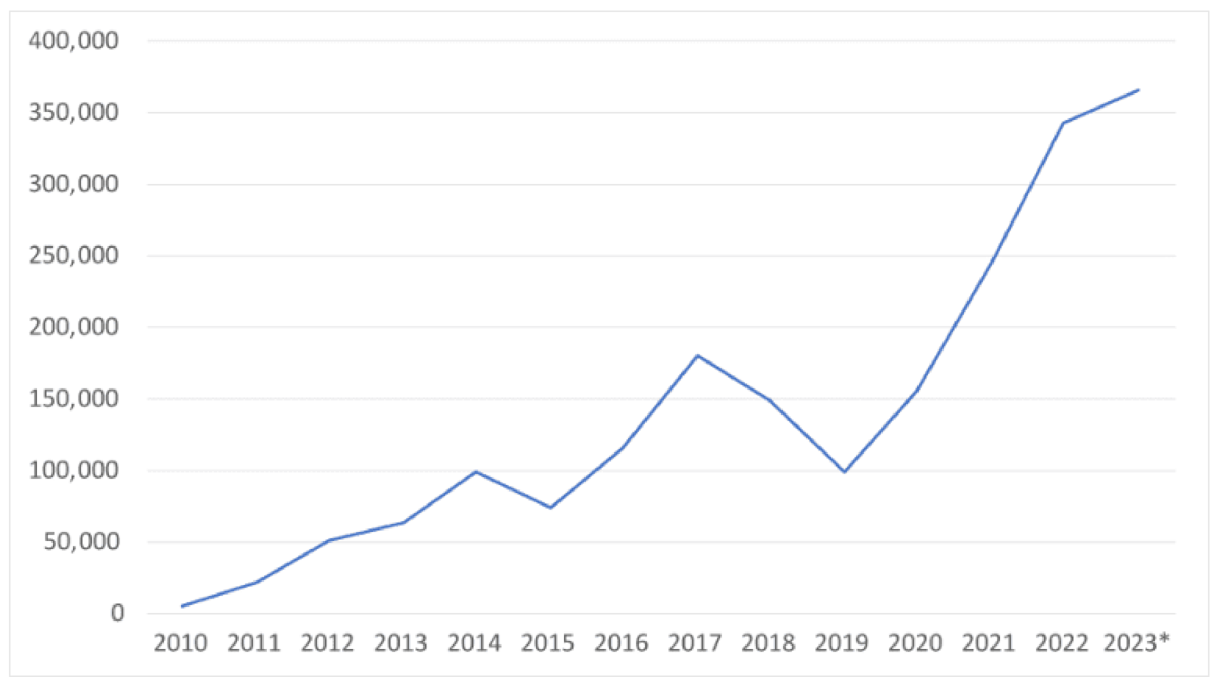


Figure 1. Reshoring + FDI job announcements by year, 2010 – 2023 projected.

According to the report, several factors have come to light that substantiate the strength of US reshoring and FDI trends. In the first quarter of this year, average spending on US factory

construction was more than double the average from the past 17 years. Reshoring Initiative data parallels the magnitude and focus of the construction investments.

Independently conducted surveys on reshoring actions by US companies also correlate very closely with Reshoring Initiative data on jobs announced over the past 12 years, adding validity to both data sets.

The "1H 2023 Report" contains data on US reshoring and FDI by companies that have shifted production or sourcing from offshore to the United States.

"We publish this data to show companies that their peers are successfully reshoring and that they should reevaluate their sourcing and siting decisions," said Harry Moser, founder and president of the Reshoring Initiative. "With 5 million manufacturing jobs still offshore, as measured by our $1.2 trillion/year goods trade deficit, there is potential for much more growth. We also call on the administration and Congress to enact policy changes to make the United States competitive again."

Read the full report here.

New Noise

Trends in the US electronics equipment market (shipments only)

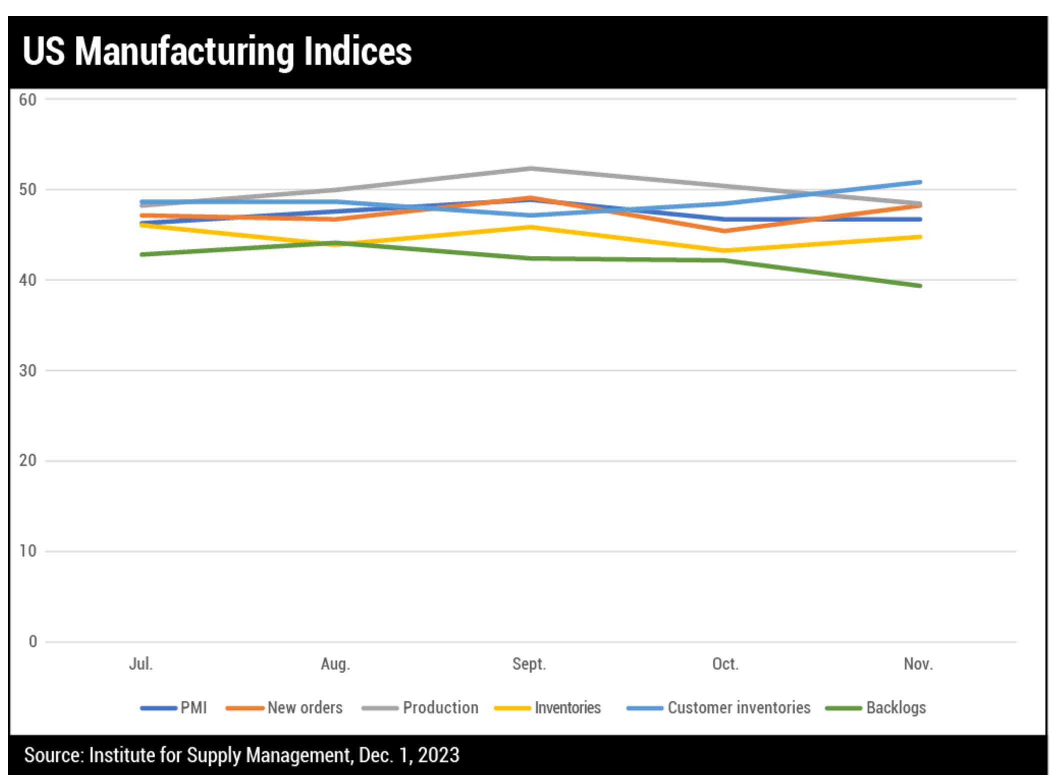
	% CHANGE			
	AUG.	SEP.[r]	OCT.[p]	YTD
Computers and electronics products	0.2	0.7	0.1	1.9
Computers	2.6	-2.9	3.4	11.4
Storage devices	-1.4	-2.1	1.5	13.2
Other peripheral equipment	9.1	3.4	-3.6	26.0
Nondefense communications equipment	-0.5	1.5	-1.1	-2.0
Defense communications equipment	-3.8	-1.5	4.0	3.3
A/V equipment	-16.2	-12.7	-8.4	15.6
Components[1]	4.8	2.8	-1.2	2.3
Nondefense search and navigation equipment	-0.9	1.2	-0.2	1.4
Defense search and navigation equipment	0.0	0.2	0.6	3.9
Electromedical, measurement and control	-0.3	0.0	1.7	1.0

[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Dec. 4, 2023

Key Components

	JUL.	AUG.	SEPT.	OCT.	NOV
EMS book-to-bill[1,3]	1.24	1.27	1.27	1.23	1.23
Semiconductors[2,3]	-11.8%	-6.8%	-4.5%	-0.7%	TBA
PCB book-to-bill[1,3]	0.98	1.00	1.01	0.97	0.97
Component sales sentiment[4]	83.0%	90.3%	86.7%	88.8%	83.3%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA



Source: Institute for Supply Management, Dec. 1, 2023

Hot Takes

Semiconductor sales worldwide are expected to contract 9.4% for 2023, followed by a robust recovery in 2024 with an estimated growth of 13.1%. (WSTS)

North American **electronics manufacturing services** in November shipments rose 0.2% from last year and slipped 1.4%from October. Bookings fell 10.1% year-over-year and increased 4.3% sequentially. (IPC)

India's electronics exports grew 26% in 2023 to $26.8 billion, while imports of finished electronic goods dropped to $13.8 billion in 2023 from $15.4 billion in 2022. (GTRI)

Global sales of **semiconductor manufacturing equipment** by OEMs are forecast to fall 6.1% to $100 billion in 2023 but are predicted to rise to a record $124 billion in 2025. (SEMI)

Worldwide **smartphone shipments** are forecast to see 7.3% year-over-year growth in the fourth quarter. (IDC)

North American **PCB shipments** in November were down 22.5% year-over-year and down 16.3 from October. Bookings fell 9.2% from last year and fell 9% sequentially. (IPC)

Global **semiconductor equipment billings** contracted 11% year-over-year to $25.6 billion in the third quarter, while quarter-over-quarter billings slipped 1% during the same period. (SEMI)

Bare PCB imports into the US soared to 151 million units in October, growing 49% compared with September. (IndexBox)

2024 **semiconductor revenue** will reach $632.8 billion this year, up 6% from 2023, with the US market remaining resilient from a demand standpoint and China's recovery beginning by the second half. (IDC)

Three-fifths of businesses view **generative artificial intelligence** as a good opportunity but many fear they are exposed to cyberattacks. (PwC)

AI server shipments are expected to double in 2024, but while more PCB fabricators are entering the market, they don't expect price competition yet. (DigiTimes)

Global **semiconductor revenue** is projected to grow 16.8% in 2024, to $624 billion. For 2023, the market declined an estimated 10.9% to $534 billion. (Gartner)

The **PCB market** will grow 4.9% year-over-year in 2024, driven by gradual improvement in demand for consumer products such as mobile phones, PCs and notebooks, plus new applications such as electric vehicles, AI servers and satellite communications. (Prismark Partners)

Revenues among the **40 leading PCB suppliers,** which account for over one-half of industry sales, fell year-over-year but grew sequentially in Q3. Year-to-date aggregate revenues were down through September. (Prismark Partners)

SAVE THE DATE!

Engineering *Tomorrow's* Electronics

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EXHIBITION:
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Bureaucracy Blues

Over-the-top security controls can do more harm than good.

IS THE BUREAUCRACY of security making us all less secure? That is a question I find myself asking increasingly as layer after layer of bureaucracy in the form of forms, protocols and additional steps makes quoting, receiving orders, building product and then shipping and invoicing more cumbersome and time-consuming.

Don't get me wrong: I believe in quality and security, especially in the world we are living in and with the cyber-reliant environment we must utilize to communicate and share data among people and businesses. Increasingly, however, some measures that are intended to increase security instead have the effect of wasting time, adding cost and extending lead times to deliver much-needed product.

To wit: A customer requested a quotation for a few spare parts from a previous production run. To obtain the quote required logging on a "secure" website to download the RFQ and then uploading the completed quotation through the same web portal. The customer then sent an email notification that there was an order, again logging on the website to download the purchase order. In this case, the customer's quality clauses required both a new FAI and Source inspection. To comply, it required logging on the same web portal – twice. After Source took place, it required two more times of logging on the website to download documentation to ship. After shipping, once again it was necessary to log on the site to invoice. I added up the number of hours required to do the extra steps for this order and found it took longer to "process" the quotation, order and shipment than it did to produce the product in the first place! Had this part been technology-rich I might understand; however, this order was for pieces of shim stock!

It has not always been this way. A great example is the development of the P-51 Mustang. For younger readers, this was not a Ford automobile but a fighter aircraft, considered among the greatest fighter planes of its era. Back in World War II, a time where the need for security was as important as it is today, a team came together and in 30 days designed the P-51. A purchase order was placed, and 102 days later, the prototype was tested. After 44 more days, the plane was coming off production lines and successfully in service. That is 176 days from concept to being in service! How could it happen so fast? Clearly, with a war on, there was a pressing need, combined with a heightened sense of urgency by all. I suspect, however, there was also much less unnecessary paperwork and bureaucratic documentation. Time spent on anything unnecessary meant added time or delays in accomplishing the more important tasks.

Fighter planes of today are far more complex than those of 80 years ago, but my guess is that today the fastest a plane could go from concept to being successfully in service would be closer to 176 months, if even that fast. It should not take as long as it now does for more basic items to go through the quote/procurement/manufacture/ship/invoice processes, however. There is a real opportunity for improvement for companies to streamline the security and quality bureaucracy to be globally competitive technologically – and more importantly – in time to market.

More importantly, it is applying the appropriate inspection and security needed for different types of products, technologies and end-uses. One size does not fit all, and more is not always better. Some may want to simplify security protocols by making all components, all parts and all items for an end-product require the same levels of security. It appears a healthy dose of common sense is needed in many situations to simplify the basic and expedite the ability to respond and deliver.

Going back to my first example, is it necessary or does it provide any real value to require a Source inspector to go on site to inspect a shim? Or is the product it is going into more secure because such a basic part being inspected onsite. I later learned that this company made a blanket decision that all components of all types that go into a particular program require Source inspection. This one-size-fits-all decision will most likely cost critical time-to-market for the product and undoubtedly add significant and unnecessary cost to the end-product.

As technology advances, products become more complex all while the competitive tensions throughout the world heighten, so the need to be cognizant of preserving security and assuring quality is necessary. All should equally strive to be prudent when applying security protocols and inspection processes, however. Consider the part, component or processes' actual potential for security risk and then apply the appropriate level to the situation. Again, consider how much quality documentation is appropriate for each specific item. Clearly highly sensitive circuitry requires far more thorough quality review and levels of inspection, as well as greater security protocols, than a shim, washer or screw.

The goal should be to quickly develop and deliver high-quality product while doing so with the appropriate level of security. By investing some time to determine the appropriate levels of security differentiate the needed quality requirements will save time and money for all companies, departments and people involved.

PETER BIGELOW is president of FTG Circuits Haverhill; (imipcb.com); pbigelow@imipcb.com. His column appears monthly.

Engineering *Tomorrow's* Electronics

CONFERENCE: June 4 - 7
EXHIBITION: Wednesday, June 5

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DESIGNER'S **NOTEBOOK**

Printing Analog Circuit Elements Directly on the PCB

Prepare yourself for unusual circuit patterns.

THERE IS NO free lunch when it comes to populating a printed circuit board. Every part has a cost and a failure rate. One of the first projects of my career was a pulse-Doppler surveillance radar called PSTAR. In typical military jargon, that acronym stands for "Portable Search and Target Acquisition Radar."

My part was the amplifier module that was subdivided into various blocks for easy field service. One of the sub-blocks was a 20dB coupler. It lived inside its own hermetically sealed aluminum housing. The PCB inside had two traces that ran alongside each other, giving the circuit four ports with feedthroughs to the outside world. SMA connectors and semi-rigid cables wired the various modules together.

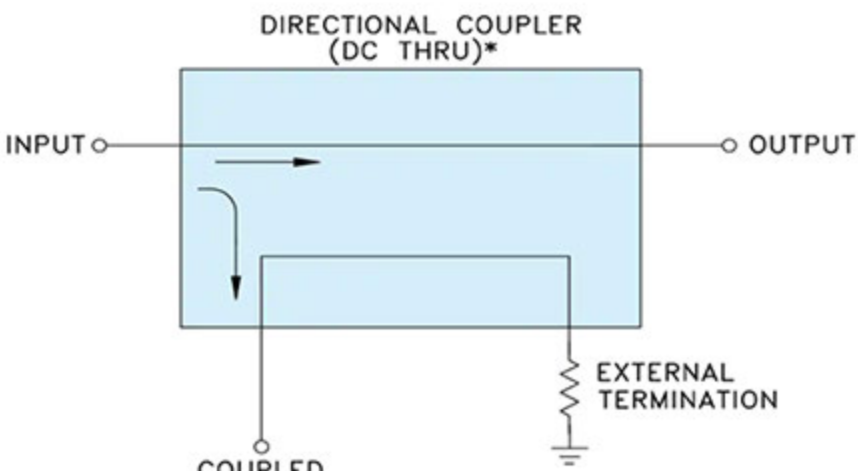


Figure 1. The typical broadside coupler will have the ports organized as shown while a quadrature hybrid coupler will flip the

output and termination port, which requires two layers on the PCB. (Source: Mini-Circuits)

My responsibilities included the little housing for the coupler, the overall mechanical packaging and all the semi-rigid cable drawings, as well as the RF amplifier. The control board was the only part designed by an external vendor. Meanwhile, the PCB for the coupler had no more than a single 50Ω termination resistor and the feedthrough connectors. We did not yet have PCB design software at that company, so this was done with AutoCAD.

That was back in 1990, but I still remember that simple board that was little more than a mirrored shape. At its core, the coupler is represented by the two transmission lines running parallel for a distance equal to a quarter of one wavelength of the resonant frequency, which was 13cm; somewhere in the 900MHz range. That type is known as a directional coupler.

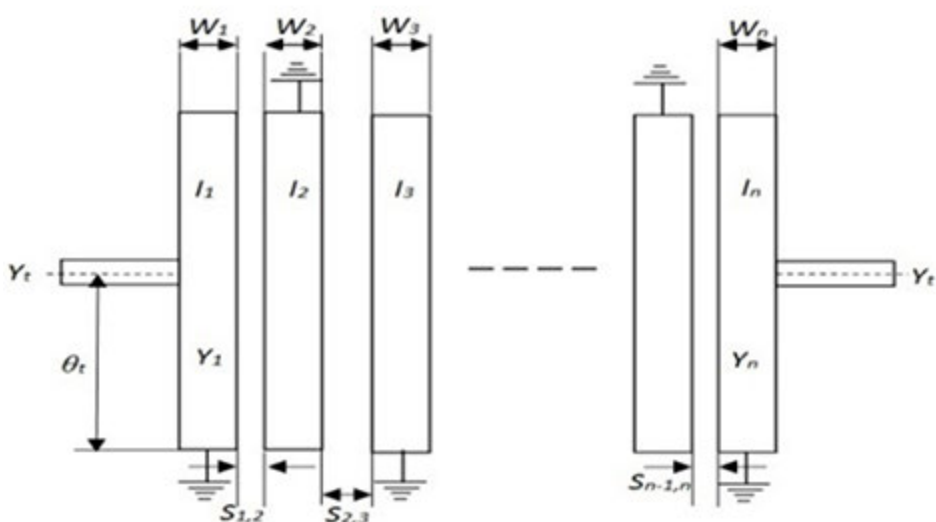


Figure 2. The interdigital bandpass filter bears a strong resemblance to this diagram. (Source: International Journal of Scientific & Engineering Research)

Quadrature hybrid couplers. Another type, a quadrature hybrid coupler, can also be printed, although the transmission lines are created on adjacent layers. The trick here is that layer-to-layer registration becomes important, particularly as the lines get thinner. Due to stackup realities, the 50Ω stripline may be something like 100μm. Now, if the layer-to-layer misregistration is 25μm off in the direction that affects the two lines going belly-to-belly,

then the coupling will drop off 25%.

Facing this exact problem, I went to the PCB West conference carrying a rolled-up blueprint with fab notes regarding the layer-to-layer constraint among other challenges. This was rather unexpected among the PCB fabrication vendors on the exhibition floor, but they would all stop what they were doing when I unrolled that D-size print. Most of the vendors had to pass on the chance to do this job but a few would take on the precise registration spec by imaging both sides of the core simultaneously.

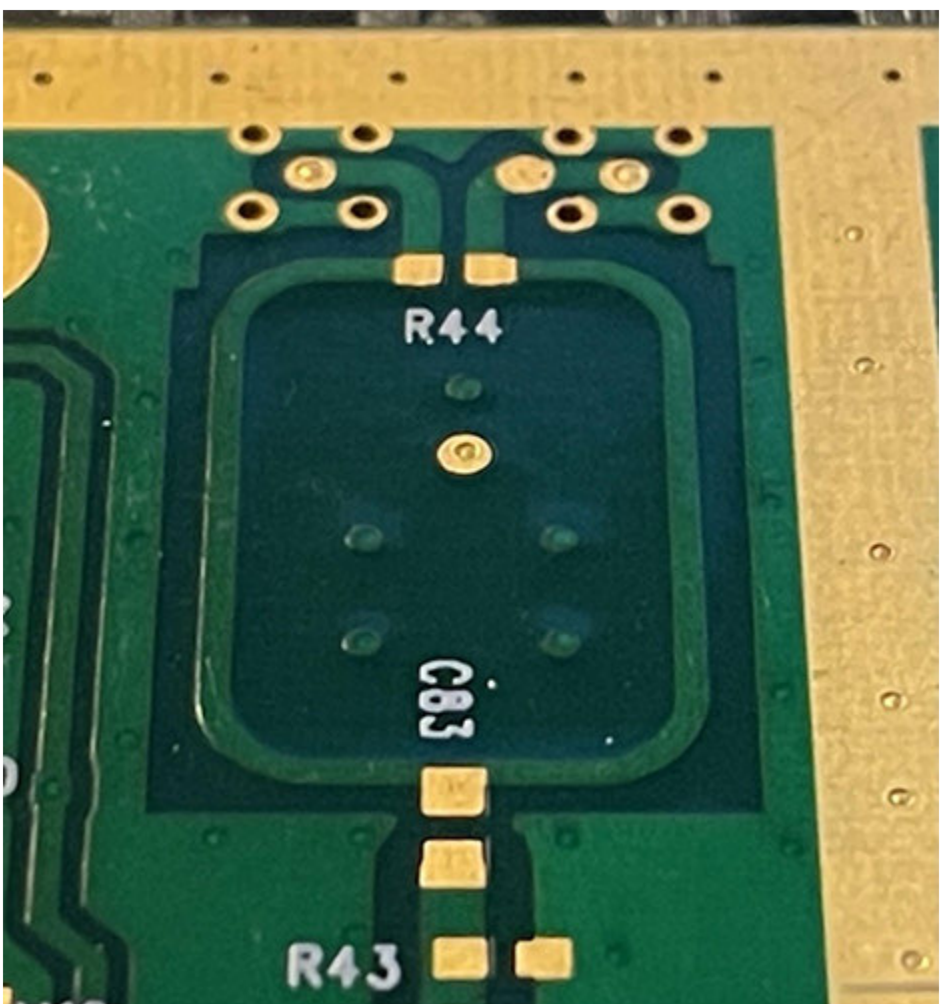


Figure 3. A Wilkinson divider circuit as part of a feed-forward correction board that controls the amplifier at the base of a cellular tower. In many cases, the solder mask is opened, leaving only a thin dam to contain solder on the SMD pads. (Source: Author)

Interdigital filters. Another type of component that can be etched rather than placed on the board is the interdigital filter. This circuit element owes something to the broadside coupler

element. Microwave signals propagate across fairly wide gaps, making this a more manufacturable item, which would be printed on the outer layers. The stub length is again determined by the 1/4 wavelength. The rest is a complex mathematical formula.

Wilkinson combiners/dividers. When you want to combine or divide RF transmission lines without inducing a phase shift, the Wilkinson element comes in handy. To be fair, this does require a balance resistor at the business end. As you may have guessed, the length of the lines is determined by the resonant frequency (wavelength) of the radio. We're looking at about 3cm on each branch in this case.

Finally, a printed inductor. This one was a bit tricky since the trace goes from a signal net directly to ground. The squared off spiral inductor in **Figure 4** extends from the transmission line and ends with a via to ground. Of course, it is also surrounded by ground pour that we don't want shorting to the signal path. A route keep-out around the edges provides that assurance.

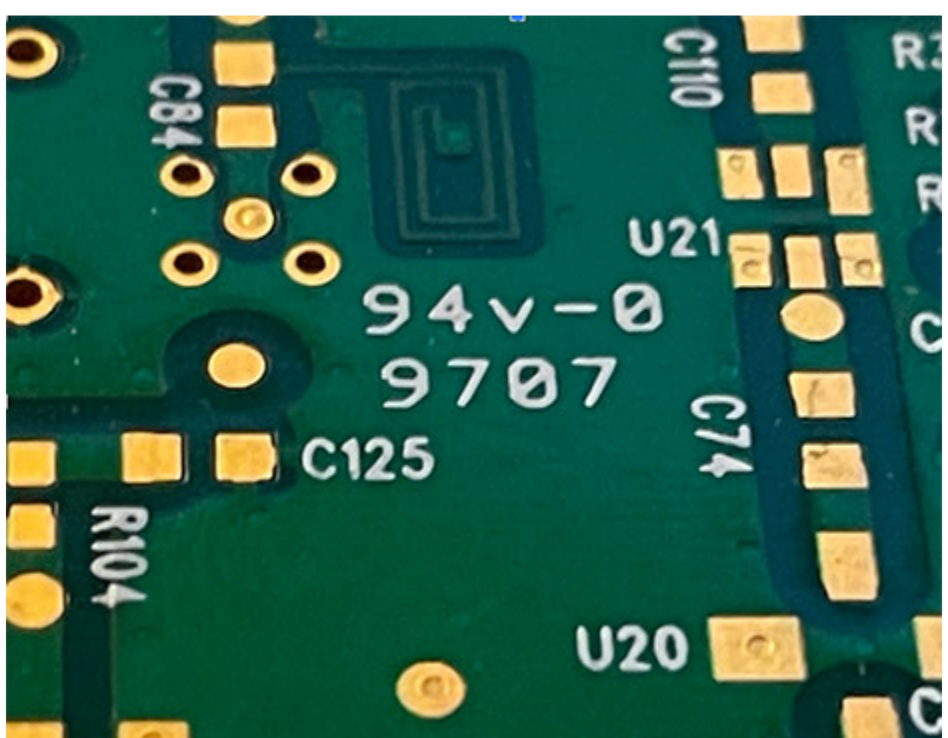


Figure 4. The same PCB as in Figure 3, and noted for being the first layout I did using Cadence Allegro. The 1997 date code puts this in the early 3G CDMA era. (Source: Author)

It seems that analog boards lend themselves to unusual circuit patterns. Matching networks can include tuning stubs that can be cut or extended with little copper tabs. Stray noise can be isolated with a band of grounded copper. Thermal dissipation can be enhanced with a tightly spaced grid of vias on an exposed copper plane. Replacing resistors, filters and heatsinks may take some PCB real estate, but earns it back by reducing the BoM cost, along with the potential for mitigating assembly defects.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

DESIGN **BEST PRACTICES**

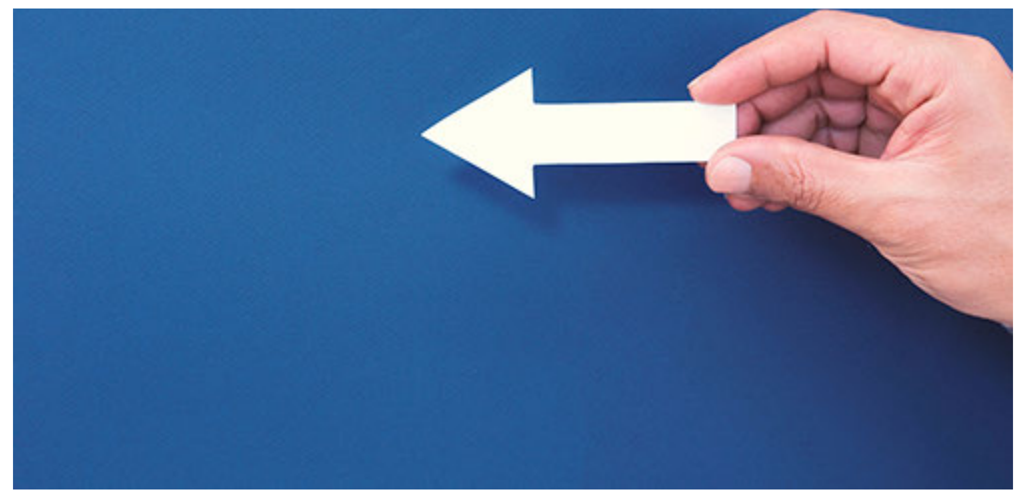
Analysis on the Move

Shifting critical processes "left" is a more proactive approach to testing and validation.

PRINTED CIRCUIT BOARD (PCB) design is a critical aspect of electronics product development, influencing the overall functionality, reliability and performance of electronic devices. Understanding the significance of analysis in PCB design and emphasizing its role in ensuring the integrity of electronic systems is key to success. The rapid evolution of electronic devices demands increasingly sophisticated PCB designs. As electronic components become more compact and complex, the need for thorough analysis in the design phase becomes paramount.

Analysis in PCB design involves evaluating various factors such as signal integrity, thermal performance, power distribution, and electromagnetic interference to guarantee the functionality and reliability of electronic systems. Implementing analysis early in the design cycle contributes to the optimization of PCB layouts, signal integrity and electromagnetic compatibility (EMC), thermal management, power distribution and overall functionality.

Surprisingly, many teams still choose to skip the analysis step entirely in an attempt to reduce project schedules and cost. This often causes costly project delays and increased cost downstream due to issues that could have been addressed if an analysis had simply not been skipped.



The ever-evolving landscape of electronics systems design demands a true paradigm shift in the approach to analysis, and that is "shifting left." We'll explore the principles, methodologies and advantages of shifting left analysis in PCB design, aiming to accelerate innovation and enhance the reliability of electronic systems.

Traditionally, the PCB design process followed a sequential approach, with testing and validation occurring towards the later stages of the flow. Shifting left analysis proposes a proactive strategy by moving testing and validation processes earlier in the design cycle, enabling rapid identification and resolution of potential issues before it's too late.

Principles of shifting left analysis:

- **Early integration of analysis tools.** Integration of simulation tools at the early stages of design enables engineers to assess the performance and reliability of the PCB. Analyzing signal integrity, power distribution and thermal considerations early on helps in making informed design decisions and preventing respins.
- **Collaborative design environment.** Collaboration between different design disciplines (electrical, mechanical and software) is crucial for a successful shifting left strategy. Early engagement of cross-disciplinary teams facilitates quick identification and resolution of design conflicts.
- **Automated design verification.** Leveraging automated design verification tools ensures that design rules and constraints are checked continuously throughout the design process. This reduces the likelihood of errors and accelerates the identification

of potential issues.

Methodologies in shifting left analysis:

- **Design for reliability (DfR).** Incorporating DfR principles early in the design process ensures that reliability is built into the product from the outset. Analysis of failure modes and stress factors aids in the development of robust and reliable PCBs.
- **Virtual prototyping.** Utilizing virtual prototypes (the digital twin) enables designers to assess the behavior of the PCB in a simulated environment. This allows early detection of design flaws and optimization for performance and reliability.
- **Continuous testing and validation.** Implementing continuous testing and validation processes ensures that the design is rigorously evaluated at every stage. Early identification of issues minimizes the likelihood of costly design changes later in the development cycle.

Advantages of shifting left analysis:

- **Faster time to market.** By addressing potential issues early in the design process, the overall time to market is significantly reduced.
- **Cost reduction.** Minimizes need for costly redesigns and reiterations, leading to cost savings in the product development cycle.
- **Enhanced product reliability.** Early identification and resolution of design issues contribute to the development of more reliable and robust PCBs.
- **Improved collaboration.** Cross-disciplinary collaboration is enhanced, fostering a more integrated approach to product development.

The importance of analysis in PCB design cannot be overstated. Thorough analysis is a proactive approach to identifying and addressing potential issues before they manifest in the final product. Signal integrity analysis, schematic analysis, thermal analysis, power distribution analysis, EMC analysis and manufacturability analysis collectively contribute to the optimization of PCB layouts, ensuring reliable and high-performance electronic systems.

Shifting left analysis is a transformative approach to PCB design that offers substantial benefits in terms of speed, cost and reliability. Embracing this methodology enables designers to proactively address potential issues early in the development cycle, ultimately leading to more innovative and reliable electronic products.

As technology continues to advance, the role of analysis in PCB design will only become more critical in meeting the growing demands for smaller, faster and more reliable electronic devices. The adoption of shifting left analysis in PCB design is poised to become a cornerstone of success in the electronics industry.

STEPHEN CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience and integrating the design-to-source Intelligence insights from Supplyframe into design for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com.

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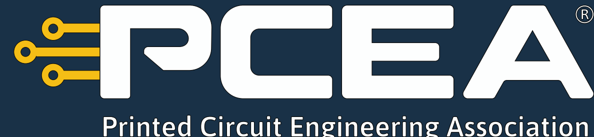

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MATERIAL **GAINS**

Who Will Own AI-Built Designs?

Generative AI could transform product design, but raises questions about creative ownership.

THE RECENT OUSTING and subsequent rehabilitation of OpenAI's CEO added some theater to the debate and buzz around artificial intelligence. AI, it seems, is everywhere and in everything from our smartwatches and phones to automobiles, data centers and factories.

With the explosion in generative AI like OpenAI's ChatGPT, it's also taking on creative roles that we might have assumed would remain the preserve of human intellect. For a while now, it has been possible to generate realistic images of human faces – not copies but unique individuals that never existed except inside a computer. Also, in 2023, the fashion brand Levi's became one of the first companies to suggest it would use AI-generated clothing models. These are expected to improve the shopping experience for customers by helping them assess clothes on likenesses that have a similar body shape and size to their own. Of course, it's also likely to help brands cut marketing and merchandising costs.

Let's set aside the prospects for the first AI catwalk model, or photographer, or bestselling novelist, and consider activities at the border between engineering creativity and design automation.

AI-based design tools are entering a variety of industries and could transform the way companies create new products. Tools like ChatGPT and Microsoft's Copilot can learn from literally thousands of worked examples to help engineers with relatively minimal coding skills quickly generate software like an embedded application or automated test routine.

There are further roles for AI in reliability engineering and analysis. I was speaking recently

at an event hosted by the European Space Agency about circuit boards for space applications. Of course, repairing failed units in space is practically impossible, so reliability is critical. The accumulated experience of space engineers in designing high-reliability systems is essential for commercial operations to be economically viable. Bringing that expertise into AI-based tools, which can continue to learn from ongoing experience and so design progressively better and more reliable systems in the future, will be important for developing the sector.

Here on earth, some forward-thinking PCB design houses are already experimenting with generative AI to assist with placement and routing of components on PCBs, using libraries of existing design examples. We can expect that generative AI will enter the toolchain in specific features and functions and subsequently become more prevalent as users understand its ability to make their lives easier and get new designs to market more quickly.

Top designers acquire their skills through years of learning and experience. As human experts age, and inevitably retire, their industries can lose the benefit of this knowhow. Traditional mechanisms for sharing knowledge have included mentoring, conference proceedings and literature, which others can study and in turn become the next generations of experts. Now, we have the opportunity to train AIs on the collective expertise of all the world's subject specialists. These can then continue to learn, improve and update, becoming ageless, always current, and accessible to a broad user base.

On the other hand, there are important questions regarding intellectual property. Some vendors of AI-based tools have sought to claim ownership of material generated by users. For its part, Microsoft has faced challenges over Copilot's reliance on open-source code for training. A judgment against the company could seriously slow development and adoption of generative AI in many areas. Other legal action is building as groups such as writers and artists claim that AI is training on their created material without consent. The dispute between Microsoft and its challengers is over the terms of the open-source license agreement, which places restrictions and obligations when code is taken from repositories such as GitHub. The arguments are far from clear cut as many current licensing and copyright laws originate from eras before generative AI. A judgment could set an important precedent. Both sides know the stakes are high.

Back in the more straightforward world of high-tech product design, bringing AI into EDA tools could help engineers create products that are easier to build, test, approve, and maintain. For many years, designers have been encouraged to consider multiple aspects as early as possible in the design process: design for test, design for manufacture, consider antenna placement, power consumption, electromagnetic compatibility. With so many aspects to prioritize, engineers could be forgiven for being unable to consider everything at the same time. AI-based tools, on the other hand, can deal with numerous issues and variables simultaneously to work out the best possible compromise, also considering supply chain issues like the availability of components, PCB materials and fabrication services, as well as optimizing for recycling and disposal at end-of-life.

In previous columns, I've referred to humans' tendency to overestimate the impact of new technologies in the short term and underestimate their effects in the long term. It's probably not contentious to suggest that everyone knows AI is going to have a huge influence on many aspects of our lives and is likely to be more transformational than the Internet. Protection is certainly needed, so we should take interest in the development of new regulations like the EU AI Act, which could become the first law of this type in the world, and international forums like the AI Safety Summit. First held at Bletchley Park in the UK last November, it could offer the prospect of a global accord to minimize the risks and maximize the opportunities for all of us.

ALUN MORGAN is technology ambassador at Ventec International Group (ventec-group.com); alun.morgan@ventec-europe.com. His column appears monthly.

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ROUGHLY **SPEAKING**

Sintered Copper Can Handle the Pressure

> A tech conference presentation spurs study of an exciting material option.

I LIKE TO ask designers about interesting projects or technologies they have worked on, and I heard from two designers, whom I met through my local PCEA chapter, about some very interesting and complex boards they designed using sintered copper. Both had used sintered Ormet Transient Liquid Phase Sintering Paste (TLPS) to design boards that would not have been possible otherwise. (There are a couple different vendors for sintered copper for vias, but I looked further into Ormet materials, as that was the material used in both the boards they told me about.) These boards were complex, with a lot of parts, limited space, RF signals with antennas and sensitive digital components, and I was told these boards would have been impossible to design without the sintered copper to create any-layer vias connections.

The Ormet paste provided a path forward to route, but this wasn't the first time I encountered this material. I first heard about it in 2014 from a fabricator that wanted to be able to document these types of vias in their stackup. In the past two years, however, I heard more and more requests for it from both designers and fabricators. What is it, and why has it taken so long to get traction in the PCB industry? This prompted me to put on my investigation cap and pursue some answers.

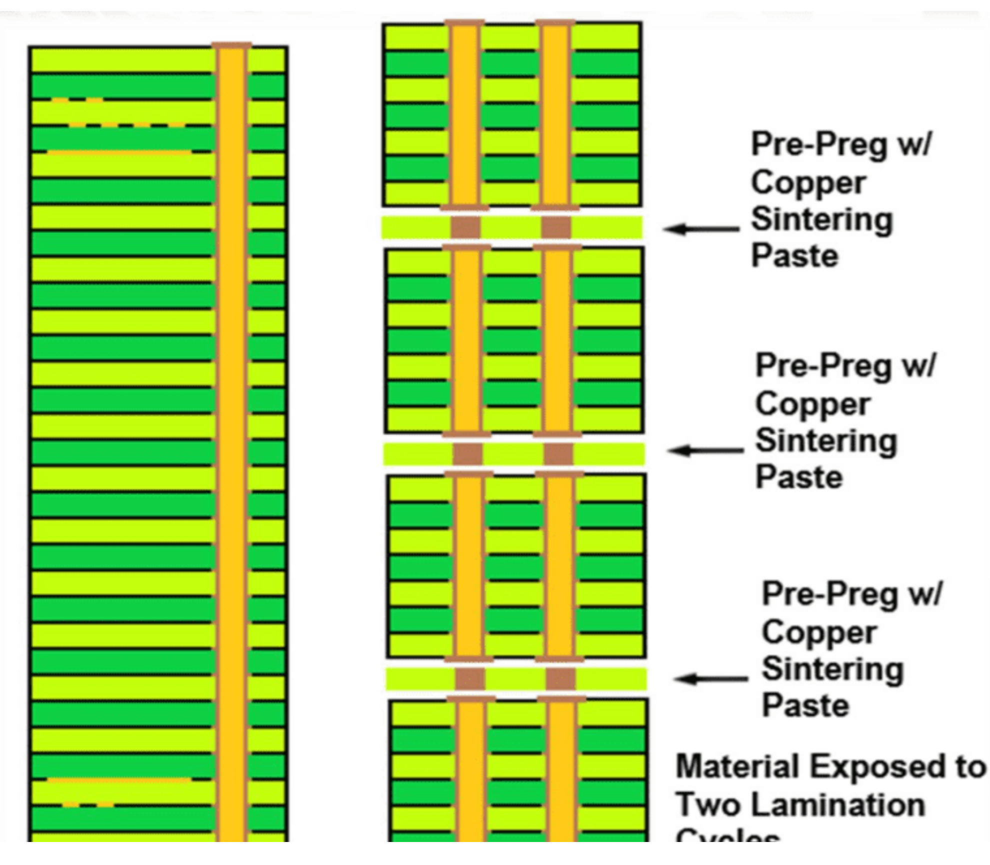
It turns out I wasn't the only one interested in these types of materials, and I was truly sparked to delve deeper into the sintered copper vias at PCB West 2023, after attending a presentation by Sean Nodado of Analog Devices, titled "Sintered Vias for HDI PCB Design." It was well-attended and focused primarily on their reliability testing of such vias. But many

of us in the audience didn't have a solid understanding of the uses and benefits to fully appreciate the research from Analog Devices showing strong reliability results and why that was significant. As it turned out, the fabricators I spoke with following the presentation frequently commented that sintered copper vias had reliability issues. Sean and his team were just ahead of the rest of us in the room, in that they had already grasped the potential of the sintered vias, and were addressing one of the roadblocks.

So why would one want to use sintered copper paste in the first place?

The ability to electrically connect two cores or sub-laminated sections together without drilling through the entire section and then going through the plating process can be both a significant time- and cost-saver on the manufacturing side, as well as a huge win for the designer.

By removing previously necessary drills/vias/backdrills from the board, huge swaths of layout real-estate can be reclaimed for laying traces for interconnects. Smaller vias reduce space taken up by keepout zones, and eliminating some drills entirely frees up even more space. And assembling subsections together **(Figure 1)** can reduce the need for expensive high-aspect ratio drilling.



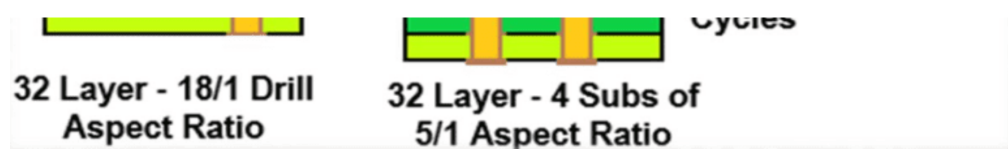


Figure 1. Assembling sub-laminated sections reduces aspect ratios and drill times.

Boards need to be symmetrical in material construction and properties or else disastrous consequences can arise in board warpage and cracking during the manufacturing process. Often RF designers are looking to incorporate exotic materials for an antenna, but then the antenna and analog signals need to connect to the digital components interfacing with analog components. One can connect a sub-lamination RF board and a sub-lamination digital board with sintered copper vias without creating parasitic vias through both boards and without disturbing the layout on each **(Figure 2)**. As such, a buried via can go anywhere on the board, without the need for backdrilling. This allows a designer to create the digital and analog sections of a board in the same vertical space, with one side of the board the RF and the other digital, rather than separating them on the X-Y plane, thus saving space **(Figure 3)**.

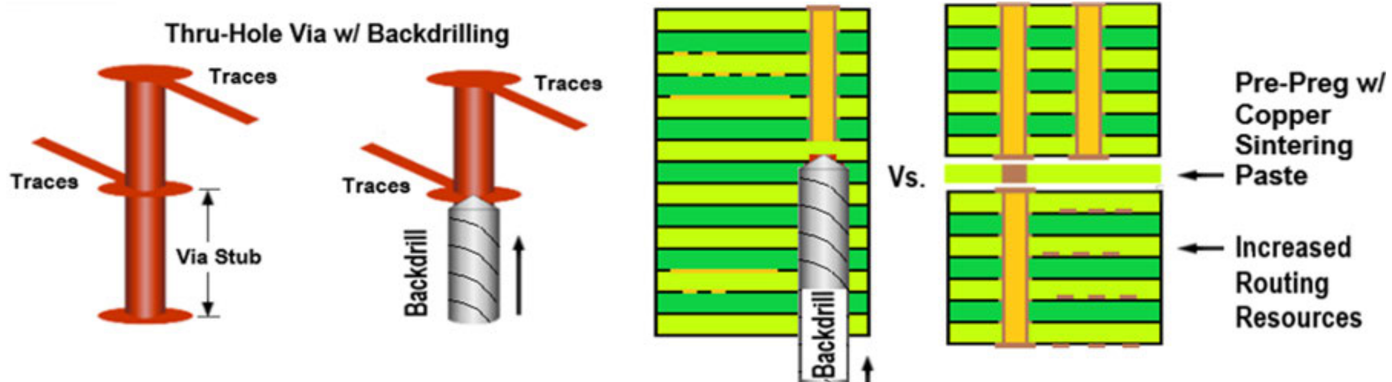
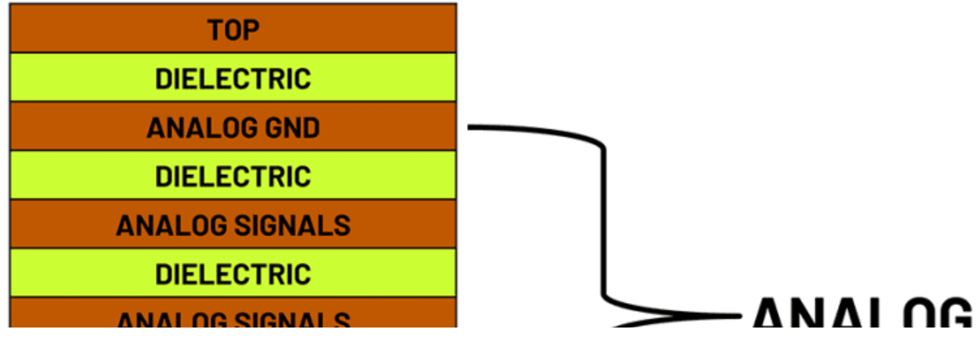


Figure 2. Sintering paste can eliminate backdrilling.



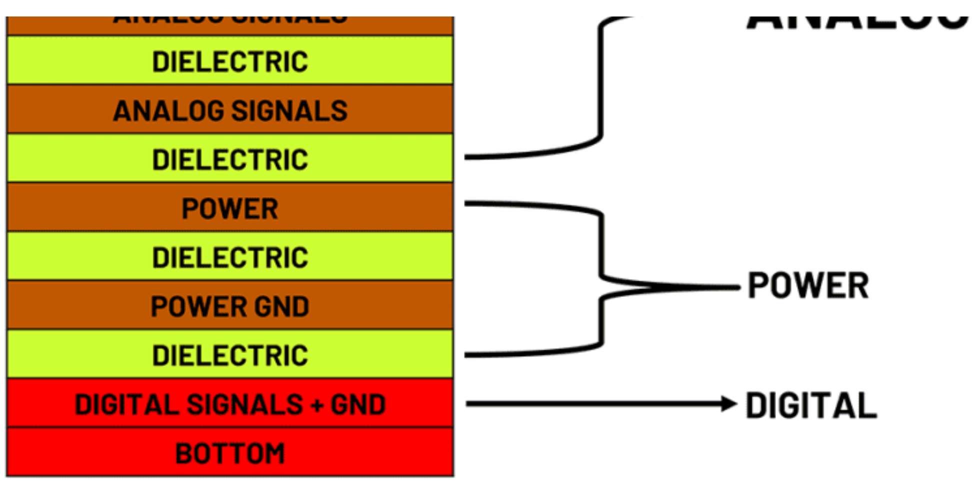


Figure 3. Digital and analog signals can occupy the same vertical plane of a board.

One might reasonably ask, then, why hasn't this caught on more? It seems multiple issues are compounding and working together to prevent further adoption.

Fabricators are not very familiar with these materials, and even when requests to use them come in, they aren't standard. Adding to the infrequent use, each different sintered copper material supplier has its own process/procedure that needs to be followed precisely, and these processes are not very similar. Another potential roadblock, as expressed by several of the PCB fabricators I spoke with, sintered vias and pastes were difficult to work with and have reliability problems.

Digging further, I learned that some of the reported reliability problems were false negatives. Those that were true failures were often the result of the fabricator's inexperience with that specific chemistry. Of the sintered pastes I looked into, each had its own complexities in working with them. And, just like laminates, they have limited shelf lives. Infrequent usage of the sintered pastes often resulted in failures due to inexperience with the materials, as well as unfamiliarity with the process necessary to use them properly. A Catch-22; if the fabricator doesn't use it frequently and often, they are more likely to have issues in processing, and thus, subsequent reliability issues, discouraging future attempts. Unfamiliarity breeds blame: When something goes wrong on a board that has sintered copper, the "new stuff" is often the first variable to be blamed.

Additionally, reliability test methods used by the industry would flag boards as failures when

in fact they improved. For Ormet, the first thermal cycle of the board, for example, as part of reliability testing results in a transition of the copper and tin mixture to one with lower conductivity. The reliability test evaluates the resistivity of the vias and flags significant changes from the pre-thermal cycled measurement as failures. The Ormet sintered copper via's resistivity decreases, flagging the board for failure, when in fact, it is perfectly fine! One would more likely expect the resistance to rise for failures in the case of an open or cracked via. (Speaking with some industry experts on the topic, there was unanimous agreement that D-coupon testing was the better method for identifying via failures.)

Designers were also hampered for some time by the CAD tools not permitting any-layer vias to be designed into boards. (For design tools that perform rule checking, a drilled and copper-filled via that goes through only a sheet or two of only prepreg, to connect the outer layer of two cores, does seem like something that should be flagged with a warning like "Oh, hey, designer! You can't do that!") These days many CAD tools have moved in the direction of guiding designers on what is manufacturable under the general concept of "design for manufacturability." But these design rule checks, without being properly updated with the latest technology trends, were hindering new technology. How could a designer communicate to a fabricator that they wanted to have a lasered via with sintered copper to create an any-layer via when their documentation and design software wouldn't allow it?

Lack of familiarity and awareness, reliability concerns, and CAD limitations have all hindered sintered copper vias from jumping into the mainstream. Given the interest in the presentation at PCB West, I would be surprised if more fabricators didn't start seeing more requests for using these materials.

Thank you to Mike Creeden, Geoffrey Leeds, Chris Hunrath, and George Harris for their assistance in answering my many questions about Ormet TLPS.

GEOFFREY HAZELETT is a contributing editor to PCD&F/CIRCUITS ASSEMBLY. He is a technical sales specialist with more than 10 years' experience in software quality engineering and sales of signal integrity software. He has a bachelor's degree in electrical engineering; geoffrey@pcea.net.

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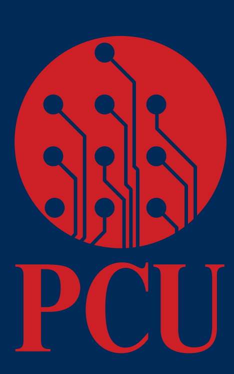

CURRENT TEMPERATURES

Electrical and Thermodynamic Parallels

Copper can conduct current and heat, but board materials conduct only heat.

by DOUGLAS BROOKS, PH.D. and DR. JOHANNES ADAM

Most PCB designers have had at least some exposure to electrical engineering principles and fundamentals. For example, they have some understanding and a working knowledge of such things as current, voltage, power, resistivity and resistance. But most designers have had almost no exposure to thermodynamics. And thermodynamic fundamentals are very relevant when it comes to such things as determining how much current a trace can carry (and how hot it will get), how to cool a heated component's pad, and what role a copper plane might have in distributing heat across a board, for example.

It turns out the parallels between electronics and thermodynamics are much closer than most imagine. For example, current is the motion of "charge" (coulombs) under the "force" of a voltage difference, while heat flux is the flow (from warmer to cooler) of "heat" under the force of a temperature difference. Thermal resistance and thermal conductivity are analogous to electrical resistance and electrical conductivity.

This article intends to provide enough parallel information on the two disciplines that board designers can at least begin to understand the basic principles of thermodynamics that they often have to deal with.

In electronics, the basic particle we deal with is the electron, sometimes referred to as an

"elementary charge." The basic unit of charge is denoted as a coulomb, "C." The movement of charge becomes "current" (Notes 1 and 2). One unit of "charge" is denoted as, q, the amount of charge represented by 6.25×10^{18} electrons. One amp, A, of current is the movement of one coulomb of charge across a surface in one second of time (A = coulomb/sec). The basic unit in thermodynamics is "heat" (Q), equal to the energy required to raise the temperature of one gram of water by 0.239 degrees Kelvin (K). The unit of heat energy is the joule. The parallel to electrical current is heat flux, $\dot{Q}$, which is heat per unit of time, or J/sec. One J/sec is one watt (W). So, so far, we can show the relationships as in **Table 1** (Note 3).

Table 1. Relationships between Electrons and Heat Units

Electronics					Thermodynamics				
Term	Sym.	Desc.	Formula	Units	Term	Sym.	Desc.	Formula	Units
Elementary Charge	e	Charge on a proton or electron							
Charge	q	Charge on 6.25×10^{18} Electrons		C = A*sec	Heat (energy)	Q	Energy required to heat one gram of water by 0.239 K		J
Current	I	"Flow" of charge	A = C/sec	A	Heat Flux	$\dot{Q}$	Heat per unit time	J/sec	W
Force	V	Difference in volt.	ΔV	V	Temperature	T	Difference in temp.	ΔT	C or K

So far, this is just a barely interesting set of definitions. Of more interest is comparing how heat flux flows compared to how current flows. This directly applies to how we cool a heated trace.

All elements and materials (at least those relevant to us) have a property called *resistivity*. It is a measure of the element's ability to *resist* electronic current or thermal heat flow. These elements also have a property called *conductivity*, a measure of the element's ability to *conduct* electronic current or heat flow. The relationship between resistivity and conductivity is very simple; conductivity is the inverse of resistivity. That is, conductivity = 1/resistivity, whether we are referring to electronics or thermodynamics.

For example, we ought to be aware that copper has a very low resistivity, ρ; only silver has a resistivity that is lower. The units of resistivity are ohms-distance, e.g. 1.65×10^{-8} ohm-meter for copper. Its conductivity, σ, is the inverse, or 5.98×10^{7} /ohm-meter. We get the electrical resistance of, say, a trace by the formula $R = \rho * L / A$, where A and L are the cross-sectional area and the length of the trace, respectively. The units of resistance are ohms. The conductance (G) of a trace is just the inverse, $G = \sigma * A / L$ /Ohm. It is much more common for us engineers to deal with resistivity and resistance than it is for us to deal with conductivity and conductance.

Thermal resistance and conductivity are perfectly analogous. Except that it is much more common for us to deal with thermal conductivity and conductance than to deal with thermal resistivity and resistance. The thermal conductivity coefficient of a material, k, has units of W/mK (watts per meter per degree Kelvin). Thermal conductance is given by k*A/L, and (predictably) thermal resistance, R_Θ, is given by R_Θ = L/kA. We can summarize all this in **Table 2**.

Table 2. Thermal Resistance and Conductivity

		Electronics			Thermodynamics		
Term	**Desc.**	**Symbol**	**Formula**	**Units**	**Symbol**	**Formula**	**Units**
Resistivity	Resistance to Current/heat flow	ρ		Ohm-m	none	1/k	mK/W
Conductivity	1/Resistance	σ	1/ ρ	1/Ohm-m	k		W/mK
Resistance	Resistance to current/heat flow	R	ρ *L/A	Ohm	R_θ	L/(k*A)	K/W
Conductance	1/Resistance	G	σ*A/L	Mho or Siemens	none	k*A/L	W/K

Our real interest in writing this and future works relates to the electrical and thermal performance of traces and vias. Three questions we will be focusing on in particular in future articles are:

1. Is via resistance important?

2. How much current can a via safely carry?

3. Can thermal vias be effective?

In the following paragraphs we use numerical examples for illustration. The calculations are very straightforward, as suggested above. Except, the calculations can *seem* difficult because they often involve unit conversions that themselves involve a lot of decimal places that are difficult to track. So, we are going to make a few basic calculations that will be useful as we go along.

Table 3 provides a few calculations in various units, so we don't have to worry about them in the various examples to follow (recall 1 meter is approximately 39 inches, and one inch is 1000 mils).

Table 3. Useful Calculations

Some Useful Calculations			
	Dimensional Units		
Parameter	**Metric**	**Inches**	**Mils**
Electrical Resistivity, ρ copper	1.65 uOhm-cm	0.676 uOhm-in	0.000676 uOhm-mil
Therm. Cond., k, typical board material	0.7 W/mK	0.0179 W/inch*K	0.0000179 W/mil*K
Therm. Cond., k, copper	395 W/mK	10.128 W/inch*K	0.010128 W/mil*K
Area, 10 mil dia. drilled via hole, $\pi r1^2$		0.000078540 in^2	78.54 mil^2
Conducting area, via plated to 1mil thickness, $\pi(r1^2-r2^2)$		0.000028.28 in^2	78.54 – 50.27 = 28.28 mil^2
Unfilled via cavity, $\pi r2^2$		0.000050.27 in^2	50.27 mil^2

An electrical conductor has a very low resistivity. From above, the resistivity of copper is $1.65\times10^{-8}\Omega$-m ($0.676\mu\Omega$-in). Therefore, it has a high electrical conductivity. As it turns out, pure (plated) copper also has a high thermal conductivity, about 395W/mK. A typical board material has a very low electrical conductivity, almost zero from a practical standpoint. But its thermal conductivity, while low, is not zero. It is around 0.4 to 0.8W/mK. A board's thermal

conductivity is still higher than the combined effects of convection through still air and radiation (at the board's surface without supplemental cooling.) We know this because we learned through IPC-2152 that internal traces are cooler than external traces of the same size carrying the same current. Although a typical dielectric has a very low thermal conductivity, it has a large impact on trace and component temperatures because of its relatively large volume. Very few circuits could survive if they were mounted on thermally isolating materials.

Therein is one of our first recognitions: copper can conduct current and heat, but board materials conduct only heat. And we may be able to use copper as a board material for just the purpose of conducting heat (think thermal via, isolated pad, or plane).

Electrical resistance; trace or via: We can easily calculate the electrical resistance of a copper trace and/or via. The electrical resistance is

$$R = \rho * L / A$$

Assume we have a 26-mils-wide, 6″-long, 1.0-mil-thick copper trace. Its conducting cross-sectional area is

$A = 26*1.0 = 26\ mil^2 = 0.000026\ in^2$, resulting in a resistance of
$R = 0.676*6/(.000026) = 156m\Omega$

Or suppose we have a 10-mil diameter, 63-mil-long via plated with 1.0 mil copper. Its conducting cross-sectional area is $\pi R1^2 - \pi R2^2$, where R1 and R2 are the outer and inner radii, respectively:

$A = \pi(.005^2 - .004^2) = 28.28\ mil^2 = 0.000028.28\ in^2$, resulting in a resistance of
$R = 676*.063/.00002828 = 1.51m\Omega$

Note that we constructed this example so that the trace and via had approximately the *same* conducting cross-sectional areas, about 28 mil^2. The trace has about 100 times more resistance than the via because it is about 100 times longer than the via. (Note: Usually via resistances are small compared to trace resistances.

Thermal resistance; via: The calculation for the thermal resistance of, for example, a via wall, is very similar. The formula for thermal resistance is (compare with the formula for electrical resistance, above) $R_\ominus$ = L/kA, where k is the material conductivity coefficient (remember, conductivity is the inverse of resistivity). The k value for copper is about 395W/mK, or about 0.01013W/mil K. The via wall conducting cross-sectional area, from above, was 28.28 mil^2. So, the thermal resistance of the via wall is

$$R_\ominus = L/kA = 63/(28.28*0.010128) = 220.0 \text{ K/W}$$

And the thermal conductance of the via wall is $1/R_\ominus$ = 0.00455 W/K

Let's compare that to what the thermal resistance and conductance of the total via cross-sectional area *would* be if it was just board material with a k = 0.7W/mK. First, 0.7W/mk is equal to 17.9 x 10^{-6}W/mil-K. The cross-sectional area of a drilled hole of 10 mil diameter is $\pi*(5^2)$ = 78.5 mil^2. So, the thermal resistance is

$$R_\ominus = L/kA = 63/(78.5*17.9\times10^{-6}) = 44.8 \text{ x } 10^3 \text{K/W}$$

And the thermal conductance is $1/R_\ominus$ = 22.3 x 10^{-6}W/K

Thermal via effectiveness. Consider whether a thermal via *ought to be* effective. A thermal via of the size we have been assuming has a thermal *resistance* of 220.0K/W while the volume of board material it replaced had a thermal *resistance* of 44.8 x 10^3K/W. The thermal *resistance* of the board material is about 203 times greater than that of the copper via that replaced it.

By this analysis, the thermal via *ought* to be much more effective at removing heat from a heated pad. We will show in the next couple articles why that is typically not true. But for now, at least, you see the thermal calculations closely follow the electrical calculations we are very familiar with.

NOTES

1. For a thorough discussion of how current flows in a conductor see Douglas Brooks, "UltraCAD's Best Articles and Applications Notes," Chapter 1, "What Is This Thing Called 'Current?' Electrons, Displacement, Light, or What?", 2022, available on Amazon.com.

2. For some lists of electrical notations, see https://en.wikipedia.org/wiki/List_of_common_physics_notations or https://en.wikipedia.org/wiki/Electric_charge, or https://en.wikipedia.org/wiki/Elementary_charge.

3. This is a very simplified description of the various technologies. Refer to any textbook on electronics or thermodynamics for more depth.

DOUGLAS BROOKS, PH.D. has bachelor's and master's degrees in electrical engineering from Stanford and a Ph.D. from the University of Washington. He owned an engineering service firm and has published multiple books, including *Physics of Electronics for PCB Designers* and *PCB Design Guide to Via and Trace Currents and Temperatures;* doug@ultracad.com.

DR. JOHANNES ADAM, CID, is founder of ADAM Research, a technical consultant for electronics companies, a software developer, and author of the Thermal Risk Management simulation program. They will host a free webinar on Via and Trace Currents and Temperatures on Jan. 17, 2024.

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SIGNAL INTEGRITY

How to Calculate Transmission Line Impedance with Dispersion and Roughness, No Field Solver Needed!

Analytical formulas, plus Microsoft Excel, are all you need.

by ZACHARIAH PETERSON

Look at just about any expert-level signal integrity guide and you will (or rather, should) see a lot of simulation data. Most often, these results are generated with 3-D electromagnetic field solvers, even if the author is not performing simulations directly from a finished PCB layout. 3-D field solvers and 2-D field solvers are also used on the front-end to design and engineer an interconnect for a specific interface.

These applications take material inputs, intended geometry and stackup, and tell the impedance of a line. They can also return the impedance and propagation constant directly. More advanced fast field solvers, such as those from Simbeor or Polar Instruments, can provide full S-parameters for a transmission line, assuming a perfect 50Ω source and load.

Another way is possible to get to the lossy characteristic impedance and propagation constant, which can then be used to predict the S-parameters for a transmission line. This article shows how to do this without requiring a field solver, meaning the user will rely only on analytical formulas. The method shown here includes dielectric and skin effect losses, causal roughness losses, and causal dielectric constant (Dk) with dispersion, which only the most advanced PCB-specific field solvers currently include.

What is shown here was originally published by the author at IEEE EPEPS,[1] and the

equations can be solved in Microsoft Excel with a simple spreadsheet.

Start with the Lossless Impedance

The equations that follow describe the characteristic impedance of a transmission line as a function of frequency that includes loss terms. The result will have the following qualities:

- The resulting impedance will be a function of frequency
- The impedance will include a small reactive component due to the presence of losses
- The impedance will only be valid in the TEM limit.

The method shown calculates transmission line impedance with losses by starting from the lossless impedance, and the lossless impedance can be calculated from the line's geometry. Essentially, provided the lossless impedance is known, loss terms can be added back in to get the lossy impedance.

The basis for this is the RLCG model, which applies only in the TEM propagation limit. The RLCG model describes the characteristic impedance of a lossy transmission line, which includes terms for the dielectric loss contribution and the resistive loss contribution. These R, L, C, and G terms are per-unit-length circuit elements that would appear in the telegrapher's equations. The lossy characteristic impedance and each of these terms are defined in Equation 1. (Note: Definitions here are described in Zhang.[2])

$$Z_0 = \sqrt{\frac{R + i\omega L}{G + i\omega C}}$$

$$R(\omega) = R_{DC} + \sqrt{\omega} R_s \qquad L(\omega) = L_\infty + {K(\omega) R_s}/{\sqrt{\omega}}$$

$$G(\omega) = \omega C(\omega) \tan\delta(\omega) \qquad C(\omega) = K_g \varepsilon_R(\omega) \varepsilon_0$$

Eq. 1

Here, we have some additional terms within the RLCG terms that need to be defined. These are:

- Kg: Fringing field constant, which defines the line capacitance
- Rs: Skin resistance arising due to the skin effect
- K: Causal copper roughness correction factor as derived in Dmitriev-Zdorov.[3]

Next, using results from standard copper roughness models,[3] we must apply a causal correction to the dielectric constant as a function of the copper surface roughness as defined by a 10-point roughness measurement. The adjusted Dk with roughness is:

$$\varepsilon_c(\omega) = \varepsilon(\omega)\frac{t_{diel}}{t_{diel} - 2H_{10}}$$

Eq. 2

Note that the dielectric constant input on the right can already be a function of frequency, and it includes the imaginary part (loss tangent) in the standard definition. This means the causally corrected dielectric constant is also a function of frequency following the same trend. This has been shown in copious experimental data from Rogers[4] for a variety of interconnects.

As mentioned, the copper roughness correction factor is defined in Dmitriev-Zdorov.[3] This can be calculated by hand at any frequency for a given copper roughness model. Skin effect resistance also obeys a simple formula when the conductor has a rectangular cross-section:

$$R_s(\omega) \approx \sqrt{\frac{\mu_0}{8\sigma(T+W)^2}}$$

Eq. 3

Equation 3 is an accurate approximation for the skin resistance for a rectangular trace above a ground plane in terms of its width and thickness.

Converting Lossless to Lossy Impedance (Z)

Note that, when there is no loss along the transmission line, the characteristic impedance and speed of a signal will be equal to:

$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{L_\infty / K_g \varepsilon_0 \varepsilon_{c,R}(\omega)} \qquad v = \frac{c}{\sqrt{\varepsilon_{c,R}(\omega)}} = \sqrt{1 / L_\infty K_g \varepsilon_0 \varepsilon_{c,R}(\omega)}$$

Eq. 4

Equation 4 shows characteristic impedance (left) and speed of a signal (right) for a single-ended line without losses. The "R" subscript in the Dk refers to the real part of the dielectric constant.

The L and C values would normally be given by a 2-D cross-section calculator (boundary element method) or from a simple online calculator.

With these two equations, we can calculate a lossy impedance, provided the lossless impedance is known (detailed below). Note that there are two equations to solve, and two unknowns (lossy impedance and lossy propagation constant). This means lossless capacitance and lossless inductance can be eliminated easily using two simple relations from the lossless characteristics:

$$i\omega L_\infty + R_{DC} + \sqrt{\omega}(1+i)R_s = \frac{i\omega Z_0 \sqrt{\varepsilon_{c,R}(\omega)} + (R_{DC} + \sqrt{\omega}(1+i)K(\omega)R_s)c_0}{c_0}$$

$$G + i\omega C = i\omega \frac{\sqrt{\varepsilon_{c.R}(\omega)}}{Z_0 c_0}(1 - i tan\delta)$$

Eq. 5

Equation 5 shows inductance and resistance (top) and capacitance (bottom) for a lossy line.

Using these equations, we can simply take the quotient and get the square root to get the lossy characteristic impedance:

$$Z(\omega) = \sqrt{\frac{i\omega Z_0^2\sqrt{\varepsilon_{c,R}(\omega)} + Z_0 c_0 \left(R_{DC} + (1+i)K(\omega)R_s\sqrt{\omega}\right)}{i\omega\sqrt{\varepsilon_{c,R}(\omega)}\left(1 - i\tan\delta(\omega)\right)}}$$

Eq. 6

Instead of taking the quotient, we take the product and then take the square root to get the lossy propagation constant:

$$\gamma(\omega) = \sqrt{\frac{-\omega^2 Z_0 \varepsilon_c(\omega) + i\omega c_0\sqrt{\varepsilon_{c,R}(\omega)}(1 - i\tan\delta(\omega))(R_{DC} + K(\omega)(1+i)\sqrt{\omega}R_s)}{Z_0 c_0^2}}$$

Eq. 7

These equations look quite messy, so how exactly is all this used and what does it all mean?

The interpretation here is actually very simple: Provided the lossless characteristic impedance and material parameters are known, the lossy characteristic impedance can always be calculated. Just plug these known values into Equations 5 and 6, and all other signal integrity metrics can be predicted by hand.

How to Calculate the Lossless Impedance (Z_0)

Those familiar with IPC-2141 or the groups of equations in Brian C. Wadell's *Transmission Line Design Handbook* will know that the lossless characteristic impedance is a function of the trace geometry and dielectric constant. This also means that the lossless dispersionless impedance result from a 2-D calculator can be converted to a lossy impedance.

Z_0 could be calculated using one of the following methods with the desired trace geometry:

- The microstrip or stripline formulas in IPC-2141
- An empirical model for lossless impedance
- The formulas in Brian C. Wadell's textbook
- Any other analytical relationship that defines lossless characteristic impedance.

Any of these groups of equations shows the lossless impedance as a function of the trace geometry and dielectric constant. Those who have dielectric constant data from a PCB material datasheet can calculate the lossless impedance as a function of frequency. This can be gone with a bulk Dk value graph from the laminate vendor, or the vendor's tabulated Dk data, which can be input into the lossless impedance equation.

The lossless impedance at each value of frequency is now known. Now simply plug in the lossless impedance into the lossy impedance equation with the other material and geometry parameters, and the result is the lossy impedance at each frequency value. This tells the lossy impedance in any frequency range where the input data are valid.

Obviously, there are a lot of data to keep track of. The easiest way to do this over a range of frequencies is to use an Excel spreadsheet. Because you are dealing with analytical formulas as outlined above, it is very easy to program these formulas into an Excel table **(Figure 1)** and get an impedance curve as a function of frequency.

	A	B	C	D	E	F	G	H	I	M
4	**Omega**	**E_R**	**E_I**	**t/h**	**w/h**	**w'/h**	**Re(W'/H)**	**Z0**	**C0**	**Z lossy**
5	0.00E+00	4.6425563	0	0.167197	0.73	0.8793855	0.879386	47.382814	3E+08	3.216
6	2.46E+08	4.6424970	0.0031070	0.167197	0.73	0.8793855	0.879386	47.383116	3E+08	51.955-6.014i
7	4.92E+08	4.6423194	0.0062069	0.167197	0.73	0.8793855	0.879386	47.384023	3E+08	50.85-3.928i
8	7.38E+08	4.6420243	0.0092925	0.167197	0.73	0.8793855	0.879386	47.385529	3E+08	50.308-3.173i
9	9.84E+08	4.6416132	0.0123570	0.167197	0.73	0.8793855	0.879386	47.387627	3E+08	49.953-2.763i
10	1.23E+09	4.6410880	0.0153934	0.167197	0.73	0.8793855	0.879386	47.390308	3E+08	49.698-2.495i
11	1.48E+09	4.6404513	0.0183953	0.167197	0.73	0.8793855	0.879386	47.393559	3E+08	49.503-2.302i
12	1.72E+09	4.6397060	0.0213563	0.167197	0.73	0.8793855	0.879386	47.397366	3E+08	49.349-2.155i
13	1.97E+09	4.6388556	0.0242703	0.167197	0.73	0.8793855	0.879386	47.401710	3E+08	49.224-2.039i
14	2.21E+09	4.6379039	0.0271319	0.167197	0.73	0.8793855	0.879386	47.406573	3E+08	49.122-1.945i
15	2.46E+09	4.6368551	0.0299357	0.167197	0.73	0.8793855	0.879386	47.411934	3E+08	49.036-1.867i
16	2.71E+09	4.6357139	0.0326769	0.167197	0.73	0.8793855	0.879386	47.417770	3E+08	48.963-1.801i
17	2.95E+09	4.6344851	0.0353511	0.167197	0.73	0.8793855	0.879386	47.424055	3E+08	48.9-1.744i

18	3.20E+09	4.6331738	0.0379543	0.167197	0.73	0.8793855	0.879386	47.430766	3E+08	48.846-1.696i
19	3.44E+09	4.6317853	0.0404831	0.167197	0.73	0.8793855	0.879386	47.437875	3E+08	48.799-1.654i
20	3.69E+09	4.6303250	0.0429345	0.167197	0.73	0.8793855	0.879386	47.445355	3E+08	48.758-1.617i
21	3.93E+09	4.6287983	0.0453059	0.167197	0.73	0.8793855	0.879386	47.453178	3E+08	48.722-1.584i

Figure 1. Microsoft Excel table showing lossless and lossy impedance calculation values up to 4GHz. Some columns have been hidden for clarity.

The numbers in column H show the lossless characteristic impedance, and the values in column M show the lossy characteristic impedance, both evaluated at each angular frequency value in column A. Note that the impedance values and column M are complex numbers, meaning they include a resistive and reactive impedance. As mentioned above, the transmission line impedance will be a complex number due to the various loss factors. This is one reason why copper roughness is such a powerful bandwidth limiting factor and it will become more difficult to ensure wideband impedance matching above 56GHz Nyquist in the future.

What's Next?

Remember that all the signal integrity metrics we care about in high-speed PCB design and RF design start from the impedance and propagation constant. In summary, we now have a process for calculating the lossy impedance of a transmission line, including dispersion, from the lossless impedance, and without the use of an electromagnetic field solver. A procedure for using this is as follows:

1. Select a material thickness, dielectric constant with loss tangent, and line geometry.
2. Calculate the lossless impedance using the uncorrected real part of dielectric constant from the datasheet and desired geometry (e.g., using IPC-2141, Wadell, etc.).
3. Use the corrected Dk (Eq. 2), lossless impedance from Step 1, calculated skin resistance (Eq. 3), and copper correction factor[3] to get the lossy impedance (Eq. 6).
4. Calculate the transmission lines propagation constant (Eq. 7).
5. Iterate through a range of width values until reaching a line that hits the desired signal integrity specification.

To quickly implement Step 2, use the impedance calculation models in high-end CAD tools. The right tools can provide the lossless impedance for the input width, and you can follow the rest of the process to get the lossy impedance.

With this process for calculating lossy impedance directly from geometry, an optimization algorithm that implements Step 5 may be used. A simple evolutionary or nonlinear algorithm can converge to a target signal integrity metric simply adjusting the dimensions of the line.

This problem can also be solved with the built-in evolutionary optimization tool in Microsoft Excel. A simple random search algorithm can find the width that produces a lossless impedance very close to the target across a very broad frequency range. An example algorithm in C code can be found in my EPEPS paper,[1] or in the differential evolution paper from Storn and Price.[5]

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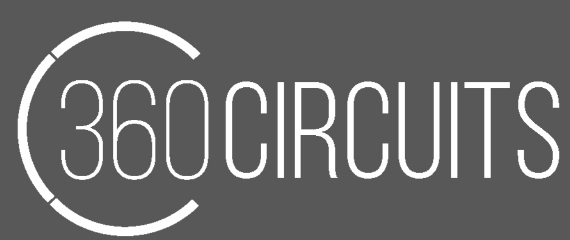
ZACHARIAH PETERSON has an extensive technical background in academia and industry. He runs Northwest Engineering Solutions (nwengineeringllc.com), a PCB design and technical marketing firm that serves industrial automation, defense and EDA software clients; zmp@nwengineeringllc.com.



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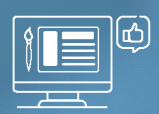

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INDUSTRY TRENDS

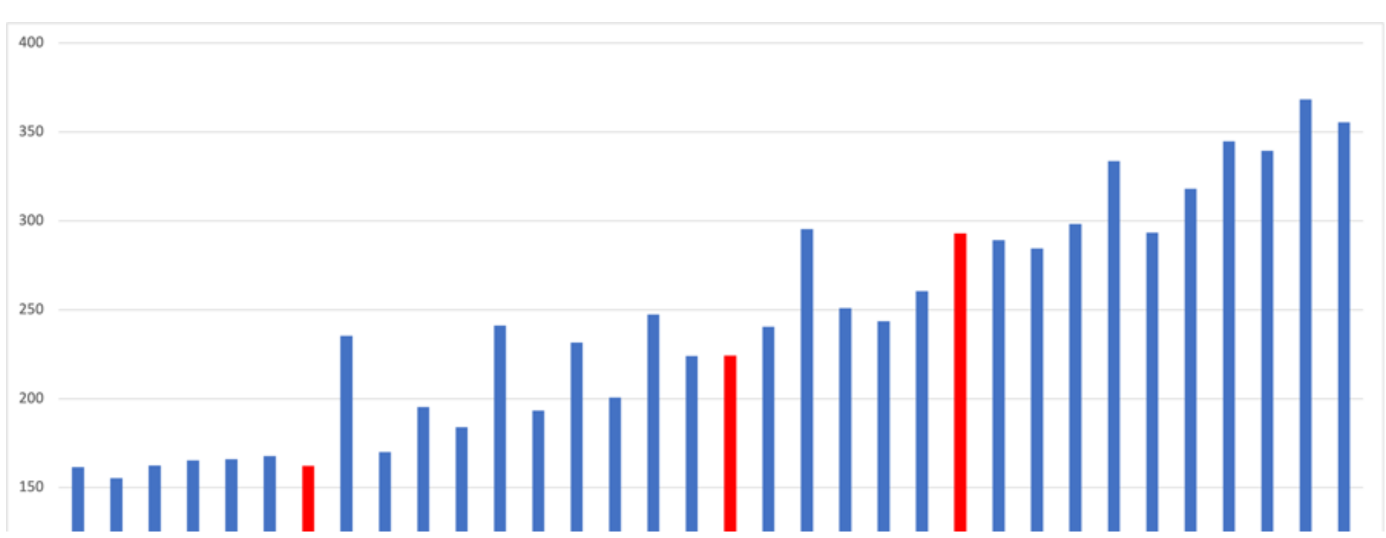
Nothing Soft about PCB Design Tools Market

Even after a long growth streak, observers still think the industry has life ahead.

by MIKE BUETOW

The Electronic Systems Design Alliance in October reported yet another staggering quarter for printed circuit board design software sales. Revenues were not only up big year-over-year, but a look at the longer-term historical trends shows just how far the sector has come even in the past few years.

Indeed, over the past seven-plus years, this supposedly mature market has experienced a year-over-year quarterly drop only thrice – in the periods ended September 2016, June 2019 and December 2020 – two of which came during the Covid pandemic. Year to date, revenues are up almost 12%. The June 2023 period, the most recent quarter for which data are available, marked the second-highest quarterly figure, behind the March 2023 period **(Figure 1)**. (The September quarter data are due to be released this month.)



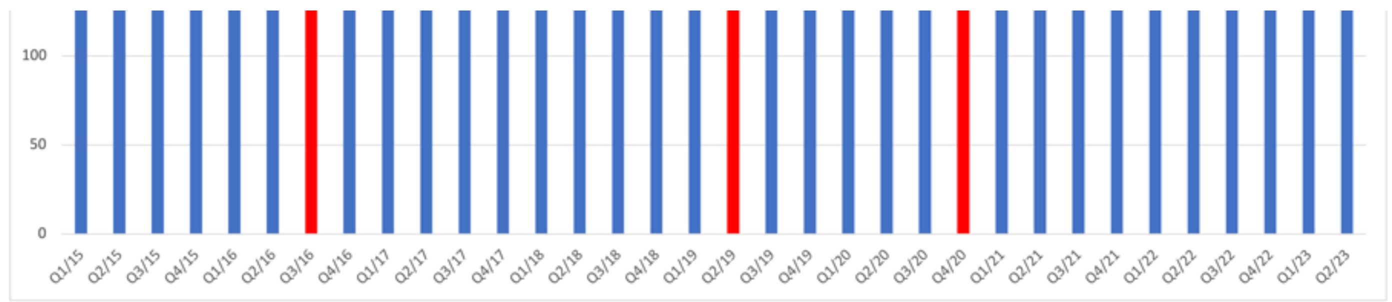


Figure 1. PCB/MCM design software revenue trends, 2015-23. (Source: ESD Alliance)

To better understand the sustained gains, and – as important – whether industry-watchers think they will continue, we polled key figures at some major EDA companies.

To understand what's lifting the market, we first must look at what defines the market. The ESD Alliance is an entity inside of SEMI, the semiconductor equipment and materials trade group. The Alliance focuses specifically on semiconductor and PCB design tool developers. The majority of the quarterly data reflects mostly that of Alliance members, but data for public companies also are included.

Among the PCB software companies included are Altium, Ansys, Cadence, Keysight, Siemens and Zuken, among others. The number of companies that report that are not part of ESDA is not substantial. In short, the ESDA data offer a better-than-solid picture of what's actually going on in the marketplace.

Then there's the results themselves. PCB tool sales over the most recent four quarters topped $1.4 billion, an industry record. If anything, revenue growth has been accelerating, rising 13% for the four quarters ended June 2023. Even longtime industry-watchers have taken notice.

According to the dean of PCB design tools market analysis, Merlyn Brunken of Siemens, the growth streak is "remarkable," adding that of the three down quarters over the past eight-plus years, two came during the pandemic and none of them showed a year-over-year drop of more than 1%.

Brunken believes several simultaneous factors are contributing to the rise. He points to a general expansion of design around the world over the past two decades, in particular, in Asia.

Going back to 2005, when the ESD Alliance first broke out the PCB market segment revenue regionally, North America (37%), Europe (25%) and Japan (23%) dominated. But while North America's portion has grown over time to 43%, the other traditional major players have seen their shares erode. Europe dropped to 22% in 2022, and Japan plummeted to 12% (more on that in a moment).

Meanwhile, Asia/Pacific, which accounted for some 16% of the PCB design tool regional market share in 2005, now makes up almost a quarter (23%) of worldwide revenue.

So more regional players have made their presence felt, expanding the playing field. But even as the field becomes wider, it's also getting bigger. And there is widespread agreement that this boils down to the proliferation of electronics, both in new end-products (think IoT and consumer handhelds like watches) and in traditional ones where the content is growing (automotive and medical, for two).

As Bob Potock, vice president of marketing at Zuken USA says, "The simple answer is that more and more new products now contain some sort of electronics and that requires a PCB."

Manny Marcano, chief executive of EMA Design Automation, perhaps the world's largest value-added reseller of PCB EDA tools, agrees, adding the expanding amount of electronics content in products and the drive for "smaller, faster, cheaper, lower power products … are enabling the market to grow as companies are turning to software and automation to meet these market requirements."

"You only have to check the statistics on the number of 5G devices approved to connect to wireless networks globally to realize that many require complex, high-speed circuit boards," says Brunken. "6G work is already underway. On top of that, you can look at all of the global design activity in the computer space, with many more companies now producing unique, high-speed MPUs, GPUs, and AI processors and the circuit boards that include those devices. These new devices are no longer restricted to the traditional computer market as industries adopt similar devices for automotive, communication, aerospace, defense, and other applications. These new devices are increasingly designed by systems companies that create custom PCBs instead of using an off-the-shelf circuit board."

“Macro trends like always-on connectivity and new business models for customers who are not only looking to sell products but monetizing and leveraging the data collected (meaning they need intelligence and sensors to collect the data) are also playing a big role in this growth,” Marcano adds.

For some, the current upcycle recalls the boom era of the personal computer, perhaps the fastest-growing time in industry history. According to Marcano, “I think this era is similar to when EDA first really started in terms of the amount of design activity and change in the market.” He and Brunken agree that the time-to-market pressures coupled with more complex designs necessitate levels of automation that will continue to drive new sales.

“Design engineers are typically a risk-averse group, especially with tools they learn and use daily. They add tools and change methodologies when they have to make a change to get the job done correctly. The reality is that complexity drives PCB engineers to adopt new or more capable tools to achieve the project goals,” said Brunken. “What is unique right now is that the industry has to deal with so many complex technology issues converging simultaneously. Complexity changes are happening across several dimensions. The only time I can recall something like this that lasted an extended period was when automation emerged and forced teams to move from manual methods to tool adoption. And they did it because they couldn’t be successful with the old techniques that they were used to.”

Added Marcano, “I also think we are in somewhat uncharted waters. At PCB West your keynote speaker stated that in North America alone there are 70,000 PCB design openings and only 10,000 filled jobs. If we combine that with your recent PCB salary survey showing 46% of active designers surveyed are over 50, what we have is a massive labor gap coming like we may have never seen before. Minting new engineers will take time and the way companies will need to solve this is to lean on automation and tools more than ever before, so although the current growth has been amazing, we are even more bullish about what lies ahead. Tremendous opportunities for those who can innovate and help meet these needs.”

Chicken and Egg

But do new tools drive growth, or is it more a function of new program starts and growth at

customers? Marcano thinks the answer is both. “We are seeing an increase in new projects and companies – and segments, electric vertical take-off and landing (eVTOL) aircraft **(Figure 2)**, for example – but we are also seeing existing customers needing more capability to meet their requirements, partially based on the staffing challenges defined above but also to help them meet the complexity, and supply-chain requirements that they have as well.”

Figure 2. EVTOLs represent another potential souped-up end-market.

Potock points to new component technology, such as MEMS, FPGA, IoT and touchscreens, that is enabling product line extensions and new markets. “An example of product line extension would be a smart refrigerator with touchscreen. An example of a new marker would be wearables in the fitness industry,” he said.

“The emergence of new technologies and requirements is the primary driver of growth in EDA,” Brunken agrees. “I think new program starts and customer growth are part of the equation, especially with the ‘electrification of everything.’ At some point, technology will drive beyond old methodologies, and tools capable of making the design team successful will be incorporated. A great example of this can be found in the integration of more simulation and analysis tools into the PCB design flow.”

Employment for All?

On the PCB Chat podcast each quarter, ESD Alliance spokesperson Wally Rhines has often noted that if the growth rate in EDA is sustained, the industry will sooner or later employ most of the world. Indeed, employment in the EDA sector was up nearly 12% year-over-year in the June quarter. It begs the question, how sustainable is this?

"It's remarkable to me that we are growing the employment that rapidly, although we almost always grow employment faster than the revenue," said Rhines, who is also former chief executive of Mentor Graphics. "We may be hiring more people in lower-cost jurisdictions and as a result the headcount goes up but the cost of hiring all those people doesn't go up quite as much. It's a very healthy and growing industry."

Brunken cautions that the employment data may not tell the whole story. The data are based only on corporate headcounts, and there's no ratio of employees to expenses. "It would be unwise to grow expenses faster than you are producing revenue," he notes. "That becomes self-limiting pretty quickly.

"Depending on the timeframe you look at, the CAGR will vary. In the EDA market, between 2016 and 2022, EDA revenue grew by 10%. However, we have seen from our earlier analysis that much of the revenue growth comes from the Asia/Pacific region where expenses are not the same as those in Europe, North America and Japan. And, even for companies headquartered in Europe and North America, there has been an effort over the years to go to where the talent is or to help address the labor shortages at home. Frequently, the full-time employee count can be less expensive. Therefore, I would argue that headcount growth is a non-issue when considering revenue growth and headcount expense."

Tools will drive revenue, Marcano says, and the jobs will follow the need for new tools. "While how AI will impact the market remains to be seen, it opens whole new areas of need for companies to develop and leverage these learning models and large data sets AI needs to be successful. To achieve that goal, the core content of CAD libraries, simulation models and references designs are required for AI and MBSE (model-based systems engineering). I think the recent history has shown that as long as we can continue to derive significant value for

customers, they are willing to invest and we will need to staff accordingly to meet those needs."

AI is, of course, all the rage, but rarely is a single technology a panacea. Where else might tomorrow's growth come from? According to Brunken, we might just need to think small: "We are just entering the packaging market's growth stage. Packaging has always been part of the PCB category and gets reported separately across several categories, including physical layout, analysis, and packaging tools. The analysis and packaging tools have CAGRs of ~12%, with the physical layout tools just over 9% during the 2016–22 timeframe." As major legislative packages such as the Chips and Science Act in the US and the European Chips Act take hold, new investments – both public and private – could spur yet another round of expansion for PCB tools.

The other question is whether another region will emerge as something more than a bit player. The decline of Japan, which has suffered in part because its traditional product mix hasn't grown as fast as the electronics produced in North America and Asia/Pacific, proves that dominance isn't forever. That should serve as both a motivator and a warning to the rest of the world not to get complacent.

MIKE BUETOW is president of the PCEA (pcea.net); mike@pcea.net. Each quarter he discusses the latest EDA data with ESD Alliance spokesperson Wally Rhines on the PCB Chat podcast.

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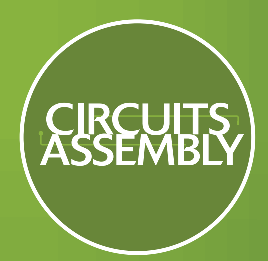

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DEPANELING

Establishing Design Rules for Laser Depaneling of Printed Circuit Boards

Analysis and summary of the most fundamental design guidelines.

by PATRICK STOCKBRÜGGER and STEPHAN SCHMIDT

Technological advantages associated with the use of laser systems include flexibility, material efficiency and performance. To exploit the potential of filigree laser tools it is necessary to know and understand the physical and technological possibilities and limitations. This article focuses on material efficiency and design rules. Various factors are decisive for the design of PCBs, such as components and their heights, and potential mechanical or thermal stress.

Methodology and Results

The following results are based on experience and know-how collected during dozens of application trials for cutting rigid FR-4 boards in the application department at LPKF Laser & Electronics SE. For simplification, results are presented mostly on the basis of a green nanosecond laser with 40W nominal power. This laser type is regularly chosen for depaneling FR-4 applications due to its relatively high power, robustness and good price-performance ratio.

Component distances. For PCB design, the requirements of the intended device in terms of available space and functionality are of central importance. Those functionalities are ensured by various components mounted and connected on the PCB substrate. Especially at the edge of the PCB, free areas may have to be accounted for to prevent damage to the component by the separation tool. Since the laser is a relatively narrow tool at around 20µm

diameter of the focused beam, the concrete significance of this size advantage is derived on the basis of physical framework conditions in the following.

In the case of a laser, the beam tapering in the direction of the substrate and its distance-dependent diameter must be considered. A general distance of 100µm should be maintained to compensate for the accuracy of the laser depaneling as well as the pick-and-place machine. The course of the laser depends on the structure of the beam path and the integrated optics. It can vary slightly for different laser systems, especially the wavelength (a green or ultraviolet laser, for example, influences the characteristics of the laser beam and its shape). The curve of the calculated distance as function of the component height is shown in **Figure 1** as a graph, with further details of the beam path omitted due to confidentiality. Basically, a linear relationship can be observed between component height and required distance to the cutting channel.

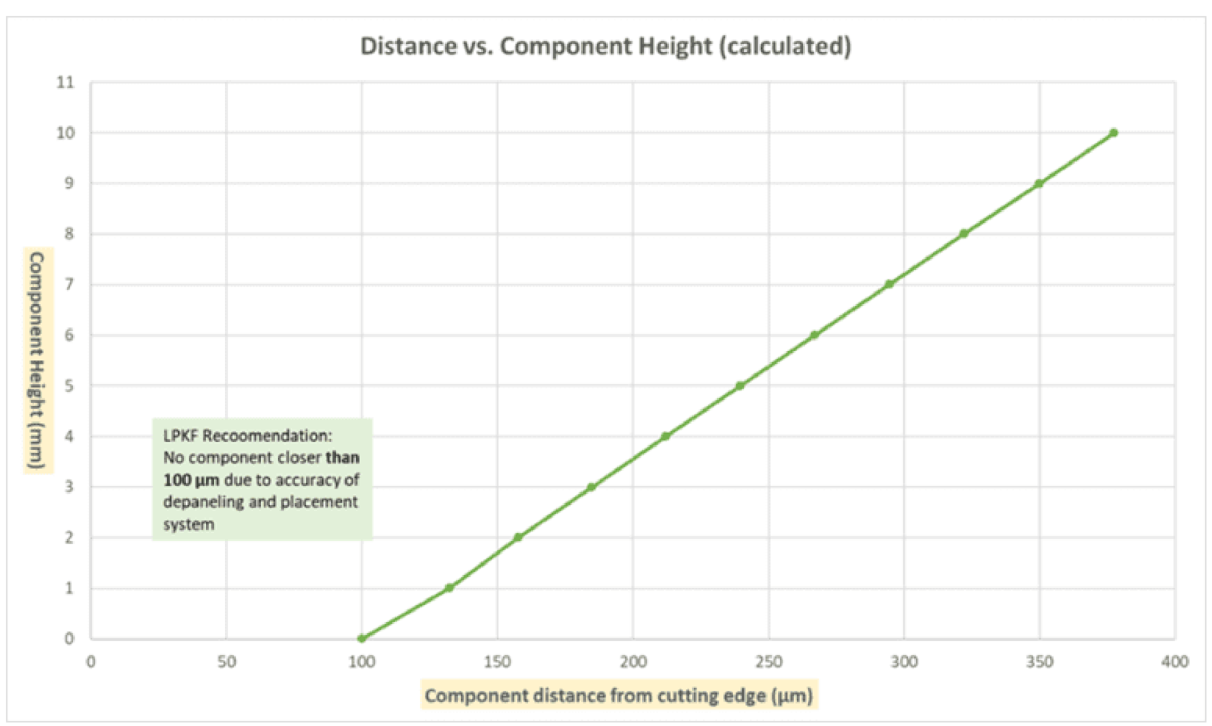

Figure 1. Minimum calculated distance of a component depending on its height for green nanosecond laser.

Considering some degree of certainty, a ratio of 1:10 for the distance-to-cutting channel in relation to the height of the component can be considered a rule of thumb.

Mechanical and thermal stress. One of the main concerns for traditional depaneling processes such as manual separation, milling and sawing is the induced mechanical stress and its potential danger for sensitive components. Consequently, the absence of mechanical stress is widely acknowledged as one of the key advantages of the noncontact laser process. A strain gauge on the PCB substrate was used for measurements in order to further evaluate mechanical vibrations during the laser process and its potential influence. **Figure 2** shows the observed acceleration with a novel cutting strategy for low to high frequencies in the x-, y- and z-axis. A critical threshold of 100g was defined as a reference value, which is representative for commonly used sensors. It is evident that during the laser process observed accelerations are significantly below a critical threshold for all the considered frequencies. Hence, there is no risk of damage due to mechanical stress.

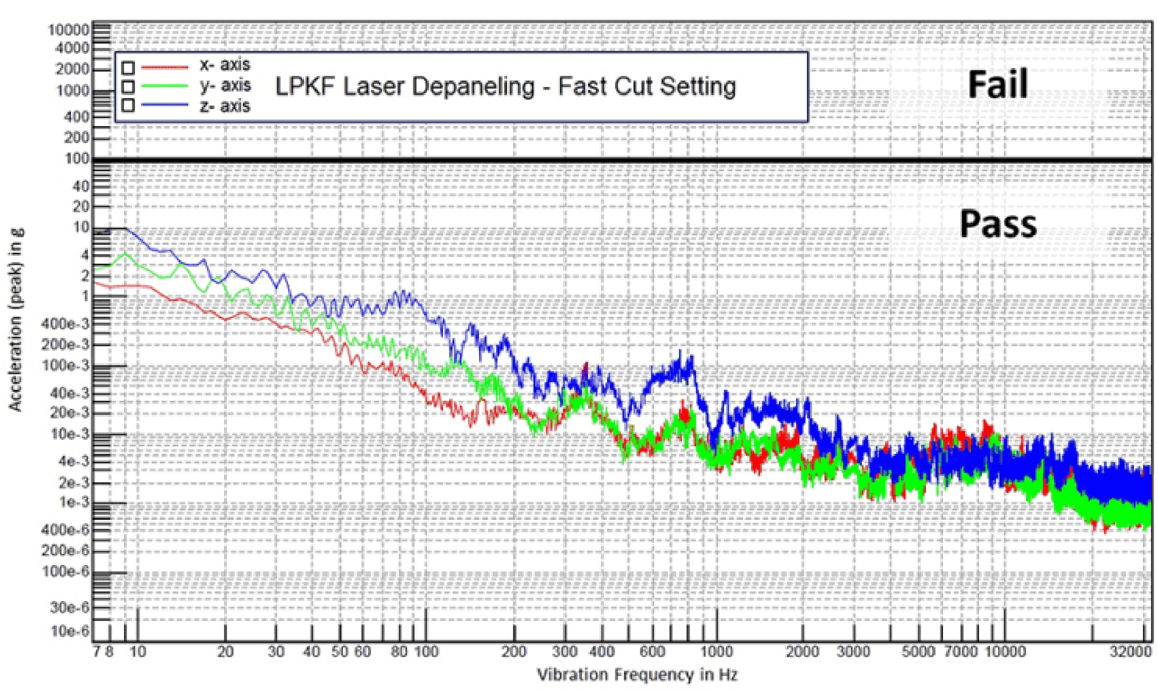

Figure 2. Measured accelerations over frequency in x-, y- and z-axis for sample layout with FastCut.

Another concern of PCB designers with laser depaneling is the potential temperatures that can occur in areas close to the cutting channel. Prior analyses have proven that these reservations are not necessary. In **Figure 3** the average maximum temperatures are shown for different cutting strategies in distances varying from 100 to 500µm. The measurements have been carried out by inserting K-type thermocouple elements into the PCB substrate. For all observed distances and even in case of the closest observed distance of 100µm, the

temperatures are significantly lower than the liquidus temperature of the tin/silver/copper (SAC) alloy. Consequently, the alloy cannot start to melt under any external circumstances. Furthermore, it can be observed that temperatures are decreasing significantly with growing distances, which means that even very heat-sensitive components can be placed very close to the laser cutting channel.

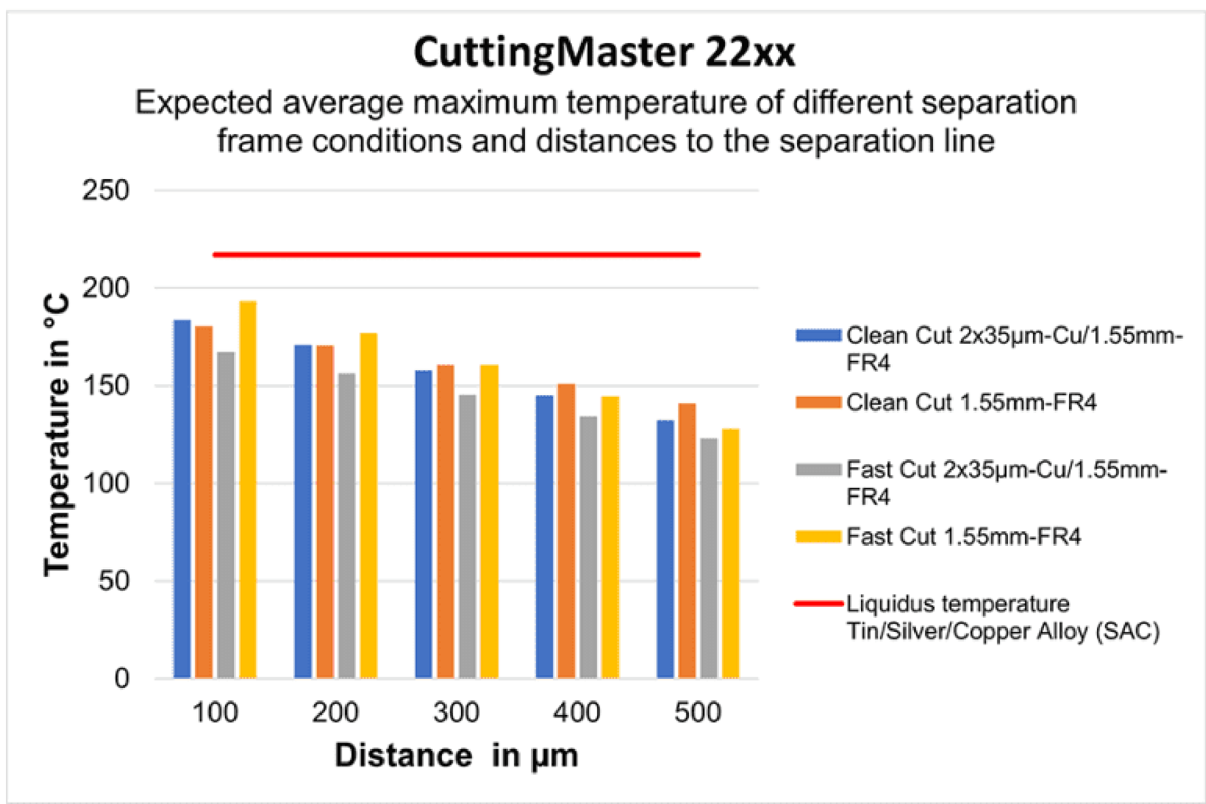

Figure 3. Average maximum temperatures for different cutting strategies, material compositions and distances to the cutting channel.

Channel widths. The laser is a flexible tool and can achieve different cutting qualities depending on the customer requirements. To enable PCB designers to lay out the panel in an appropriate way for lasers, we compared channel widths for a fast, standard and clean cutting edge. The designation is based on the quality of the cutting edge and the speed the cut is executed and is defined as follows:

- **FastCut:** Focus on performance and less on quality. Cutting edge is discolored and might show a slight but harmless and safe carbonization.
- **StandardCut:** Compromise between Fast- and CleanCut, with slight discoloration and minimal to no carbonization.

- **CleanCut:** Cutting edge with maximal technical cleanliness with no discoloration or carbonization but less focus on performance.

Figure 4 compares the three cutting strategies, and the qualitative differences are evident by the degree of discoloration and/or carbonization.

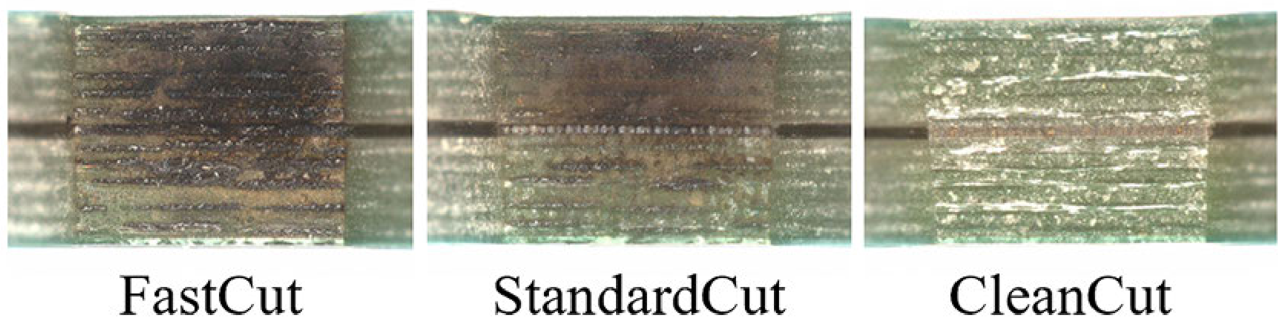

Figure 4. Comparison of cutting strategies Fast-, Standard and CleanCut with corresponding edge quality.

Figure 5 shows the width of the required cutting channel on the entry side for the laser tool depending on the material thickness of the FR-4 substrate. In general, it can be observed that the required channel width increases with thicker material thicknesses.

- **FastCut:** Relatively small cutting channel on the laser entry side with slight and not linear growth for increasing material thicknesses.
- **StandardCut and CleanCut:** Both cutting strategies require a wider cutting channel on the laser entry side which increases linear with the material thickness. CleanCut needs a slightly larger laser entry for the same material thickness.

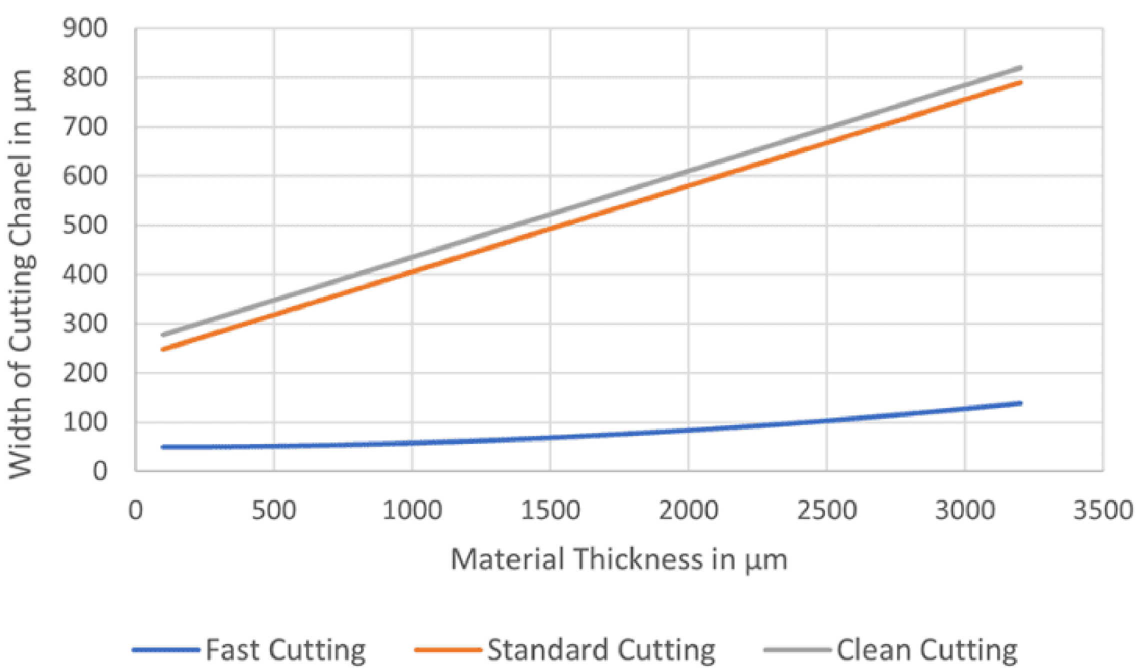

Figure 5. Width of laser cutting channel on entry side for a green nanosecond laser with Fast-, Standard and CleanCut.

As the laser beam is not equally shaped over the whole distance but tapered from top to bottom side (focus point), the laser entry and exit side have different channel widths. **Figure 6** illustrates the exit comparison for the three observed cutting strategies in relation to the material thickness. Based on the results the following behavior can be seen:

- **FastCut:** (Relatively) very small and constant channel width on laser exit side of 35µm.
- **StandardCut:** Relatively high and constant channel width of around 120µm.
- **CleanCut:** Highest observed and constant channel width of 140µm.

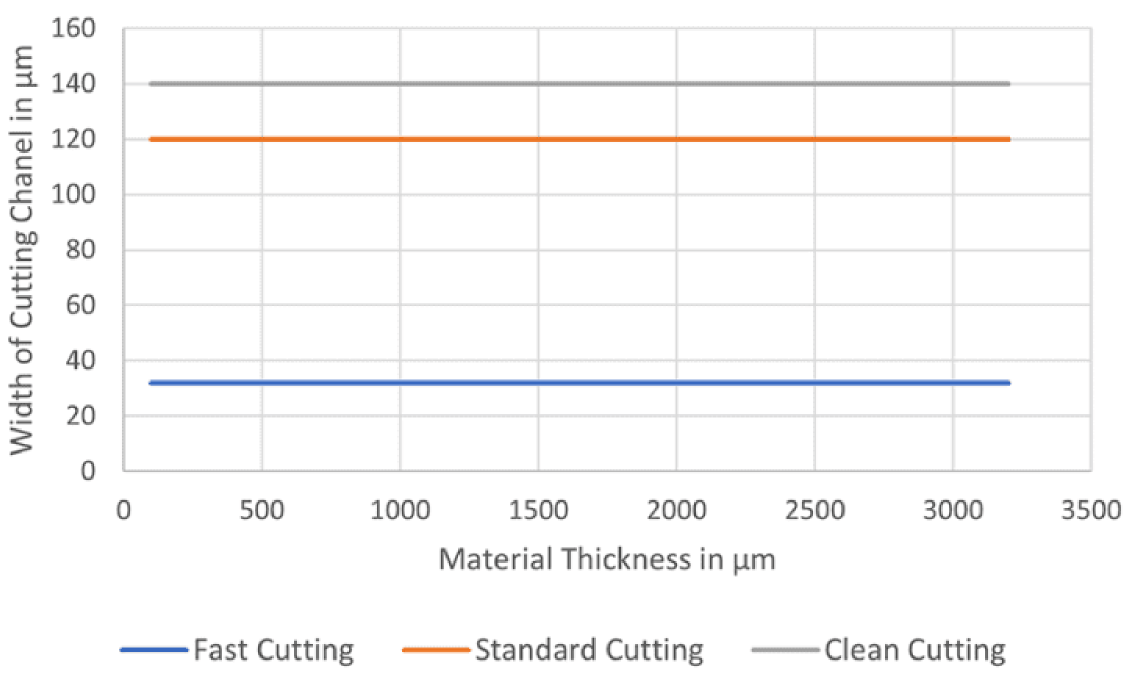

Figure 6. Width of laser cutting channel on exit side for a green nanosecond laser with Fast-, Standard and CleanCut.

The consequence of the width of the channel on the laser entry and exit side is a small angle of the PCB edge – the so-called taper. It is the difference of the widths of the cutting channel on the entry and exit side. **Figure 7** shows the size of the taper relative to the substrate thickness for the cutting strategies FastCut, StandardCut and CleanCut. The following results can be observed for the different cutting strategies:

- **FastCut:** Relatively small taper for all material thicknesses due to a very small increase for thicker substrates.
- **StandardCut and CleanCut:** For both cutting strategies a comparable and relatively large taper especially for increasing material thicknesses can be observed.

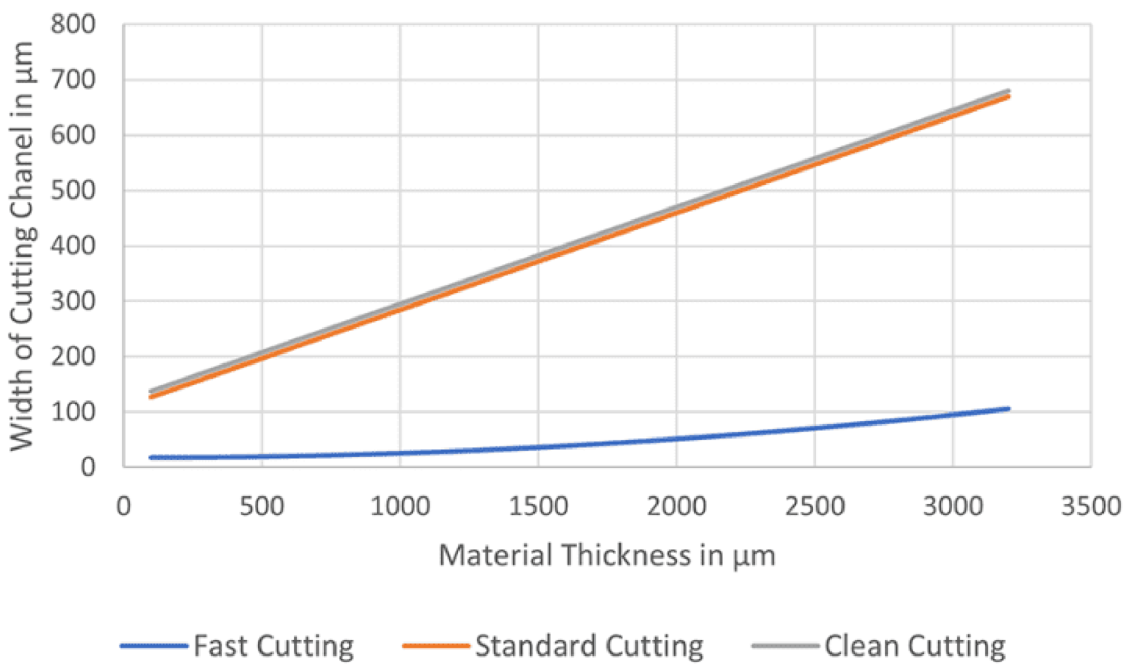

Figure 7. Taper size depending on laser-cutting strategies for an interval of material thicknesses.

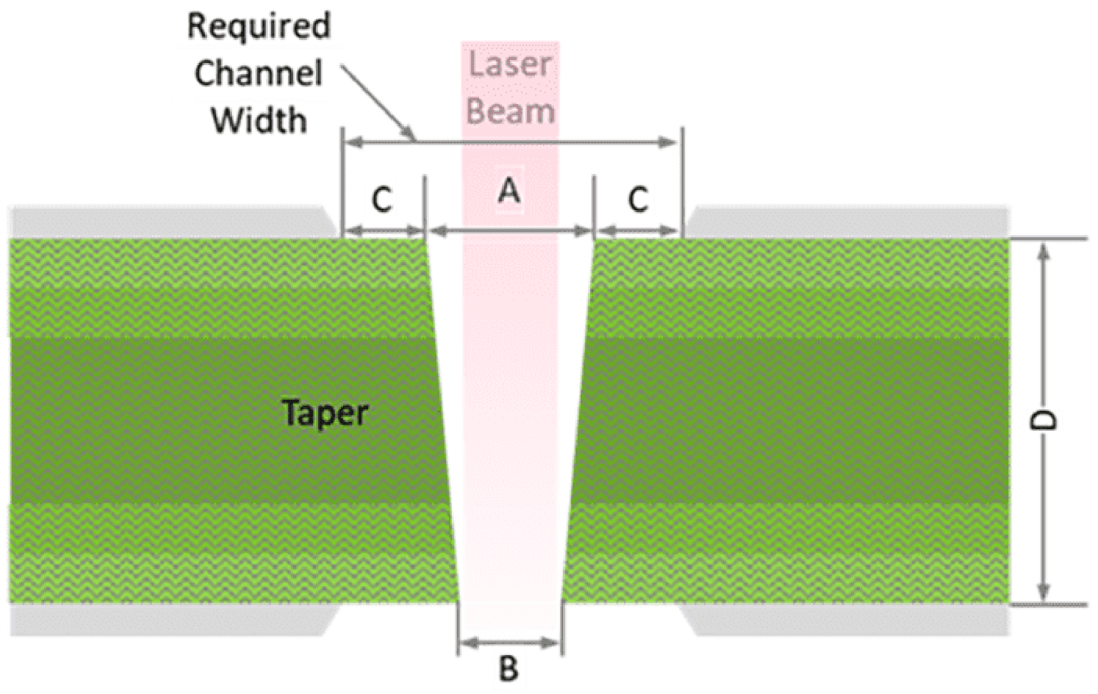

Figure 8. Schematic structure of the required cutting channel, determined by the width on the laser entrance side (A) and the twofold accuracy value (C) for a shift to the left or right.

To determine the required distance between circuit boards, not only the required laser channel but also the accuracy of the laser system need to be considered. As consequence, the required channel width is defined as follows:

Required channel width = A (width of laser entry) + 2 x C (accuracy of laser system)

It can be summarized that the desired quality or performance is decisive for the width of the cutting channel and the taper. Therefore, especially in the case of a full cut with the laser, this determines the maximum possible utilization of the panel material. In this case FastCut tends to achieve higher utilization rates.

Size and Position of Scan Fields

During laser depaneling, material is removed layer by layer by vaporizing it. With each repetition, a pulse of energy of the focused laser beam is induced into the material. Consequently, the temperature of the substrate would in principle increase with each additional repetition. To avoid this effect, usually short cooling times, called delays, are considered between two iterations.

The scan field is usually a square area in which the laser beam can be deflected without any need to move the substrate underneath (e.g., 80mm x 80mm). To achieve the best compromise of cutting quality and performance, two factors are of central importance: the size and position of scan fields on the panel. Consequently, the best results can be achieved when a PCB designer considers the effects of the size and position of the scan fields during panel layout. To better understand this, both effects are then considered on the basis of a schematic example. **Figure 9** shows a potential panel design before (left) and after (right) design optimization. By adjusting the position of the tabs from the bottom and top to the sides, the number of scan fields could be reduced by two (33%). As a result, more cutting information is part of one scan field and potential delays can be reduced or even avoided.

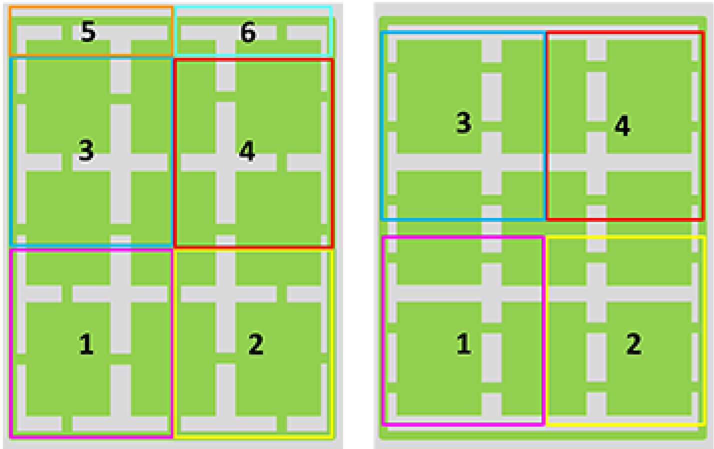

Figure 9. Schematic illustration of design optimization for laser depaneling.

Table 1 shows the influence of the illustrated scan field reduction by optimized arrangement of tabs on a mathematical example using a calculation tool for an exemplary LPKF laser tool (green nanosecond laser). As shown in Figure 9, the tabs have simply been rearranged, with otherwise unchanged framework conditions. For each PCB four tabs with a single length of 5mm have been considered. Resulting in a total cutting length of 180mm. For those framework conditions, layout A, with six scan fields, results in a cycle time of 153 sec., while layout B, with four scan fields, requires a cycle time of only 103 sec. In total the cycle time could thereby be reduced 50 sec. – roughly a third (32.7%) of the original value. The example illustrates that even slight design optimizations might have a significant influence on the cycle time for a laser tool.

Table 1. Comparison of Sample Layout before (A) and after (B) Optimization of Tab Positioning

Properties	Layout A	Layout B
No. PCBs per panel	9	
Material dimension (X x Y)	140mm x 180mm	
No. fiducials	3	
Cutting length in mm	180	
No. tabs	36	
Material thickness	1600µm	
Scan fields	6	4
Cycle time	153 sec	103 sec
Comparison	-	-32.7%

Subsequently, **Table 2** shows the potential influence of the scan field size on the cutting performance and the correlation with the panel design. For the following example the cycle time was determined for the optimized layout from Figure 9 with a 50mm and 80mm scan field size. The first result is the number of scan fields required to map the panel size. For the 50mm scan field size, 12 are required, while for the 80mm size only four are needed. For the same layout, the smaller scan field size logically results in fewer cutting lengths per scan field. The effect is relatively significant for the example, so that 200 sec. – 66% of the cycle time – is saved in comparison.

Table 2. Comparison of Sample Layout with 50mm and 80mm Scan Field Size

Properties	50mm	80mm
No. PCBs per panel	9	
Material dimension (X x Y)	140mm x 180mm	
No. fiducials	3	
Cutting length in mm	180	
No. tabs	36	
Material thickness	1600µm	
Scan fields	12	4
Cycle time	303 sec	103 sec
Comparison	-	-66%

Both examples visualize that the effect of design adjustments and scan field size can have a major impact on the cycle time of laser depaneling. This is especially true when there is relatively little cutting length, for instance due to small and few tabs.

Panel Preparation

To increase the cycle time per panel and printed circuit board, e.g., to achieve a certain clock cycle of a production line, there are multiple ways to prepare a panel by reducing the material to be cut at the end of the SMT line. Popular approaches to do so are among others pre-milling, V- and U-score. Due to the characteristics of the laser process, those preparation methods differ in terms of their efficiency. Before going into detail for each of the preparation approaches, the processes are shortly described and differentiated:

- **Pre-milling:** Typically performed by the PCB manufacturer, the contour of the PCB is widely mill away. The remaining material to the frame structure is also called tab(s).
- **V-score:** With this preparation approach the material thickness is locally reduced (in general by a third) from the top and/or bottom. This results in a V-shaped profile of the channel.

- **U-score:** Similar approach and generation as a V-score, but with a U-shaped or top hat channel profile.

Pre-routed tabs are a widespread approach to reduce cycle times of milling or laser tools to depanelize. **Figure 10** shows a schematic illustration of a pre-routed tab with a channel width of 2.5mm. Depending on the material thickness and required panel stability for other SMT processes, the tab width can vary in the low single-digit millimeter range. In the event of mechanical separation, it also minimizes mechanical stress during depaneling. For a laser, it offers only the potential to optimize cycle times especially in combination with additional drillings. Due to the working principle of the laser, however, this does not necessarily lead to a reduction in cycle time, as it depends on other factors, which we will examine in more detail in the following.

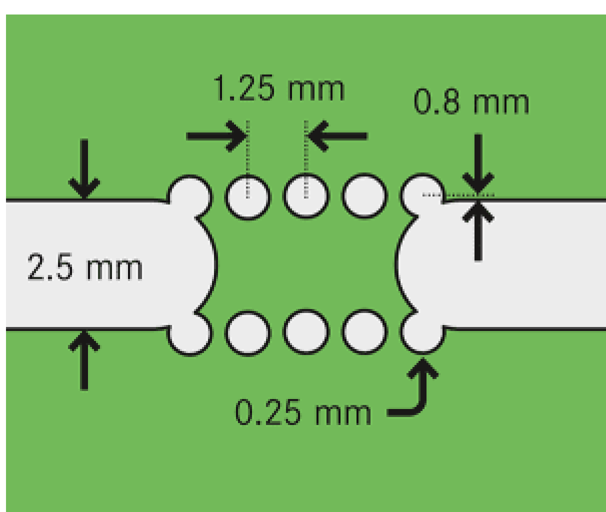

Figure 10. Schematic illustration of a pre-routed tab with additional millings for cycle time optimization.

As explained in the section on design optimizations regarding the size and position of scan fields, the target for laser depaneling is to get as many cutting lengths (cutting information) as possible in one scan field. The reason for this is to reduce or avoid cooling times to prevent excessive carbonization of the substrate material. Consequently, by reducing the cutting length in the scan field, the additional drillings may also result in more delays being required again. This is especially valid if there is relatively less cutting information, e.g., few and small tabs per scan field. In principle, the effect is therefore smaller or counterproductive

depending on how much cutting length is present in the scan field. Due to varying pulse durations, laser powers and frequencies, this can vary depending on the laser depaneling system.

Another relatively widespread method is the so-called V-scoring, where the panel is scribed locally from one or both sides. This is particularly useful for rectangular circuit board contours, as only straight scribes can be made using this method. **Figure 11** displays a schematic drawing of a groove with a reduction of the material thickness by one third each from the bottom and top.

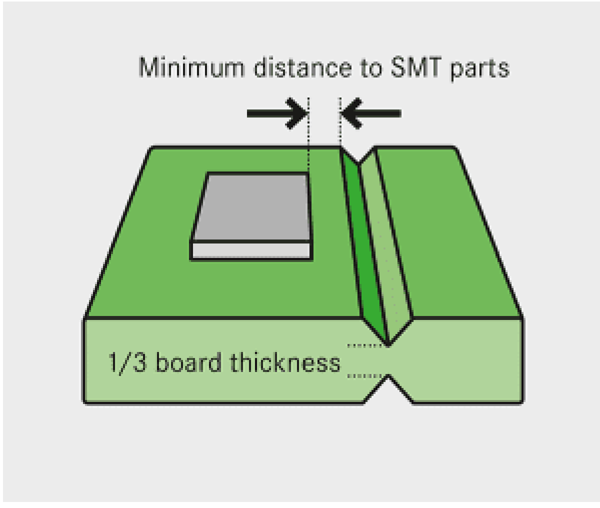

Figure 11. Schematic illustration of a V-score with reduction of the board thick to one-third.

In principle, a reduction in material thickness is beneficial to the laser, as the speed increases disproportionately for a decreasing thickness. Because fewer repetitions during ablation avoid cooling times, that could become necessary due to overheating of the material.

As **Figure 12** shows, the actual effect depends on other factors: The position of the cutting channel in the scoring groove and, if applicable (in the case of preparation on both sides), the position of the grooves in relation to each other. Finally, both factors depend on the accuracy of the scoring tool. The effect of increasing inaccuracy of the scoring tool can be illustrated quite simply, since the accuracy of a laser system is relatively high, it will match the groove specified in the data with a deviation of around 20µm. However, if the groove shifts by

100µm, 200µm or even more compared with the data, the laser will not hit the groove at the lowest point but further up one of the V-shaped flanks. Figure 12 illustrates that schematic effect for a shift of roughly 100µm. While the upper groove is not cut at the lowest point but in the middle of the right flank, the lower groove would be consistent with the laser cutting channel. Accordingly, to ensure the circuit board is completely cut out, further ablation repetitions must be considered to cut through and therefore a process-reliable production.

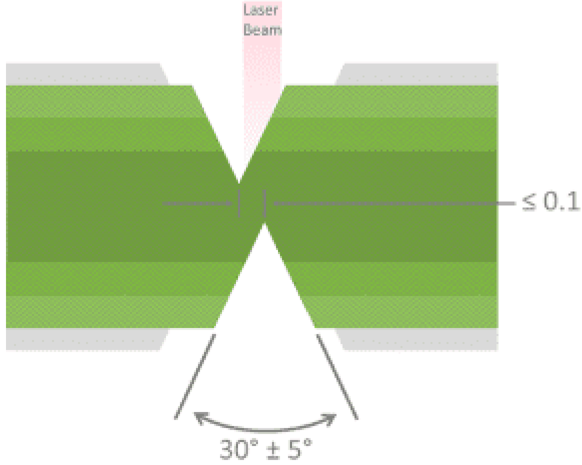

Figure 12. Offset of V-shaped grooves to each other as well as to the laser cutting channel.

With the U-groove, the approach is largely comparable to that of the V-groove, with one decisive difference in the shape of the removal profile. **Figure 13** shows the schematic structure of an ablation on both sides, where the material thickness is also reduced to one-third. The characteristic U-shaped profile is clearly visible.

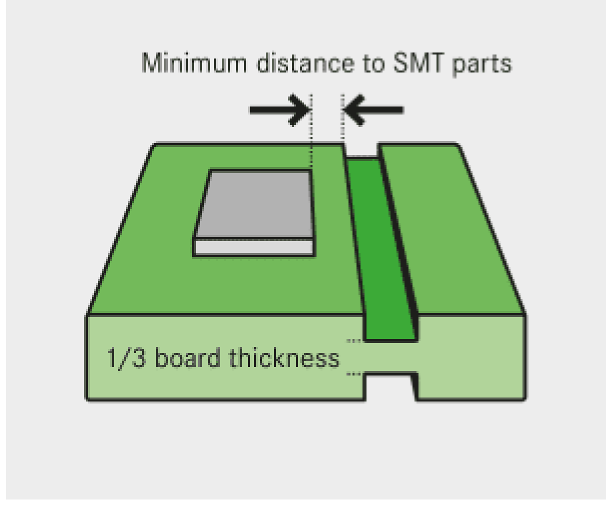

Figure 13. Schematic illustration of a U-score with reduction of the board thick to one-third.

In contrast to the V-groove, **Figure 14** shows the effect of a similar offset for the U-groove. Despite an offset to the center of the scoring, the depth is constant and thus no additional repetitions need be considered. Even an offset of the upper and lower groove has no negative effect on the desired performance increase within the usual accuracy intervals of the groove tools, as the wide low points remain to overlap.

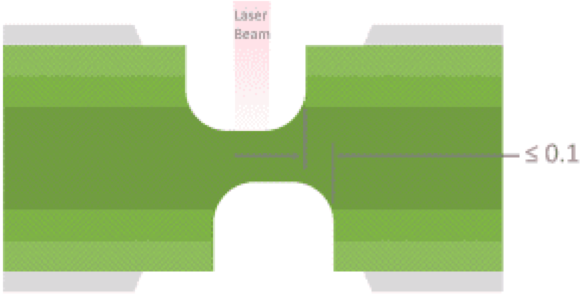

Figure 14. Offset of U-grooves to each other as well as to the laser cutting channel.

To summarize, the U-groove and pre-milled channels in particular offer a reliable increase in performance for laser depaneling. If there is a relatively large amount of cutting information in the scan field, the tabs can also be further reduced by additional drillings.

Summary

Overall, it is evident that PCB and panel design are of central importance for laser depaneling. On the one hand, potentials are revealed through placement of components on the circuit board close to the cutting channel and material savings through the relatively narrow cutting channels when the contour is fully cut. On the other hand, it shows that factors such as the cutting strategy, arrangement of tabs, the size and positioning of the scan fields and also the selection of possible panel preparation should be taken into account during

the design in order to get the best possible performance and quality out of the technology.

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PATRICK STOCKBRÜGGER is product manager SMT/PCB Production Equipment, at LPKF Laser & Electronics (lpkf.com); patrick.stockbruegger@lpkf.com. **STEPHAN SCHMIDT** is former president of LPKF Laser & Electronics North America; stschmidt@outlook.com.

ULTRASONIC WIREBONDING

Vibration Resistance and Durability of Wirebond for EV Batteries

Mitigation techniques to eliminate wire breakage failures.

by DODGIE CALPITO, SHUICHI MITOMA, SHIZU MATSUNAGA, KOSUKE ONO and TSUKASA ICHIKAWA

Wirebond technology has long been used in semiconductor manufacturing because of its inherent flexibility, considered a major advantage as an interconnect method. With wirebonding, electrical interconnections or wirebonds are created between the silicon die and its leadframe or substrate using fine bonding wires made of gold, aluminum, copper, silver alloys or palladium-coated copper composites. These wirebonds are delicate though flexible, and in semiconductors, are usually encapsulated by buffer materials such as resin or mold compounds, giving them a measure of durability and the ability to resist damage from vibration. That measure of durability is lost in open-air applications, however, including EV battery packs where there is no molding or encapsulation material to protect the wirebond from the effects of vibration.

Here, the authors look at ultrasonic wirebonding as currently used for interconnecting cylindrical lithium-ion (Li-ion) cells in EV battery packs, where such wirebonds are vulnerable to breakage due to vibration in part because they are not encapsulated. Also reviewed are vibration tests of wirebonds using a) test equipment developed for this study, and b) five types of comparison studies (vibration direction, material, wire shape, loop height, single bond or wirebond).

Ultrasonic wirebonding is currently used for the interconnection of cylindrical Li-ion cells in EV battery packs. The negative wire is bonded to the cell rim while the positive wire is bonded to the cell center cathode, which is supported by thin legs that are prone to vibration. The cell can is made of nickel-plated steel with the crimped rim having rounded cross-sections. Wirebonds are designed for flat surfaces, and bonding on the rounded cell rim makes it even more challenging. The cell rim surface roughness is also inconsistent due to the crimping process and is prone to corrosion and electrolyte contamination.

Rough road conditions, rough handling or sudden acceleration/deceleration of the EV could cause wire fatigue and eventual breakage due to vibrations generated under such conditions. The result can be breakage at the neck region between the bond and the span of the wirebond, a common cause of energy capacity loss in EV battery packs.

The goal of this study was to analyze the wire breakage problem and to offer mitigation solutions to reduce or eliminate the failure.

Setup

Vibration tests were performed using in-house designed test equipment composed of a vibration generator, tables and automatic timer installed in a clean room, with temperature set around 20°C and humidity around 50% RH.

For the vibration, given a constant acceleration of 1.0G, the test vibration frequency was varied from 10-70Hz, providing inversely proportional amplitudes as listed in **Table 1.** One table is vibrated while the other is stationary. The automatic timer is wired such that it stops on the occurrence of wire breakage.

$$A = (2\pi f)^2 \times D/1000 \ (m/s^2)$$

where

A = Acceleration (m/s^2)

D = Amplitude (mm)

F = Frequency (Hz)

Table 1. Vibration Frequency vs. Amplitude

Frequency (Hz)	Acceleration (m/s^2)	Amplitude (mm)
10	1.0G	2.484
12		1.725
21		0.563
25		0.397
50		0.099
70		0.051

Using a high-speed camera, crack propagation and wire breaks were recorded during the tests. As expected, cracks are initiated in proportion and direction to the vibration. For example, in the vertical vibration test where the top motion is longer than the bottom motion with respect to the original plane of the vibrated bond, a crack initiates from the top portion of wire first. This is followed by a bottom crack directly opposite it. Both cracks progress toward each other across the cross-section of the wire until rupture. **Figure 1** shows a SEM image of a typical wire break.

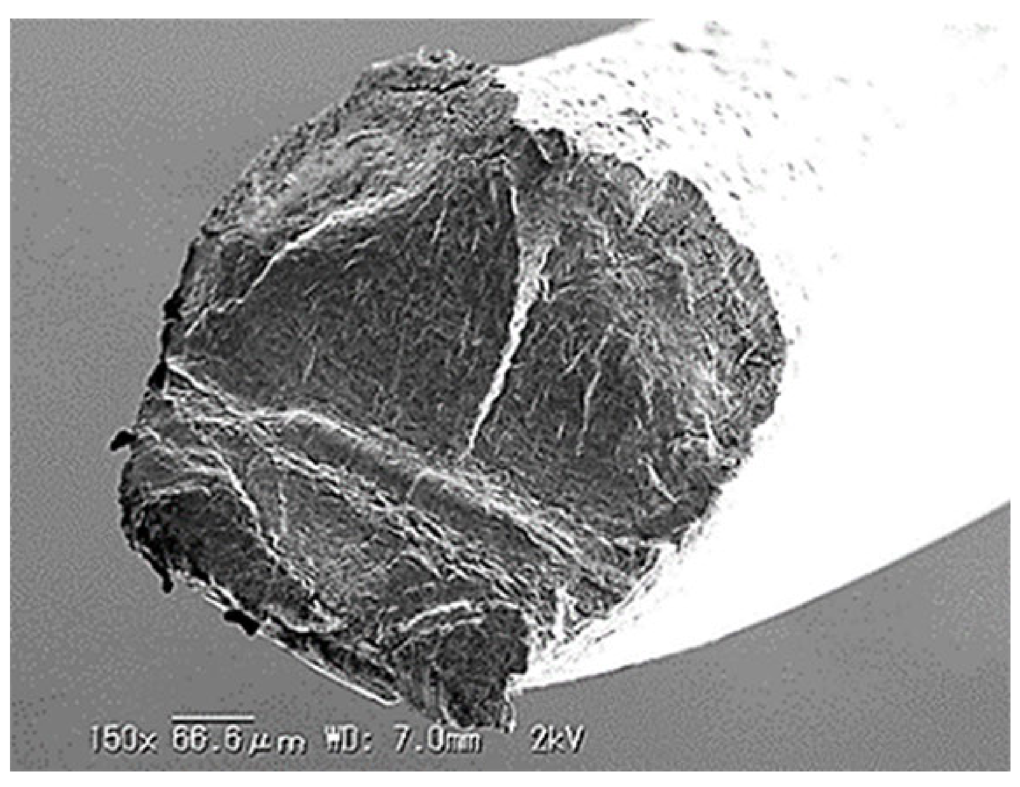


Figure 1. Typical wire break. Note rupture line near center.

Figure 2 shows the test wires made with either 20mm long wire or ribbon bonds spanning two aluminum plates spaced 5mm apart. The first bond side is stationary, and the second bond side subjected to vibration during testing.

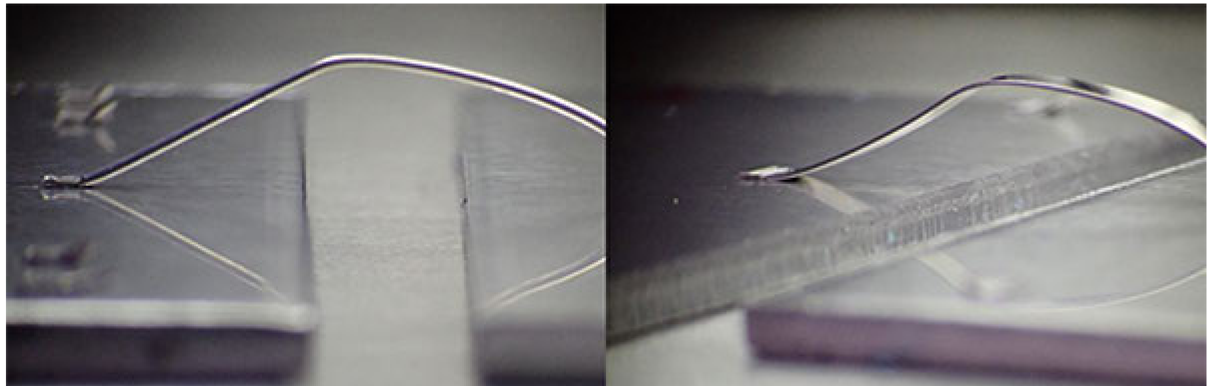


Figure 2. Round wires used in the study are 400μm in diameter (L) while the ribbons measure 2000μm x 200μm (R).

Results

The test conditions were designed to help understand the most significant factors that might contribute to broken wires in EV applications. The study consists of five tests composed of various factors as listed in **Table 2.** Three vibration axes (x, y, z), four types of aluminum wires, three loop heights, two wire shapes (round vs ribbon) were tested. The final test compared the performance of one bond vs. one wire vibration.

Table 2. Factors Used in the Study

Test No.	Factor	Comparison
1	Vibration direction	Three directions (x, y and z)
2	Wire material	Four Al wires (4N and alloyed)
3	Loop height	Low, medium and high loop heights
4	Wire shape	Round vs. ribbon
5	Bond vibration	Single vs. both bonds

Test 1: Vibration direction. The first set of tests was for the vibration of the second bond, with the first bond being stationary, in x, y or z axes with respect to the wirebond length using 400µm diameter Al wires.

As shown in **Figure 3,** in the x direction test where the wirebond is basically stretched, there is a high incidence of failure. This is akin to a tensile stress of the wirebond and the weakest link in this case, the neck region of the vibrated second bond, typically ruptured after at least a thousand cycles.

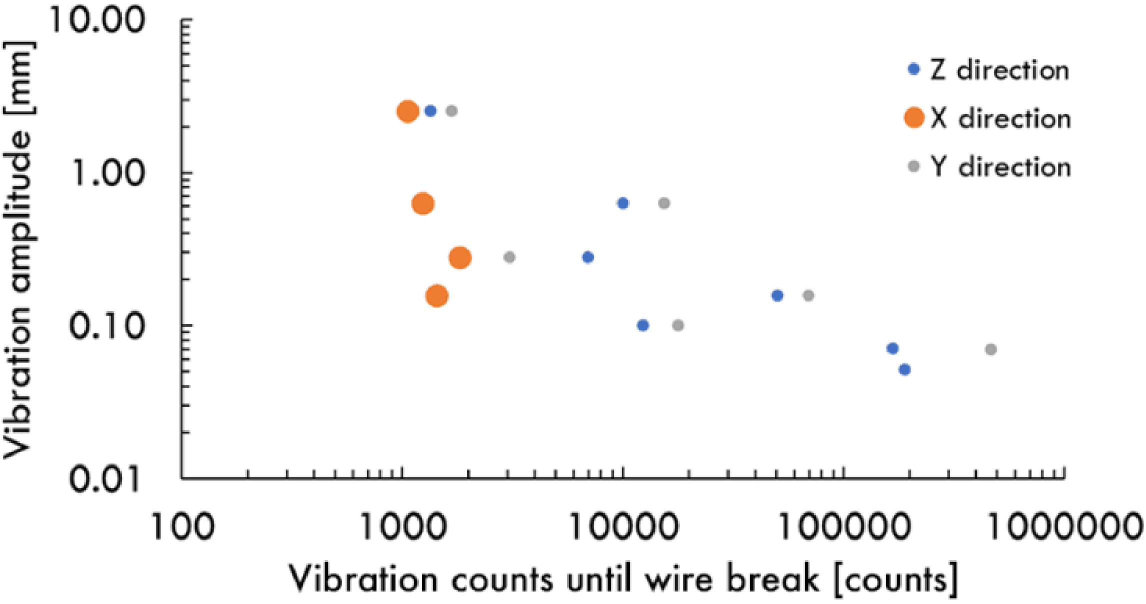


Figure 3. Wire breakage vs. vibration axes.

For the y direction where the second bond is vibrated from side to side with respect to the first bond, failures varied from 1,000 up to 1 million cycles. Surprisingly, the same failure rate was observed during the z direction vibration, where the second bond is vibrated up and down with respect to the first bond.

Test 2: Wire material. In the second test, four aluminum materials made in 400µm diameters with various tensile strength and electrical conductivity were compared as listed in **Table 3.**

Table 3. Aluminum Materials Tested

No.	Wire	Tensile Strength (MPa)	Electrical Conductivity (%IACS)
1	4N (99.99%) standard	50	63
2	Al alloy prototype-A	140	55
3	Al alloy prototype-B	130	50
4	Al alloy prototype-C	130	59

The results shown in **Figure 4** show no significant difference among the wires except perhaps for Al prototype alloy no. 2 where, if the amplitude <0.1mm, improved vibration resistance was observed near 1 million cycles compared to other wires, including the standard production wire.

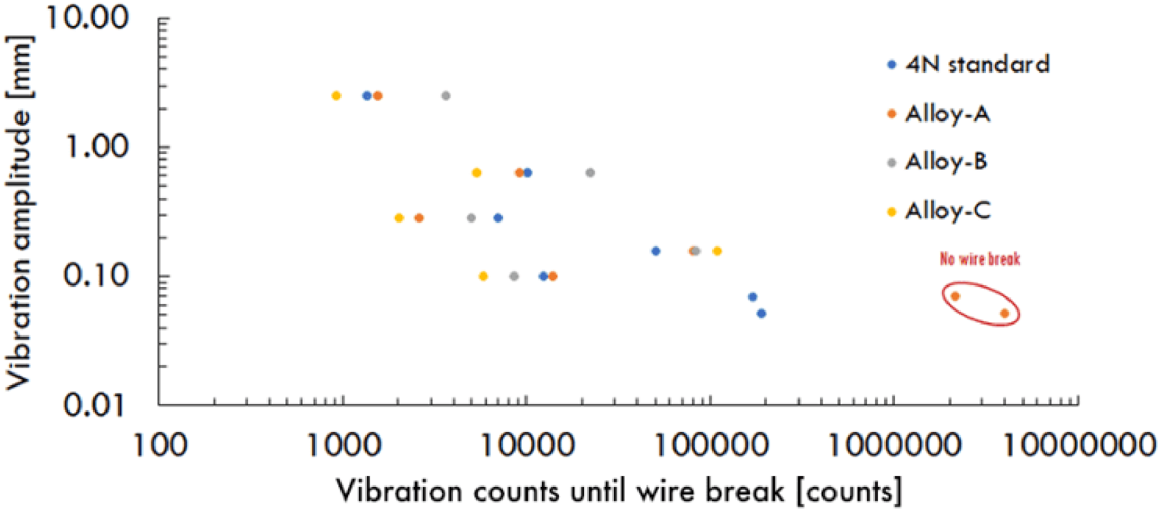


Figure 4. Wire break vs. Al material.

Test 3: Loop height. Test wirebonds were made with three loop heights: 2mm, 4mm and 8mm. As expected, the wirebond with the highest 8mm loop heights had slack that absorbed some of the vibration **(Figure 5)**, some of which lasted up to 1 million cycles without breaking.

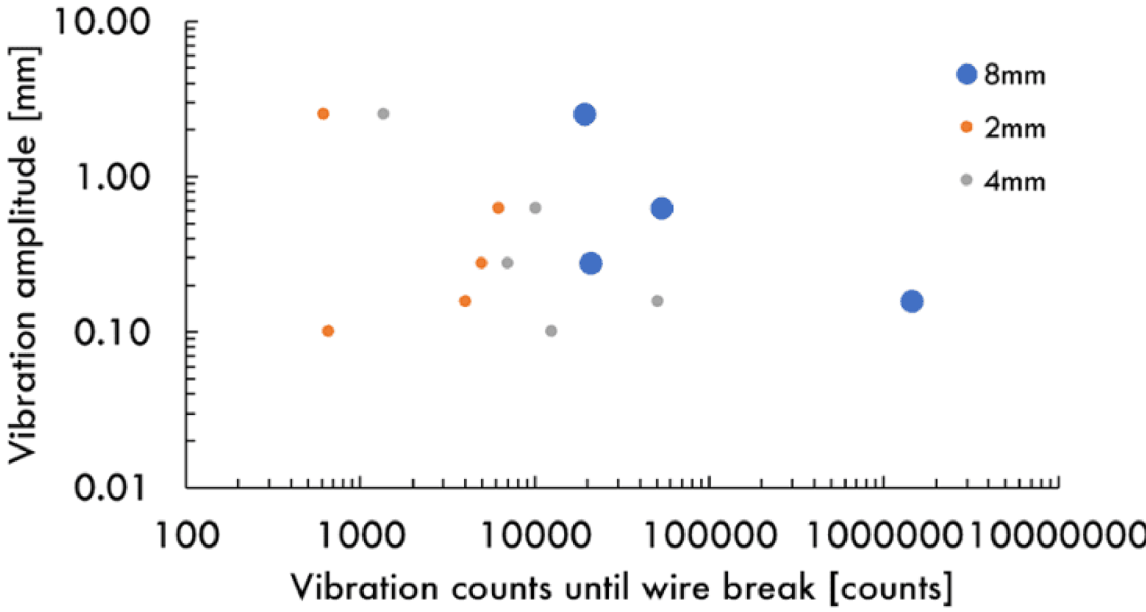


Figure 5. Wire break vs. loop height.

Test 4: Wire shape – round (400μm) vs. ribbon wire (2 x 0.2mm). Wire cross-section, either round or ribbon, was also investigated in all x, y and z axes, which resulted in significant but unsurprising results. In both z- and x-axis vibrations, the ribbon wirebond showed better vibration resistance than the round wirebond because of the former's inherent rigidity along its cross-sectional width. In the y-axis or sideways movement, the same rigidity of ribbon wirebond worked against it, resulting in increased breakage frequency.

Test 5: Bond vibration – First bond vs. both bonds (400μm Al). The fifth test determined the vibration resistance of a single bond versus whole wirebond. As expected, wirebonds break easily when only one of the bonds is vibrated. No breakage was observed if the whole wirebond was vibrated, even for extended periods.

Conclusions

The following are findings of the study:

- Bond terminals (battery cell and busbar) rigidity with respect to wirebond are important for enhanced vibration resistance;
- Loop height is directly proportional to vibration resistance;

- Higher strength wire showed higher vibration resistance but only with amplitudes <0.1mm;
- Ribbon wires showed better resistance than round wires in x and z vibration directions.

DODGIE CALPITO is business development manager at Tanaka Kikinzoku International (America), Inc.; dodgie@ml.tanaka.co.jp. **SHUICHI MITOMA** is a materials engineer, **SHIZU MATSUNAGA** is an analysis engineer, **KOSUKE ONO** is a wirebond engineer and **TSUKASA ICHIKAWA** is a materials engineer with Tanaka Denshi Kogyo K.K. (Japan).

GETTING **LEAN**

The Benefits of Internal Benchmarking

Looking within the organization can yield unexpected benefits.

BENCHMARKING IS AN integral part of any continuous improvement strategy. There are typically three types of benchmarking: cross-industry, competitive and internal. Cross-industry benchmarking looks at similar processes in different industries and often delivers the biggest breakthroughs because it helps companies identify processes and systems not widely used in their industries. One example is Southwest Airlines benchmarking NASCAR pit crews' performance. Competitive benchmarking looks at data from competitors. The challenge is that direct competitors are not likely to share at the level possible with a cross-industry benchmarking exercise, and given the similarity of processes, the best-case improvement is often just being as good as your best competitor.

Internal benchmarking can take two forms. In the first form, processes and systems are evaluated against Lean manufacturing standards to target areas of improvement. In the second form, different facilities of a company are benchmarked to find improvements based on differences in processes and systems.

SigmaTron is increasing its use of internal benchmarking. Its facilities each focus on the industries and customer requirements that they serve. For example, its Mexico and China operations typically run higher-volume products which often cost-justify specialized equipment, tooling or processes not as well developed in operations running lower volumes. One of the most common benchmarking activities involves equipment acquisition. As facilities consider upgrading equipment options, they look to other facilities to better understand the options and experiences with the equipment they use. This reduces the

learning curve associated with new technologies while providing more context on how this equipment operates in real-world environments. For example, when one of SigmaTron's facilities was adding nitrogen to reflow process, it benchmarked other facilities to determine whether nitrogen tanks or a generation unit made more sense.

Benchmarking can be virtual or onsite. The virtual process examines metrics, and the onsite process enables a team to view the operations they are studying. The increase in internal benchmarking has brought a switch from virtual benchmarking to onsite visits. Virtual benchmarking typically utilized a preplanned questionnaire, and while it saved on travel expenses, the downside was that it just gathered data found in the questionnaire. Improvements that weren't specifically asked about weren't mentioned in the response.

This issue was recently illustrated in a benchmarking trip that sent a five-person cross-functional team from the EGV facility in Elk Grove Village, IL, facility to one in Acuna, Mexico. One of the areas being evaluated was selective soldering. The Acuna facility's high-volume environment has made it an expert in solder pallet design, and its team has been designing EGV's solder pallets to requirements specified by EGV's team.

While in the facility, the team realized Acuna's solder pallets had additional features driven by poka-yoke that weren't incorporated in their pallet design. The Acuna pallet design poka-yoke incorporated features that made it impossible for an operator to place a component incorrectly, while the EGV facility had been using transparent overlays as a poka-yoke to eliminate this defect opportunity. Additionally, some Acuna pallets had been modified to shield the printed circuit board assembly (PCBA) from flux overspray. EGV had also modified some of its pallets to deal with this issue in conformal coating, but the Acuna shield design represented an improvement they hadn't considered.

The team included both technical and managerial resources. Teams composed exclusively of technical personnel tend to focus on production processes and equipment. Broadening the team to include managerial resources enables better analysis of non-value-added but necessary processes, such as planning and release of kits from the stockroom for potential improvements. Quality practices were also reviewed. The Acuna facility's higher volumes make it data-driven and focused on inspection efficiency. Operators check the work of the

previous station as part of this process. Additionally, acceptable quality level (AQL) data are utilized to determine sampling plans, and in some cases, specialized short-term inspection operations are set up to address specific issues.

Similarly, a recent all-hands meeting at EGV enabled personnel from other facilities to look at EGV processes. While not designed as a formal benchmarking effort, the tour generated discussions that will likely lead to further internal benchmarking efforts among facilities.

Multi-facility manufacturing operations benefit from focused internal benchmarking efforts. In some cases, this benchmarking may drive improvements in similar processes. In other cases, this benchmarking may create strategic partnerships where a facility deemed expert in an area such as tooling design can supply that expertise in facilities not able to justify developing that capability internally. Onsite benchmarking enables teams to view improvements they may not have been originally looking for. It also breaks down silos that can develop when different facilities have different areas of expertise.

ANITA TUCKER is the general manager of SigmaTron International's EGV facility. She can be reached at anita.tucker@sigmatronintl.com.

SEEING **IS BELIEVING**

Dealing with Deadbeats

A striking lesson in leverage against a larger opponent.

THE WORST PART is the silence. Experience says silence means they have nothing but bad news to report, and they're afraid to report it. The technique is notably effective when conveyed (or not because it's silent) across 10 or more time zones, thereby avoiding real time confrontation. Silence seldom means anything good.

So they say nothing. Employing the time-tested method of patient endurance, they expect by saying nothing that attention will be diverted inevitably, enabling the problem to magically go away. Just like politicians' common practice, taking a dim view of voters' average intelligence and grasp of the facts. People have short attention spans. They know that. They count on it.

The problem never goes away. Receivables still age until they're settled. You have to push. They need to know that you know. Otherwise, they wait it out, and the silence, their friend, prevails. Notch one more for them. And you're still not paid.

It's true, every now and then they'll throw you a bone to knock you off the scent, change the subject, and leave them alone.

Our apologies. We've experienced some turnover in our accounting department. Please be patient as we undergo some personnel changes, and we'll pay your outstanding balance as soon as possible.

Stalling Tactic #1: Thank you for your patience.

Time to appeal to the principals.

Not my job, say the engineers and the engineering managers. Assuming they respond at all.

Wrong department.

Plausible deniability thrives in a far-flung organization. Easy to blame a faceless Someone Else of an abstraction who's halfway around the world, and beyond accountability.

We persist.

To our new demand for payment, the response is anodyne and formulaic.

We await closure of our latest funding round. It will be a few more days, possibly a week or two but, rest assured, your account has been given highest priority for payment.

Stalling Tactic #2: Keep thanking them for their patience.

The dynamics change overnight when they want something. Suddenly it's urgent, and emails get returned. Their request – really a demand – reeks of entitlement:

I have a high-level expedite request coming in from one of our key customers that needs these parts. Is there any way you can please expedite these parts for us and complete today for pick-up either tonight or first thing in the morning? That would allow us to complete our stuff and ship something on Saturday; otherwise, we are in next week. You guys have always done a great job for us, and I'm hoping you can pull through on this one. This customer is about to give us a large new contract which will be great business for both of us going forward. This will help seal the deal. Let me know if there is someone else in your organization that could help if we escalate our request.

Escalate? To whom? In case you missed it, the title on the email was P-R-E-S-I-D-E-N-T.

Busy guy. Doing important work. Short attention span shows he has his priorities straight. Nice touch on his part, dropping the hint that we could make beautiful music together next year, if only we have x-ray results by 8 a.m. tomorrow morning. Thus inspired, let's take that

hill. Wondrous things they teach in MBA school.

There's still that inconvenient matter of nonpayment.

We try a third time. The answer is the same.

We continue to await closure of our latest funding round. It has been delayed several times due to banking complications. We await closure any day, and we thank you for your patience.

As if we are a bottomless pit of patience. Which we are not. So much for Stalling Tactic #3.

It all started promisingly enough, five or six years ago. They came to us. Local engineers looking for local support. Local failure analysis, performed in a week or less to give feedback to the line. Drop parts off Monday; receive uploaded images by Friday. Sometimes sooner if we weren't that busy. We'd charge by the hour: typically two to four hours per job, done during our swing shift. It was not uncommon during slow periods for parts to be dropped off at 5 p.m., with results available the following day or the next day at the latest. At busier times, during an epidemic of failures, not unknown in this business, with long x-ray queues, results might wait for three or four days. But always done in a week or less. And we got paid in about 30 days. They were content; we were content.

They sealed their confidence in us with a blanket purchase order, covering six months' failure analysis activity, in support of multiple engineering teams. No need for new quotes, and new orders, for every project. All they had to do was drop the parts off, notify us whose project it was, and the rest would happen, on trust. Autopilot actually. Nice business.

Enter Private Equity. Our cozy little relationship was merged and acquired into a state of operational frenzy. Our locally based customer, with intimate knowledge of us, and we of them, became, courtesy of financial engineering, a micro cog in a macro, multinational wheel. Somewhere, somehow, our x-ray services became, in the minds of those driving spreadsheets, indistinguishable from a vending machine: insert units here, expect images there, on demand, every time. Alert and in readiness 24/7. Like flipping a switch. At a bargain hourly rate. At their beck and call on the metaphorical Front Porch, sipping metaphorical mint juleps until the siren sounds.

As if we have nothing else to do.

Private equity wants services faster. The spreadsheets were specific: everything needed to be done overnight, including x-ray and CT scanning services. The fate of everything hung in the balance, 100% of the time. Operating expectations were that parts would always be dropped off at 5 p.m. and picked up the following morning at 8 a.m., every time. For no premium.

And no payment.

Being private equity, they wanted to preserve the asset side of their balance sheet, especially the short-term asset conventionally labeled, "cash and cash equivalents." The best way to preserve that asset is to not spend cash. Which to their way of thinking is acceptable because cash only goes to vendors (none dare call them "suppliers"). Vendors are expendable (see note above about vending machines). Better to hold it as long as possible, until the vendors scream.

Curiously, beginning with the consummation of the acquisition, payment times began to lengthen. Aging increased from 30 days to 45 days, to 60 days, to 90 days. The increases happened gradually, resembling the predicament of the slowly boiling frog, whose doom is sealed when he realizes the harsh reality of his situation, too late. They rely on our not noticing.

We noticed.

Especially when July invoices, for very rapid-turnaround FA work, remained unpaid in November. Irony noted, and reciprocation is for suckers.

Something must give. We have something they want, desperately. So much so that their managers are calling to micromanage completion and delivery.

We understand you operate a swing shift. We'd like you to x-ray our units this evening, so that we may pick them up, with images, first thing in the morning.

They have something we want.

We understand you operate what could best be described as a scam, trading worthless promises of payment for performance concessions from us. Nice try.

Time to play the Ace of Spades.

> Dear Customer,
>
> You have not paid us in two months, despite numerous requests for payment status. It is now November. Your company owes us $XX,XXX.00 to date, most of it in past due invoices going back to July, 135 days ago. Our terms are net 30, not net 135. I have repeatedly asked your colleagues and your management to allow me to speak to someone in authority at your company who can pay these past due amounts and pledge to honor our terms going forward. To date I have had no response to my request but silence from management. Silence is not a response. I have also repeatedly emailed your Accounts Payable with the same request. Same worthless response: silence, punctuated by occasional weak pleas, detailing excuses such as personnel changes, pending funding rounds, and flimsy arguments unsupported by facts about net 120 being standard business practice in our industry. Personnel turnover is no excuse for nonpayment. Nor is the timing of funding rounds: that's what lines of credit address. As to the argument that net 120 is the norm, see the April edition of *Aviation Week**.* Be careful about making unsupported assertions regarding standard business practices. Come up with a better argument. Better yet, pay your bill.
>
> Unless and until this problem of nonpayment has been addressed to our satisfaction, we will hold your parts and the x-ray results at our facility. We hate to do this, but your actions – or rather, lack of them – leave us no choice. You created this problem, and you can solve it, as fast as we are able to inspect your parts. Well, almost as fast. Back to you.
>
> Thank you for your attention to this urgent matter. You know how to reach me if you wish to discuss further, which would be uncharacteristically refreshing.
>
> Happy Holidays

Full payment of the past due amounts cleared our bank within 72 hours.

*Kevin Michaels, "Suppliers Aren't Banks: Why Payment Terms Need to Change," *Aviation Week & Space Technology,* April 10-23, 2023.

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

EASYLOGIX PCB-INVESTIGATOR V15

PCB-Investigator Version 15 new features include design history to log actions and exports, with log entries for designs from the PCBI 365 Cloud stored directly in 365. Also permits several PCBI 365 Cloud Servers to be integrated at the same time. New Part Expert connects BoM information from the design directly with data sources such as DigiKey, Mouser, Avnet and Octopart, which permits reports to be created on prices, availability and delivery times. Also includes IPC-2581C importer and IDX Exporter, plus additions and improvements in Analysis and Production Control.

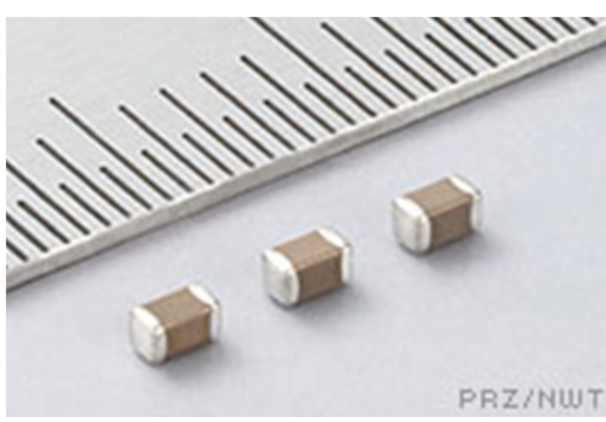
EasyLogix
easylogix.de

KYOCERA LINEAR CARD-EDGE CONNECTORS

9159-7X0 series linear card-edge connectors feature beryllium copper spring contact system, said to deliver high electrical and mechanical reliability, high signal integrity and high durability in harsh environment applications. Comes in open- and closed-side

configurations with high-temperature white or black UL94 V-0 insulators, five contact variations (4, 6, 8, 10, and 12 positions), gold or tin over nickel contact plating, and current ratings up to 2A per contact. Is designed to mate with 1.5mm-thick (±0.15mm) PCBs with gold- or tin-plated pads and is rated for 150VACrms or the DC equivalent, up to 1,000 cycles with gold-plated contacts (up to 20 with tin), and operating temperatures extending from -40° to +130°C. Is UL and RoHS compliant and can be customized to suit customers' specifications. For linear PCB mating in harsh industrial, LED lighting, automotive lighting, and transportation lighting applications.

Kyocera AVX
kyocera-avx.com



MURATA MANUFACTURING CERAMIC CAPACITOR

GRM188D72A105KE01 multilayer ceramic capacitor features 1μF capacitance in a 1608M (1.6 x 0.8mm) size. Is rated at 100V for use in 48V power supply lines in base stations, servers, and data centers. Uses proprietary thin layer technology to permit capacitor to be approximately 67% smaller in volume and 49% smaller in area than Murata's 2012M size multilayer ceramic capacitors.

Murata Manufacturing
murata.com

RENISHAW RENAM 500 ULTRA 3-D PRINTER

RenAM 500 Ultra laser powder bed fusion (LPBF) 3-D printer incorporates new scanning algorithms that permit the laser to fire while the recoater is moving, saving up to 9 sec. per build layer. Also features advanced process monitoring software that delivers detailed insights into the build to provide users with data and in-process visibility. Available with one (500S) or four (500Q) high-power lasers, each able to access the whole powder bed simultaneously.

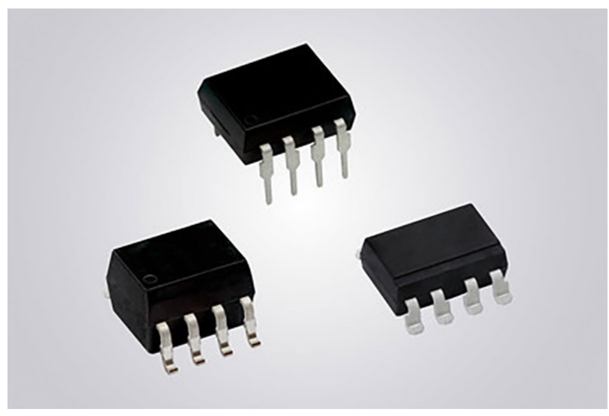
Renishaw

renishaw.com

SWANCOR EZCICLO EPOXY HARDENER

EzCiclo low-dielectric epoxy hardener is tailored for copper-clad laminates and enables use of recycled waste plastics in PCB production. Uses more than 80% of waste plastic materials while retaining the properties of traditional hardeners. Enhances the electrical properties of epoxy resin FR-4 boards, achieving Dk-2.78/Df-0.011 at 10GHz after pure resin curing. Also increases the recyclable material content of PCBs, as the CCL can be decomposed by proprietary chemical treatment, allowing separation of resin and glass fiber from circuit board. Can be applied to any product that uses a PCB, including general electronic products, in-vehicle or network communications.

Swancor

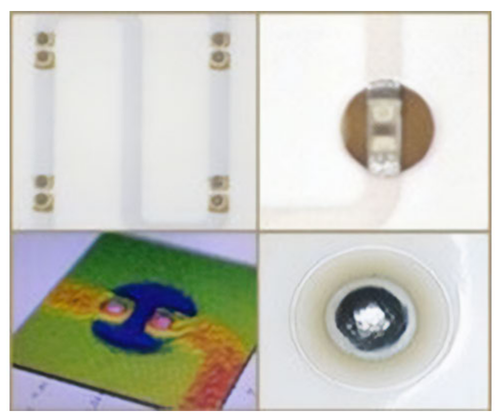


VISHAY 10MBD OPTOCOUPLERS

10MBd high-speed optocouplers provide low power consumption to save energy in industrial applications. Includes single-channel VOH260A, VOIH060A, and VOWH260A and dual-channel VOH263A and VOIH063A, and features a voltage supply range of 2.7V to 5.5V and an open collector output. Come in DIP-8, SMD-8, and SOIC-8 packages and utilize a highly efficient input LED coupled to an integrated photodetector logic gate with a strobable output. Combine a low supply current of 5mA maximum per channel with a low typical turn-on threshold current of 2mA typical. Are for data communications, high-speed A/D and D/A conversion, level shifting, and providing high voltage safety in automation equipment, motor drives and tools. Feature an internal shield that provides a guaranteed common mode transient immunity (CMTI) of 15kV/μs minimum. Offer maximum rated withstand isolation voltage up to 5000VRMS and provide isolation distances from 5mm to 10mm to cover a wide range of requirements, including those of applications with working voltages exceeding 1000V.

Vishay

vishay.com



AIM NC259FPA SOLDER PASTE

NC259FPA zero-halogen solder paste is engineered for precise print definition with Type 6 and smaller alloy powders through stencil apertures less than 150µm in diameter. Is for miniLED, microLED, die attach, µBGA, and HDI boards, and features excellent wetting, high transfer efficiency, high reliability, and high tack force for mass transfer.

AIM Solder

aimsolder.com

ASMPT CMAT-S PRODUCTION SYSTEM

CMAT-S is an all-in-one system for assembling and dynamically aligning lenses in ADAS cameras. Features Continuous Sweep Alignment process, which is said to significantly improve system throughput without compromising on quality of cameras installed in advanced driver assistance systems. Reduces process cycle time by a reported 50% in the

same footprint. Aligns lenses for ADAS cameras in 10 sec. and below per camera. Employs a proprietary and patented algorithm for its active alignments, and takes advantage of the continuous movement of the target object during imaging to increase precision and speed of alignment process. Comes with V curing system with partial curing times of as few as 1 sec. for certain camera modules.

ASMPT
asmpt.com

ANTENOVA SURFACE MOUNT WIRELESS ANTENNAS

Curta SR4L096, Abdita SCRW090 and Admotus SRCG091 wireless antennas are designed and developed for three different wireless technologies.

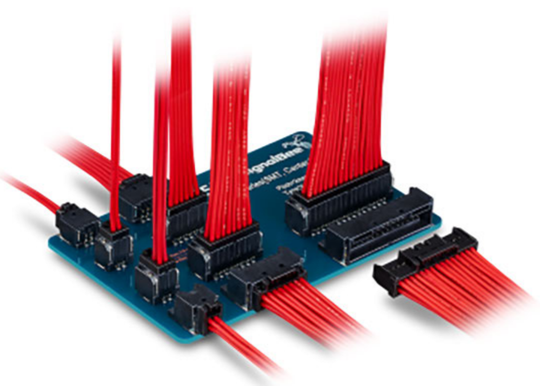
Curta SR4L096 is a surface mount antenna measuring 40 x 10 x 1.7mm with placement on the short end of the host PCB. Is designed for coexistence requirements, which can be integrated as a single antenna or in a MIMO system. Supports many technologies – LTE, GSM, CDMA, DCS, PCS, WCDMA, UMTS, HSPDA, GPRS, EDGE, and IMT that cover multiple bands and provide optimal efficiency ratings – 698-960MHz (56%); 1710-2170MHz (66%); 2300-2400MHz (52%); and 2500-2700MHz (53%). Average peak gain ranges from -2.5dB, -1.7dB, -2.8dB, and -2.7dB, respectively. Temperature range is -40° to 140°C.

Abdita SCRW090 is a surface mount ceramic antenna that can be integrated into a design and operate on various GND plane sizes. Utilizes a ground plane to radiate efficiently in

2.4GHz applications such as Bluetooth/BLE, WiFi (802.11a/b/g/n), and ZigBee. Is said to offer longer range connectivity than most ceramic antennas due to its higher efficiency of 60.5%. Has an overall size of 1 x 0.5 x 0.5mm and fits on PCB as small as 50 x 30mm and requires 7 x 7mm clearance area. Operating temperature ranges from -40° to 125°C. Peak gain is 2.8dBi with an average gain of -1.9dB. Maximum return loss is -13.0dB and has maximum VSWR at 1.6:1.

Admotus SRCG091 is a surface mount ceramic antenna designed for connectivity on L1 GNSS signals on all constellations including GPS-L1 at 1575.42MHz; GLONASS L1, 1602MHz; Galileo L1, 1575.42MHz; BeiDou (B1); and QZSS. Is said to provide comparable performance to a small patch antenna on a small ground plane. Measures 1.0 x 0.5 x 0.5mm, requires 7.0 x 15mm clearance area and is said to perform well on small PCB sizes. Offers peak gain of 0.9dBi with average gain of -2.6dB, provides maximum return loss of -11.5dB and maximum VSWR 1.8:1.

Antenova
antenova.com



HIROSE SMT WIRE-TO-BOARD CONNECTOR

DF51K wire-to-board connector series now includes an SMT version. Is compatible with automated assembly processes, including pick-and-place machines, and features a center lock design to offer high-density mounting on PCB while preventing damage during cable assembly and ensuring secure mating. Positive lock provides a clear tactile click and

secures a reliable connection and enables users to recognize reverse-mating and prevents mechanical interference. Supports up to 3A and is designed for a broad range of products, including industrial machinery, medical equipment, office equipment, robotics, smart meters and more. Has a rated voltage of 650V AC/DC and an operating temperature of -55° to +105°C.

Hirose Electric

hirose.com

KURTZ ERSA POWERFLOW ULTRA WAVE SOLDERING

Powerflow Ultra wave soldering machine features a new soldering module capable of speeds of up to 5mm/s. Is available with frame and finger conveyor, with working widths ranging from 330mm to 610mm in the XXL version. Distance between soldering nozzle and PCB is defined via the Ersasoft 5 operating software, which permits assemblies to be soldered at a precise distance, and nozzle distance and solder wave height can also be adjusted as required within an assembly. Also features the permanent measurement of real solder volume – independent of pump speed and tin level – using a sensor and automatic solder feeding, which significantly shortens measuring times and increases system availability. Also features a modular design that enables optimum adaptation of the system configuration to customer-specific requirements, such as the availability of three different preheating lengths: 1.8m, 2.4m and 3m.

Kurtz Ersa

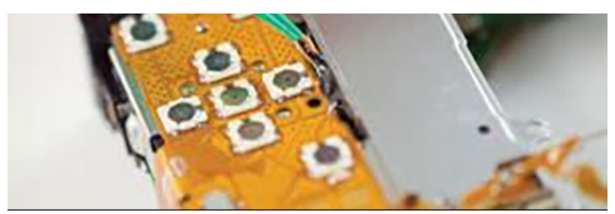
kurtzersa.com

KURTZ ERSA VERSAFLOW ONE X-SERIES SELECTIVE SOLDERING

Versaflow One X-Series of selective soldering machines offers the option of two pots per soldering module, and can process up to eight assemblies (max. dimensions 350 x 508mm) and up to four assemblies (max. dimensions 508 x 508mm) simultaneously. Features a 3mm pin chain/roller conveyor and program-controlled width adjustment as standard for maximum flexibility and performance, plus a flux module that features a multidrop system, with one or two flux heads and numerous options, that offers the precision to handle almost any conceivable geometry. Includes a basic version of a preheater that is equipped with a short-wave IR heating module from below, with top heating with convection in the preheater available as an option. Also offers contactless monitoring of the PCB temperature in the preheater, and features such as automatic nozzle activation and solder wire feed are also on board. Also includes connection to the KE Connect digital service platform on request.

Kurtz Ersa

kurtzersa.com



MASTER BOND UV23FLDC-80TK EPOXY

UV23FLDC-80TK is a moderate viscosity, cationic type system that offers both UV-light- and heat-curing mechanisms. Cures readily within 20-30 sec. when exposed to a UV light source emitting a wavelength of 320-365nm. Can also undergo a secondary heat curing for shadowed areas, typically curing in 60-90 min. at 80°-85°C. Has a viscosity of 25,000-50,000cps, and is highly thixotropic. Has a low tensile modulus of 250-500psi, and a high elongation of 90-100% at room temperature. Withstands rigorous thermal cycling, and is said to feature excellent electrical insulation with a volume resistivity exceeding 10^{14}Ω-cm. Is not susceptible to oxygen inhibition and bonds well to metals, glass, ceramics and many plastics, including but not limited to acrylics and polycarbonates. Has a service temperature ranging from -80° to +300°F and comes in a wide range of packaging options, including syringes, ½ pint, pint, quart and gallon containers.

Master Bond

masterbond.com

MEK SPECTORBOX X1 AOI

SpectorBOX X series is a modular full 3-D AOI for through-hole technology (THT) solder

joints and THT components. Can be used bottom-up for volume measurement of THT solder joints and pin height measurement, or top-down for a 150mm+ clearance for 3-D THT components measurement. Delivers direct volumetric measurements of solder joints from selective, wave, robotic, pin-in-paste reflow, laser and manual soldering systems in addition to accurate pin height measurement. Offers a clearance of 150mm (5.9") and beyond on the component side and over 100mm (3.9") on the solder side to accommodate most conveyor designs, and the x, y and z-axis moving optics ensure inspection of most pallet designs.

Marantz Electronics

marantz-electronics.com

NORDSON ASYMTEK SL-1040 CONFORMAL COATER

Asymtek Select Coat SL-1040 conformal coating system includes system-level advancements to elevate automation, control, precision and preventive maintenance for better yield and uptime. Pairs new process control and preventive maintenance with the new SC-450 PreciseCoat Jet and enhanced EasyCoat software that are ideal for high-volume production. Dual and triple applicators maximize throughput, and flexible features drive better yields through efficient changeover, traceability and setup consistency. Also features a new ultrasonic cleaning station that simplifies nozzle cleaning to improve uptime and cost of ownership. Includes advanced safety features, ESD-safe components and compliance to standards including SMEMA, CE, NFPA, and SEMI.

Nordson Electronics Solutions

nordson.com

STIRRI LT-HF SOLDER PASTE

LT-HF solder paste is a low-temperature halogen-free solder paste with an optical tracer. Incorporates QC-Aid to harness UV light and permit immediate visual PCB contamination inspection without complex testing equipment or training. Specially designed for tin-bismuth applications, and ensures exceptional soldering performance while maintaining the longevity and reliability of delicate electronic components promoting mechanical properties of bismuth-containing alloys while enabling instant optional visual QC.

Stirri

stirri.com

TAGARNO T50 DIGITAL MICROSCOPE

T50 digital microscope is equipped with a 4K/60FPS block camera to provide a seamless and lag-free viewing experience. Is compatible with +3, +4, +5, +10, +25 and +50 lenses, at a magnification level of 1.3x to 660x and a field of view of 0.8mm to 409mm. Features a magnetic ring light that is also controlled with the same control box as the microscope to reduce the number of control boxes needed in the workspace, and readjusts height automatically to keep images in focus.

Tagarno

tagarno.com

TECHCON EXTRA-LARGE SYRINGE BARREL

TS60C-LL-N syringe barrel features a capacity of 177cc/6oz. Is made of clear polypropylene, is free of silicon and chloride and features a design with consistent internal diameter to maintain the proper seal with the piston for optimal dispensing results. Also features an ultra-low draft construction of the inner diameter that results in high dispensing accuracy and stability. Can connect directly to air adapters, and is for bonding, underfill, potting, and conformal coating. Is compatible with most dispensing materials including adhesives, epoxies, sealants and solder pastes.

Techcon

techcon.com

TRI TR7600F2D LARGE BOARD AXI

TR7600F2D QL AXI is designed for the evolving needs of large board applications, especially in automotive and telecommunications electronics manufacturing. Inspects large boards measuring up to 2100 x 510mm and is capable of inspection with resolution ranges from 5-25µm. Is equipped with AI algorithms surpassing conventional gray-level-based methods, and is said to excel in detecting void and open defects, ensuring reliability in identifying

defects across various components such as BGAs, capacitors, chips, WLCSP, DIMM connectors and more. Also features a specialized 2-D camera specifically designed for automotive applications, including barcode reading and fiducial detection. Supports current Smart Factory Standards, including IPC-CFX, IPC-DPMX, and Hermes (IPC-HERMES-9852).

TRI

tri.com

VISCOTEC ECO-PEN XS 180 MICRODISPENSER

eco-PEN XS 180 volumetric microdispenser dispenses quantities as small as 0.25µL and beads as narrow as 0.1mm, depending on the material. Weighs 175g and can be used for high-speed, high-acceleration operations. Multiple units can be coupled together in an automated dispensing cell with 25mm spacing between valves. Dispenses a variety of materials, including solder pastes, die-attach adhesives, edge-bond adhesives, electrically conductive adhesives, underfills and potting materials. Progressive cavity dispenser accommodates a range of viscosities, and filled materials can be dispensed with low shear, which prevents material separations or the destruction of filler particles.

ViscoTec

viscotec.com

TECHNICAL **ABSTRACTS**

In Case You Missed It

AME Solderability

"Solderability of Additively Manufactured Copper Surfaces"

Authors: Rebecca Wheeling, *et. al.*

Abstract: As additive manufacturing technology for copper rapidly evolves, the likelihood exists for downstream joining like soldering and brazing. A solderability study was performed to assess process fundamentals over a variety of AM approaches. The solderability of seven different copper (Cu) surface types were evaluated using the wetting balance technique: four Cu coatings (CP-007 and CP-008 conductive copper pastes, IMC-4118 conductive laser sinter paste, IMC-2501 copper ink), two laser-processed Cu surfaces, and one bulk additively manufactured (AM) Cu coupon type. Laser-processed surfaces were subjected to either circular or linear laser raster patterns. AM coupons were fabricated via a powder-bed laser process. In-situ force measurements were recorded while coupons were dipped into and removed from a 63Sn37Pb (SnPb) or 96.4Sn3.0Ag0.6Cu (SAC 305) solder bath, permitting contact angles and surface energies to be calculated. Meniscus height values were also measured. Surfaces were characterized before and after dipping via optical and electron microscopy. Results conclusively indicated that although all samples were intended to represent pure Cu, wettability was found to be strongly dependent on surface type with several samples exhibiting no wetting. Although the CP-007 paste performed the best of any nontraditional surface, all nontraditional surfaces saw significant wettability improvements with aggressive cleaning via HCl etching. (*Journal of Surface Mount Technology,* October 2023, https://doi.org/10.37665/smt.v36i3.32)

Routing

"A Novel Global Routing Algorithm for Printed Circuit Boards Based on Triangular Grid"

Authors: Jiarui Chen, *et. al.*

Abstract: Global routing plays a crucial role in printed circuit board (PCB) design and affects the cost of the design significantly. Conventional methods based on rectangular grids have some limitations, whereas this paper introduces a new algorithm that employs a triangular grid model, which offers a more efficient solution to the problem. First, the authors present a technique to sort all unconnected two-pin nets. Next, a triangular grid graph is constructed to represent the routing resources on the printed circuit board. Finally, the authors use the concept of maximum flow to identify the paths for global routing and apply detailed routing for the completion of wires. Results from experiments demonstrate that the authors' algorithm is faster than two state-of-the-art routers and does not have any design rule violations for all industrial PCB instances. (*Electronics,* December 2023, https://doi.org/10.3390/electronics12244942)

Thermal Conductance

"Material Characteristics Governing In-Plane Phonon-Polariton Thermal Conductance"

Authors: Jacob Minyard and Thomas E. Beechem

Abstract: The material dependence of phonon-polariton-based in-plane thermal conductance is investigated by examining systems composed of air and several wurtzite and zinc-blende crystals. Phonon-polariton-based thermal conductance varies by over an order of magnitude (~0.5–60nW/K), similar to the variation observed in the materials corresponding to bulk thermal conductivity. Regardless of the material, phonon-polaritons exhibit similar thermal conductance to that of phonons when layers become ultrathin (~10nm), suggesting the generality of the effect at these length-scales. A figure of merit is proposed to explain the large variation of in-plane polariton thermal conductance that is composed entirely of easily predicted and measured optical phonon energies and lifetimes. Using this figure of merit, in-

plane phonon-polariton thermal conductance enlarges with increases in 1) optical phonon energies, 2) splitting between transverse and longitudinal mode pairs, and 3) phonon lifetimes. (*Journal of Applied Physics,* October 2023, https://doi.org/10.1063/5.0173917)

Thermal Performance

"Thermal Modeling of Hybrid Three-Dimensional Integrated, Ring-Based Silicon Photonic–Electronic Transceivers"

Authors: David Coenen, *et. al.*

Abstract: Co-packaged optics for high performance computing or other data center applications requires dense integration of silicon photonic integrated circuits (PICs) with electronic integrated circuits (EICs). This work discusses the impact of three-dimensional (3-D) hybrid integration on the thermal performance of Si ring-based photonic devices in wavelength-division multiplexing PICs. A thermal finite element model of the EIC-PIC assembly is developed and calibrated with thermo-optic device measurements, before and after integration of an electrical driver on top of the PIC by means of microbump flip-chip bonding. Both measurements and simulations of the thermal tuning efficiency and crosstalk between silicon photonic devices show that the EIC can have a significant impact on the thermal performance of the integrated heaters in the PIC by acting as an undesired heat spreader. This heat spreading lowers the heater efficiency to 43.3% and increases thermal crosstalk between the devices by up to 44.4% compared with a PIC-only case. Finally, it is shown that these negative thermal effects of 3-D integration can largely be mitigated by a thermally aware design of the microbump array and the back-end-of-line interconnect, guided by the calibrated thermal simulation model. (*Journal of Optical Microsystems,* December 2023, https://doi.org/10.1117/1.JOM.4.1.011004)