Burkhert: What is Wafer-Level Chip-Scale Packaging?

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February 2024

Understanding the Sources of Crosstalk

MiXeD SiGNaLS

- Effects of Trace Coatings and Via Fillings
- Touring Chicago's Assembly Shops
- EMA's CAD Spinoff
- A Closer Look at HDI

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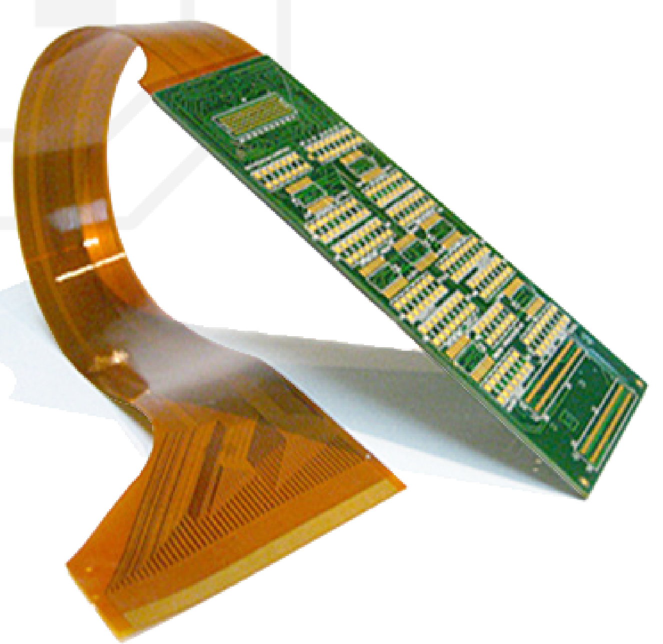

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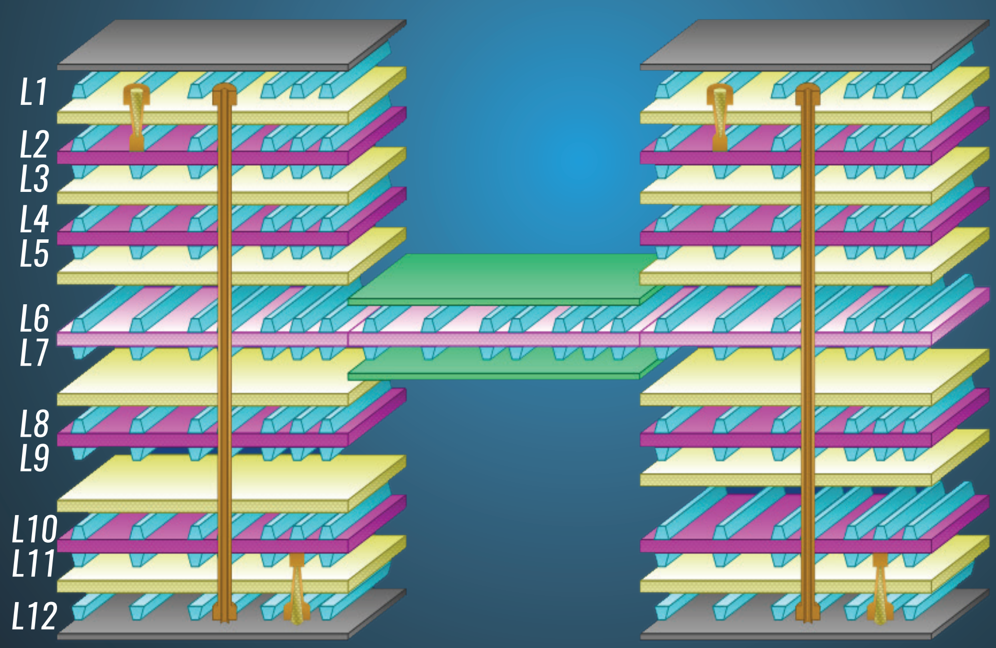

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FIRST PERSON

THE ROUTE
Message for the future.
Mike Buetow

MONEY MATTERS

ROI
Finding a middle ground.
Peter Bigelow

BOARD BUYING
New year, new cost savings.
Greg Papandrew

FOCUS ON BUSINESS
Tailor business to your customers.
Susan Mucha

TECH TALK

DESIGNER'S NOTEBOOK
Get to know WLCSP.
John Burkhert Jr.

DESIGN BEST PRACTICES
More power through multiple boards.
Stephen Chavez

MATERIAL GAINS
The PCB space race.
Alun Morgan

ROUGHLY SPEAKING
New skills on the block.
Geoffrey Hazelett

THE FLEXERTS
Eliminating through-holes.
Nick Koop

TECHNICAL ABSTRACTS

DEPARTMENTS

AROUND THE WORLD

PCEA CURRENT EVENTS

MARKET WATCH

OFF THE SHELF

FEATURES

CONDUCTIVITY
Do Trace Coatings or Via Fillings Improve (Thermal or Electrical) Conductivity?
A number of people and board manufacturers suggest that coating a trace or filling a via cavity can result in significant thermal and/or electrical conductivity improvements, but this is usually not the case. A look at via fillings and trace coatings and the effect that different materials can have on conductivity.
by DOUGLAS BROOKS and DR. JOHANNES ADAM

SIGNAL MODELING (COVER STORY)
How Interconnects Work: Anatomy of Crosstalk
Crosstalk in PCB and packaging interconnects can cause signal degradation that results in costly redesigns, but many designers do not know how to correctly identify its sources and mitigate its effects. An overview of crosstalk sources and terminology, plus models for identifying its effects.
by YURIY SHLEPNEV, PH.D.

LEFT SHIFT
Building the Efficient Design System
EMA Design Automation recently announced that it will be spinning off its software products for library management, component supply chain data, and other areas into a new company, Accelerated Designs. President Manny Marcano discusses the rationale and plans for the new company.
by MIKE BUETOW

MINIATURIZATION
High-Density Interconnect Technology: An Overview
Production and assembly of HDI PCBs comes with unique technical challenges centered around reliability and quality. An overview of standards and best practices for designing and building HDI PCBs.
by AKBER ROY

ASSEMBLY SERVICES
Windy City Tour
While not as well-recognized as the Silicon Valley, Chicagoland is another US hotbed of EMS activity. PCD&F/CIRCUITS ASSEMBLY visited a trio of area companies – Imagineering, BEST and BESTProto – each of which specializes in different niches but has recognized the need for responsiveness in a demanding environment.
by TYLER HANES

ON PCB CHAT (PCBCHAT.COM)

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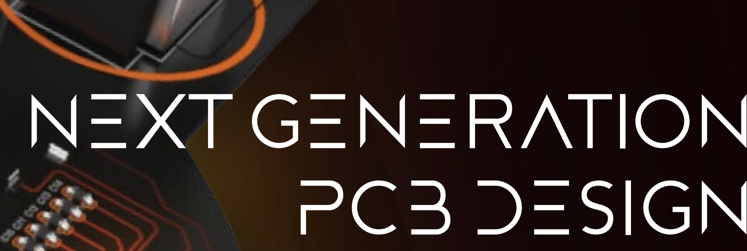

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IF YOU HAVE a child in Mrs. Dollas' eighth-grade class at the Rupert A. Nock Middle School in Newburyport, MA, odds are you are probably pretty steamed with me right now.

For those who aren't up to speed, here's why.

On a cold winter day in mid-January, I addressed her students about careers in electronics. About 20 teens gathered for the school's ongoing career exploration series (which as an aside, is a wonderful concept that all middle schools should adopt). I was invited to speak about my own career, but I quickly pivoted to the possibilities in tech that don't involve creating an app.

After asking for a show of hands from those who have been scolded by their folks for excessive video game playing – all of them – I then served them a counterargument: Play more!

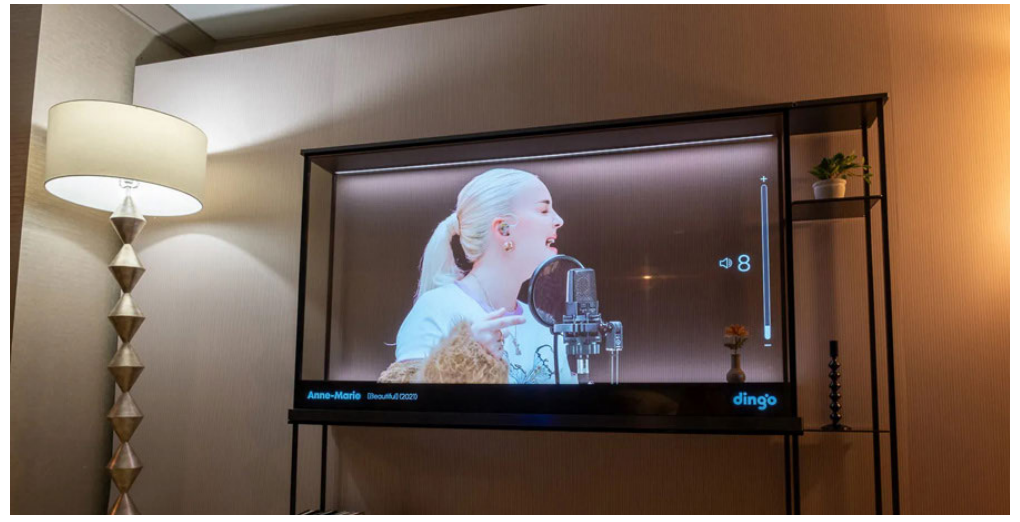
My reason, I explained, is because video games – well, many of them – encourage students to use their imaginations. And while acknowledging their inherent addictiveness, I also believe they impart tremendous skills and subtle knowledge that will be useful to future generations of workers.

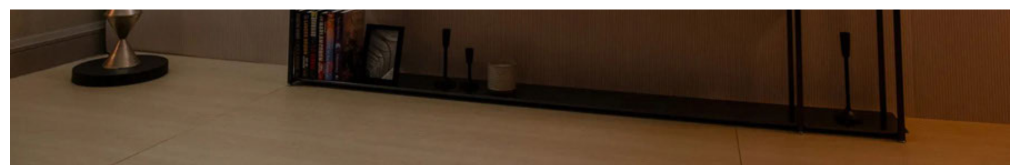
The first major trade show I attended was the Summer Consumer Electronics Show some 30 years ago, back when it was held in Chicago. There I saw the prototypes for HDTV and widescreen TVs, and more interesting, the first foldable screens.

I have to admit, nothing quite caught their attention more than the images of the devices that were common when I was their age. Seeing their faces as I showed the old floor TV models as large as a desk and the computer terminals the size of small ovens I grew up with was amusing. But it also reinforced the point that, as 13- and 14-year-olds, at least some of them are a scant eight years away from graduating college and facing the possibility of dreaming up and making the next round of electronics.

A Magnavox floor model similar to the one I grew up with. Fancy!

We are reminded, of course, that it takes a generation or more for most ideas to become mainstream. But fast forward to this year's CES, and among other innovations there were transparent TVs (thanks to LG and Samsung), foldable OLED PC monitors (Asus), and a portable rolling robot projector (Samsung again) that, well, you really have to see to understand what it is capable of.





Samsung's "transparent" TV, introduced this year.

Who but avid video game players would think of these things?

Of my cohort that January morning, two of them are already thinking in terms of engineering careers, but in my opinion what's more important is that none of them rules out this path. I took care to point out the many different ways there are to get here, and how many opportunities there are, regardless of one's particular skill set or interests. In other words, a lifetime in technology doesn't have to start with mad math skills.

Mentoring peers is great and important, but I'm a big proponent of talking to youth and helping them connect the dots. As the saying goes, if you want to see the future, take a look at your kids.

And if you agree that we need the next generation to consider careers in electronics design and manufacturing, are you doing what you can to encourage them?

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P.S. Our condolences to the many friends and family of Michael Ford, who passed away Jan. 27. Michael was a former columnist for PCD&F/CIRCUITS ASSEMBLY, a regular speaker at our conferences, a trusted advisor and a fantastically warm person. We will miss him.

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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Synopsys to Acquire Ansys in $35B Deal

SUNNYVALE, CA – Synopsys and Ansys in January announced a definitive agreement under which Synopsys will acquire its fellow ECAD provider for $35 billion in stock and cash. The deal is expected to close in the first half of 2025.

Cadence Design Systems and Siemens also reportedly made bids for Ansys before Ansys agreed to the Synopsys sale, with Cadence kicking off the sales process after making an initial acquisition offer last fall, CNBC reported.

Ansys shareholders will own 16.5% of Synopsys following the merger, Synopsys CEO Sassine Ghazi said during a conference call after the announcement. The deal will be funded in part by $16 billion of new debt, plus $3 billion in cash.

Combining Synopsys' semiconductor EDA tools with Ansys' broad simulation and analysis portfolio will create a leader in silicon to systems design solutions, the companies said.

"The megatrends of AI, silicon proliferation and software-defined systems are requiring more compute performance and efficiency in the face of growing, systemic complexity," Ghazi said. "Bringing together Synopsys' industry-leading EDA solutions with Ansys' world-class simulation and analysis capabilities will enable us to deliver a holistic, powerful and seamlessly integrated silicon to systems approach to innovation to help maximize the capabilities of technology R&D teams across a broad range of industries. This is the logical next step for our successful, seven-year partnership with Ansys and I look forward to working closely with the talented Ansys team to realize the benefits of this combination for our customers, shareholders and employees."

"Since inception 37 years ago, Synopsys has been an innovation pioneer, central to world-

changing semiconductor advances in computation, networking, and mobility, and now enabling the new era of 'pervasive intelligence'," said Aart de Geus, executive chair and founder of Synopsys. "Joining forces with Ansys, a company we know well from our longstanding partnership, is the latest example of how Synopsys remains at the forefront. Our board and management team carefully evaluated our top strategic options to lead and win in this fast-growing new wave of electronics and system design. The technology-broadening team-up with Ansys is an ideal, value-enhancing step for our company, our shareholders, and the innovative customers we serve."

"For more than 50 years, Ansys has enabled customers to design, develop and deliver cutting-edge products that are limited only by imagination. By joining forces with Synopsys, we will amplify our joint efforts to drive new levels of customer innovation," said Ajei Gopal, president and CEO of Ansys. "This transformative combination brings together each company's highly complementary capabilities to meet the evolving needs of today's engineers and give them unprecedented insight into the performance of their products."

GreenSource Nabs $43M DoD Award for Fab Upgrades

WASHINGTON – The Department of Defense in late December announced an award of $46.2 million to GreenSource Fabrication to enhance existing production capabilities at a manufacturing facility of state-of-the-art IC substrate, high-density interconnect (HDI) and ultra-high-density interconnect (UHDI), and advanced packaging.

The grant was made as part of the recently signed Defense Production Act Investment (DPAI) Program.

"Reshoring advanced packaging and assembly are essential to increase semiconductor supply chain security," said Dr. Laura Taylor-Kale, Assistant Secretary of Defense for Industrial Base Policy. "Expanding domestic production capability for printed circuit boards and advanced packaging is necessary to avert a shortfall that would severely impair national defense capability."

The award will enable GreenSource to scale up engineering, tooling, and manufacturing operations to establish a dedicated facility for IC substrate fabrication for a high-mix, low-volume offering of advanced interconnect solutions. These domestic production capabilities for HDI, UHDI, IC substrates, and advanced packaging are critical enabling technologies for sixth-generation systems and applications, including for radar, electronic warfare, information processing, and communications.

Siemens Adds Thermal Digital Twin Technology

PLANO, TX – Siemens Digital Industries Software has announced a new approach for sharing accurate thermal models of IC packages.

The main advantages of the new technology are protecting intellectual property, enhancing supply chain collaboration and accuracy of models for steady state and transient thermal analysis to enhance design studies, the company said.

Introduced in the latest updates to Simcenter Flotherm software for electronics cooling simulation from the Siemens Xcelerator portfolio, the Embeddable Boundary Condition Independent Reduced Order Model (BCI-ROM) technology permits a semiconductor company to generate an accurate model that can be shared with its clients for use in downstream high-fidelity 3-D thermal analysis without exposing the IC's internal physical structure.

MediaTek, a fabless semiconductor company specializing in systems-on-chip (SoC) for mobile, home entertainment, connectivity and IoT products, uses Simcenter Flotherm to drive efficiency in its collaboration with customers.

"Embeddable BCI-ROM is a great way to share our thermal models with our customers. It has several key features: easy generation, confidentiality, low error rate, and suitability for steady-state and transient applications," said Jimmy Lin, technical manager, MediaTek.

Today's electronics often have heat dissipation challenges that need to be resolved during

design due to higher power density influenced by the miniaturization of semiconductor packages and electronic systems, trends for thin-form consumer products, or demanding processing requirements. As a result, the need for more detailed thermal models to help solve thermal management design tasks is growing. Increasingly, modern IC package architectures such as 2.5-D, 3-D IC, or chiplet-based designs have highly complex thermal management challenges that require 3-D thermal simulation both during their development and during integration of IC packages into electronics products.

"Given electronics supply chain pressures and the growing complexity of IC packages, barriers to collaboration and thermal analysis efficiency during design must be eliminated where possible to support competitive development," said Jean-Claude Ercolanelli, senior vice president, Simulation and Test Solutions, Siemens Digital Industries Software. "Our breakthrough new technology enables accurate thermal models to be shared securely within the electronics supply chain without exposing sensitive intellectual property, allowing all parties to resolve thermal issues faster and bring advanced products to market more quickly."

Cadence Acquires Invecas

SAN JOSE – Cadence Design Systems has announced the acquisition of Invecas, a provider of design engineering, embedded software and system-level solutions headquartered in Santa Clara, CA. Terms of the transaction were not disclosed. The acquisition is expected to be immaterial to Cadence's total revenue and earnings this year, the company said.

The acquisition brings a skilled engineering team centered in Hyderabad, led by Invecas CEO Dasaradha Gude, that has vast experience in delivering end-to-end system solutions with deep expertise in advanced nodes, mixed-signal, verification, embedded software, packaging and turnkey custom silicon production, Cadence said a release.

Invecas has served hundreds of customers across various verticals, including mobile, networking, hyperscaler and automotive, and in addition to Cadence's EDA solutions, the newly acquired company will also leverage and augment Cadence's IP portfolio to enable more comprehensive custom product solutions.

"With complexity and challenges increasing due to the proliferation of AI, 2.5-D/3-D and chiplet designs, customers need access to experienced teams that can assist with bringing designs from ideation to production," said Boyd Phelps, senior vice president and general manager, Silicon Solutions Group, Cadence. "With the acquisition of Invecas, Cadence is able to scale our system design engineering offerings to support customers in critical high-growth verticals who are faced with the need to aggressively increase performance while tackling ever-increasing system-level complexity."

"Generational trends are accelerating the increases in design complexity and driving a customer need for skilled engineering talent that can assist with system design," said Dasaradha Gude, CEO, Invecas. "We are excited to join the Cadence team and to enhance the solutions available to customers, utilizing our core expertise to accelerate customer silicon and system development efforts."

Simmtech Investing in Indian Semiconductor Fab

CHEONGJU, KOREA – South Korean PCB maker Simmtech has announced plans for a INR1,250 core ($151 million) investment in the Indian state of Gujarat to support Micron's semiconductor plant being built in the state.

Simmtech CEO Jeffery Chun made the announcement at the 2024 Vibrant Gujarat Global Summit.

"Through the support of central and state governments, we are ready to make an investment in Gujarat which will create thousands of jobs," he said.

Last year, Micron announced plans to set up a semiconductor assembly and test plant in Gujarat with a total investment of $2.8 billion.

Chun said the colocation investment with Micron mirrors a similar investment that the company previously made in China, and this investment will further India's goal to become a major player in the global semiconductor supply chain.

“We really look forward to further supporting our customers’ supply chain, both in India and globally,” he said. “And we will further enable India’s domestic players to be part of the global supply chain ecosystem.”

Simmtech ranked 21st on the 2023 NTI-100 list of the world’s largest PCB fabricators, with reported revenue of $1.3 billion in 2022.

Orbic Electronics to Move Manufacturing from China to US

HAUPPAUGE, NY – Orbic Electronics Manufacturing has announced the launch of its Project Patriot initiative, which will move its manufacturing operation from China to New York’s Suffolk County, bringing more than 1,000 new jobs to the area.

Orbic Electronics Manufacturing produces a range of connected devices, including smartphones, tablets and mobile hotspots.

“This initiative is a stride forward in our vision of a sustainable, job-creating future,” said Mike Narula, President and CEO, Orbic Electronics. “Project Patriot is set to be a very exciting time in our company’s history, and Suffolk County is the perfect location for the bulk of our work to advance the production of American-Made products and grow American manufacturing jobs. Having our products read ‘Made in America’ is a tremendous point of pride for us, and it will also allow our company to bolster the local economy, helping other vendors in Suffolk County succeed alongside us.”

Orbic received an incentive from the Suffolk County Industrial Development Agency to lease and renovate a 70,000 sq. ft. building, which sits on a five-acre lot in Hauppauge, as part of a $30.8 million investment. The investment into renovating the building and adding manufacturing technology is expected to achieve a mass production target of five million units per year and create more than 1,000 jobs in the next five years, the company said.

Amber Enterprises Acquires Majority Stake in Ascent Circuits, Signs MoU with Korea Circuits

GURGAON, INDIA – Indian EMS provider Amber Enterprises, through its subsidiary Iljin Electronics, has acquired a 60% stake in PCB maker Ascent Circuits for an undisclosed sum.

India-based Ascent Circuits' clients include the Indian Space Research Organisation (ISRO), Bharat Electronics (BEL) and Bharat Heavy Electricals (BHEL), as well as several domestic and global automotive, telecom, and consumer electronics companies.

Amber, under the newly acquired Ascent Circuits, also signed a memorandum of understanding with South Korea's Korea Circuit to boost its PCB portfolio.

"This association between Amber and Korea Circuit will envelop the entire portfolio of PCBs required for various applications in India's electronics manufacturing growth story i.e. HDI (high density interconnect), flex, semiconductor substrate, multilayer, double-sided, (and) single-sided," the company said.

The company said the agreement will permit Korea Circuit to gain a competitive advantage in the Indian market and help to grow its business, and will strengthen its electronics manufacturing portfolio by increasing its local value addition and backward integration into passive components of PCB assemblies.

Kontron Acquires Majority Stake in EMS Katek

LINZ, AUSTRIA – Kontron has agreed to acquire around 60% of the shares in Katek in a bid to expand its portfolio of green energy solutions and the aerospace segment.

The transaction, in which Kontron is acquiring 8,587,138 shares in Katek for a purchase price

of €15 ($16.30) per share from primary shareholder Primepulse, is expected to be completed by March pending regulatory review, Kontron said in a release.

Katek offers electronics manufacturing and products for solar energy and e-mobility. The company had revenue of more than €750 million ($815.2 million) in 2023, and has more than 3,200 employees in locations across Europe, Asia and North America.

The aim of the acquisition is to expand Kontron's portfolio with smart solutions for renewable energies and other industries, the company said, and to achieve this, Katek's products will be upgraded with Kontron's software expertise and IoT connectivity – enabling the products to become more secure, have firewall functionality, be able to connect to complex grids and be maintained remotely. The merger expands Kontron's "Software + Solutions" segment to include the future-oriented "GreenTec" division.

"With the acquisition of Katek SE, we are expanding our presence in the high-growth area of clean energy solutions in a targeted manner and also strengthening the Aerospace division at Kontron with the Katek subsidiary NexTek," said CEO Hannes Niederhauser. "The clean energy sector holds considerable potential for the future. Upgrading with Kontron software will increase gross margins by around 5% in the medium term, thereby increasing profitability at Katek as well."

Neways Acquires Microsystems Firm Sencio

SON, NETHERLANDS – Neways in January announced the acquisition of Sencio, a microsystems company based in Nijmegen, Netherlands, that specializes in advanced packaging for smart sensing and actuation applications.

The acquisition solidifies Neways' position in microelectronics technology, the company said in a release. Sencio will continue to operate under the brand Neways Advanced Microsystems and operate out of its current facilities in Nijmegen.

"Over the past years Neways has invested significantly in its technology position, that allows

us to act as innovation partner for the most demanding customers in the industry," said Hans Büthker, CEO, Neways. "Through the acquisition of Sencio we further strengthen our market position in microelectronics and are able to offer a broader suite of integrated services to both Neways' and Sencio's customers. We welcome the Sencio team and are looking forward to our joint journey forwards."

"I am excited to become part of the Neways team and continue offering our technology with a large part of the dedicated and specialized Sencio team," said Sencio CEO Oliver Maiwald. "Joining forces with Neways enables us to offer a complete suite of advanced microelectronics services to a broad set of customers that can benefit from advanced packaging for smart sensing and actuation applications."

Inission Announces Acquisition of AXXE

KARLSTAD, SWEDEN – Swedish EMS provider Inission has expanded its presence in southern Norway with the acquisition of AXXE. The companies signed an agreement for the sale on Jan. 17, and the deal closed on Jan. 31.

According to the agreement, Inission will pay NOK27 million ($2.6 million) for 50.1% of the shares in AXXE, which is five times the average EBITDA for 2021-23. Inission will further pay six times the average EBIDTA from 2024-26 for the remaining 49.9% of AXXE.

AXXE has a portfolio of customers in several different segments such as marine, communications and IoT and industrial, and has 46 employees located in Halden, Norway. In 2022, AXXE had sales of NOK138 million ($13.1 million) and EBITDA of NOK8 million ($759,000).

"We are extremely happy to see Inission expand in Norway through the acquisition of AXXE," said Erik Dragset, CEO, Inission. "The company is one of the best-known EMS companies in the country and we look forward to a strong collaboration. With Inission's and AXXE's combined capacity and industry knowledge, we can offer our customers both ground-breaking solutions and world-class customer service."

"As an EMS company in electronics manufacturing, we are one of the oldest and most experienced in our field," said AXXE CEO Øystein Back. "We have worked with the production and assembly of complex electronics together with many of our customers for more than 17 years. By combining our strengths with Inission, we can take care of our customers more efficiently, offer a wider range of services and develop our business in a completely new way. This ensures that we meet the growing needs of all sectors of the electronics industry."

LCY Group Signs $9.5M Deal with Nippon Denkai

TAIPEI – Taiwan's LCY Group has signed a business and capital alliance agreement with Nippon Denkai's US electrolytic copper foils subsidiary to offer a $9.5 million loan to support collaborations and share experiences in operations and expansions in the US.

In addition to the loan offered by LCY Group, the two companies have signed a license agreement under which LCY Technology will have access to Denkai's technology license. Under the agreement, LCY and Denkai will be able to complete and expand geographical customer portfolios and strengthen technological cooperation in rigid and flexible boards as well as high-functioning fields (high-frequency, high-density mounting, etc.), LCY said in a release.

The partnership aims to enhance the production flexibility of both parties in manufacturing high-end PCB copper foils, which are used in packaging substrates, 5G and advanced driver assistance systems (ADAS) applications in Taiwan, China and the global market. LCY said it believes that the combined technical expertise, product portfolio and rich customer experience of both sides will help Denkai Group accelerate the realization of its mid- to long-term goals, and the collaboration aims to maximize production and sales synergies through accelerated sales growth of specialized PCB copper foil.

Foxconn Establishes EV Production

Business in China

TAIPEI – Foxconn Technology Group has established an electric vehicle business in Zhengzhou, China, amid declining smartphone sales.

The new firm, Foxconn New Energy Automobile Industry Development, was founded in Zhengzhou – also home to Foxconn's 200,000-employee iPhone factory – with a registered capital of 500 million yuan ($70 million), according to public records. Its business covers car component manufacturing and development, motor production and NEV sales, among other areas.

Foxconn said the new venture belongs to Foxconn Innovation Industry Development Group and aims to sharpen the company's focus on the electric vehicle industry, according to the South China Morning Post.

Dixon Factory Searched by Indian Government

NOIDA, INDIA – Dixon Technologies has announced a search of one of its subsidiary's manufacturing facilities here by India's Directorate of Revenue Intelligence.

In a regulatory filing, Dixon said the DRI searched the factory regarding the classification of the raw material imported for manufacturing one of the products. The company said the search took place on Jan. 17, but did not specify the product or the raw materials that were searched.

Dixon said the search should not have a material impact on the company's operations, and it is cooperating with the investigation.

"The issues raised by the DRI are interpretational in nature and we stand committed to defend our interpretation using all recourse available to us. We have extended full cooperation to the DRI, including providing complete information in a timely manner," the

company said.

DSL Launches In-House Assembly Service

LETCHWORTH GARDEN CITY, UK – DSL – Electronic Manufacture has established an in-house PCB assembly service to bring design and manufacturing under the same roof.

The company, which has specialized in electronic design services during its history, said it first initiated the plans in the summer of 2023, after finding that the scarcity of components made it nearly impossible to produce PCB assemblies, and if they could be obtained, the costs were exorbitant.

"We found ourselves in a difficult position, trying to justify the significant price increases imposed by our outsourced manufacturing partners without any valid justifications ourselves," the company said in a release. "Moreover, we faced numerous manufacturing issues, including costly mistakes, especially considering the high prices of these components. Once again, DSL was left in a compromising position, disappointing our valued clients through no fault of our own. We reached a breaking point and decided that enough was enough."

After conducting research on the necessary equipment and manufacturers/models available, the company opted for a fully automated SMT assembly line, plus a 3-D automated optical inspection machine, and it revamped its entire production area by installing dedicated benches for through-hole assembly. Its production manager had also previously managed a contract electronics manufacturer in a past role, and with the support of its in-house design engineering team and the recruitment of skilled hand soldering technicians, DSL said it was well-prepared for the addition of assembly services.

The company said it will be fully equipped to launch its manufacturing capability by January.

Cicor Closes STS Defence Acquisition

BRONSCHHOFEN, SWITZERLAND – Cicor Group has successfully closed the acquisition of 100% of the shares of the UK-based STS Defence announced in October 2023.

With the acquisition, Cicor adds a specialist in the design, manufacture and assembly of equipment and systems, as well as the integration and maintenance throughout the equipment's life cycle. STS Defence employs around 150 people in the south of the UK and generated sales of GBP27.5 million ($35 million) in the fiscal year ended Jun. 30.

Cicor said it is committed to continue providing engineering support and manufacturing services from the existing STS Defence site under the current management team.

PCD&F

Altair welcomed **CADY** to the Altair Partner Alliance.

Aohong Electronics announced plans to raise up to RMB580 million ($81 million) for a production base project in Thailand.

Aspocomp announced the beginning of negotiations on possible temporary and permanent layoffs in Finland.

CML Micro acquired **MwT**, an MMIC and mmWave supplier based in California.

Excellon opened a new manufacturing facility in Paramount, CA.

Icape announced the completion of a €47 million ($51 million) financing package.

Jove PCB expects its new production facility in Thailand to open in June.

MacDermid Enthone Industrial Solutions announced the acquisition of **All-Star Chemical Company's** surface finishing and cleaning chemical solutions.

Nanya Technology announced a 15-month high revenue of NT$3.16 billion ($102 million) for December.

PCBPit is extending its specialized services in PCB prototype manufacturing, fabrication and assembly.

TTM Technologies donated $20,000 to the international humanitarian organization, Rise Against Hunger, through its TTM Chair of Community Service

Award.

Zhen Ding Technology held a groundbreaking ceremony for its $250 million production facility in Thailand.

CA

Alan Anderson Manufacturing invested £2 million ($2.5 million) in PCBA production equipment, including surface mount and conventional assembly, selective soldering, conformal coating and 3-D AOI and x-ray inspection.

Arch Systems announced a three-year strategic collaboration with **Jabil**.

Avalon Technologies is now a strategic manufacturing partner for India's **Center for Development of Advanced Computing.**

Blue M announced the shipment of a Low Oxygen Class A oven to the medical industry.

Cloud Network Technology, a subsidiary of **Foxconn**, will increase its investment in **Ingrasys Technology Mexico** by $10 million to expand its server assembly business in the country.

Creation Technologies opened a new 150,000 sq. ft. EMS facility in Newark, NY.

Critical Manufacturing was listed in the Deloitte "Technology Fast 50," which recognizes and profiles the fastest-growing public or private technology companies in a specific region.

Danutek opened a new facility in Timisoara, Romania.

East West Manufacturing will close its facility in Youngsville, NC, in March and lay off 107 workers.

Foxconn has injected Rs 461 crore ($55.3 million) into Foxconn Precision Engineering in Bengaluru and signed a Mandarin-language education project MOU with four tertiary institutions in India aimed to deepen industry-academia ties and incubate future talent.

Hanza is building a new 8,800 sq. m. factory section in Töcksfors, Sweden.

Horizon Sales will distribute **Aven's** optical inspection tools.

HyRel Technologies appointed **Horizon Sales** as its representative in the Midwest.

Jabil opened a new 1 million sq. ft. plant in Chihuahua, Mexico.

Koh Young Technology is expanding into the medical robot business.

Kübler High Tech Solutions named **SMarTsol Technologies** exclusive sales representative for Arcadia in Mexico.

LG is planning to bring some operations to West Virginia.

Plexus received notification that its Chinese subsidiary, **Plexus Xiamen,** will be removed from the Bureau of Industry and Security's Unverified List.

Redarc purchased a factory in Adelaide, Australia, to house staff spearheading its move into the defense and space sectors.

Renesas is acquiring **Transphorm** in a $339 million deal to leverage its GaN expertise in power electronics.

Scanfil signed a multi-year agreement to produce **BrainCool** systems and components.

Silicon Mountain purchased an RO1 cobot robotic arm.

SMTXtra named **Performance Technologies Group** its representative for the

region spanning from Virginia to Maine.

StenTech opened a new facility in Clearwater, FL, and expanded its parts division in the US and Canada.

Rocka Solutions announced a strategic partnership to distribute **Weller Tools'** equipment.

Swiss electronics manufacturer **Veratron** has entered the Romanian market.

Vitrox opened a new office and demo center in Texas.

Quectel Wireless Solutions announced a collaboration with **Syrma SGS Technology** to facilitate the manufacturing of modules in India.

Taliang Technology will be stepping up its presence in the chipmaking industry, which presently contributes 10% of the company's overall revenue.

Trueview is expanding its electronics manufacturing plant for interactive flat panel displays in India.

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  - Increased Throughput
  - Improved Reliability
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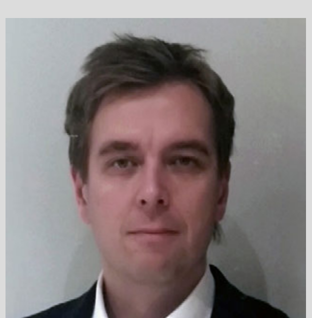
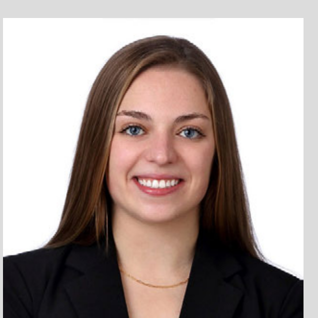
PCDF

Antti Ojala


Pekka Holopainen

Avi Avula


Katarina Roy

Amjad Obeidat

Aspocomp named **Antti Ojala** chief commercial officer and **Pekka Holopainen** chief operating officer.

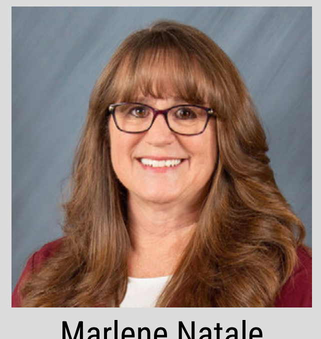
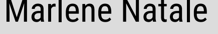
Methode Electronics appointed **Avi Avula** president and CEO.

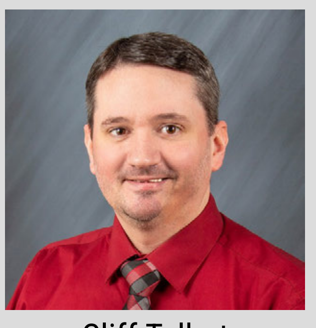
Summit Interconnect named **Alfred Macha** vice president and general manager, Santa Clara facility.

Uyemura hired **Katarina Roy** as technical service engineer.

Waymo named **Amjad Obeidat, Ph.D.** to head Sensing & Perception Systems Engineering.

CA



Marlene Natale

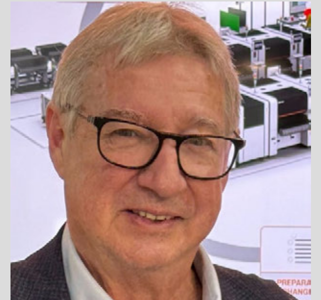

Cliff Talbot

Taylor Wang

Walter Wang

Brett Larsen

Patrick Prondzinski


Don Dennison

Ray Page

Lu Anne Green

Vince Libercci

Benjamin Smith

Dan-Mar named **Anthony Bellitto** senior quality systems manager.

Indium promoted **Marlene Natale** to senior manager corporate quality, **Cliff Talbot** to senior quality engineering technician, **Taylor Wang** to associate director, China sales, and **Walter Wang** to associate director, operations.

Keytronic appointed **Brett R. Larsen** to succeed **Craig D. Gates** as president and CEO, effective June 30.

Kimball Electronics promoted **Patrick Prondzinski** to vice president of new business development.

Kübler named **Don Dennison** of PIT Equipment Services sales representative for Arcadia in the Northeast US.

Libra Industries appointed **Ray Page** chief financial officer.

MicroCare appointed **Lu Anne Green** COO and **Vince Libercci** national sales manager.

SelecTech appointed **Benjamin Smith** sales director.

VJ Electronix named **Clint Buldrini** New England sales representative.

Support For Flex, Rigid Flex and Embedded Component Designs Now Available.

BluePrint-PCB®

CAM350®

DownStream's CAM350 and BluePrint-PCB support importation and visualization of PCB designs containing Flex, Rigid Flex or Embedded components. Visualize designs in both 2D and 3D, and easily document complex Flex or Rigid- Flex Stack-Ups for submission to PCB Fabricators.

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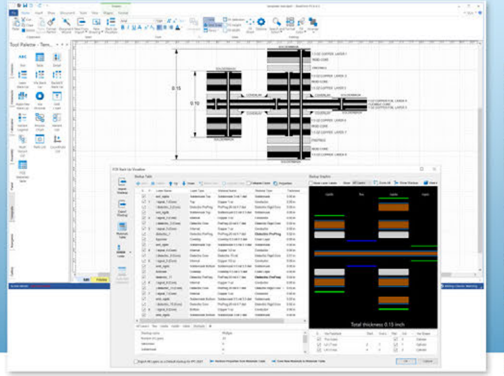
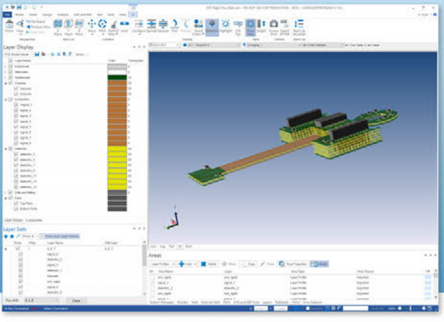
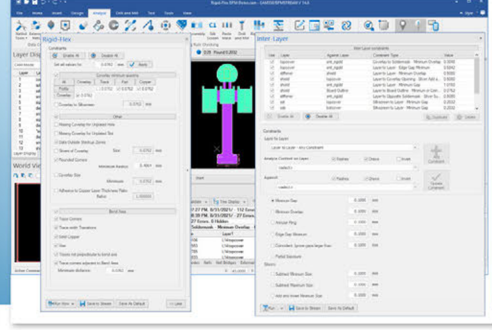
- **Manage Variable Stackup Zones for Rigid-Flex Designs**
- **Easily Create Custom Flex or Rigid-Flex Fabrication and Assembly Documentation**
- **Use DFM analysis to analyze a flex or rigid-flex design for potential fabrication or bend related defects**



Use Stack Up Visualizer and Blueprint's Rigid-Flex Stackup template to easily manage and document rigid-flex stackups.



A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



Use Rigid-Flex and Inter-layer DFM analysis to analyze flex and rigid-flex designs.

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PCB East 2024 Conference Registration Open

PEACHTREE CITY, GA – Registration for the technical program for PCB East 2024, featuring more than 75 hours of in-depth electronics engineering training, is now open.

Rick Hartley, Susy Webb, Tomas Chester and Zach Peterson are among the headliners of this year's conference. It will be held June 4-7 at the Boxboro Regency Hotel and Conference Center in Boxborough, MA. It features classes for every level of experience, from novice to expert.

The scope of classes ranges from basics on design engineering and circuit grounding, to DDR5 routing, impedance characterization, controlling noise and EMI, thermal management, board stackups and design for assembly.

More than half the presentations are new to the PCEA, including ones on SMT equipment validation, medical wearable device compliance, flex design, AI in electronics, and signal integrity/power integrity.

"Attendance more than doubled in 2023, showing both the vibrancy of the East coast electronics ecosystem and the need for topnotch technical training," said Mike Buetow, conference director, PCB East. "This year's event offers an array of experts in printed circuit

design engineering and manufacturing, and a new emphasis on assembly."

Registration is now open for both the technical conference and the exhibition at pcbeast.com.

Registrants who sign up by May 3 can take advantage of the Early Bird Special discounts for the conference.

The program was developed by the PCEA Conferences Task Group from more than 60 abstracts submitted. The task group is made up of nine industry veterans with more than 270 years of cumulative experience in the printed circuit industry, chaired by Troy Hopkins.

PCEA Announces Upcoming Webinar on IMS

PEACHTREE CITY, GA – Printed Circuit Engineering Association (PCEA) this month will hold a special member webinar on high-performance PCB materials for thermal management.

On Feb. 27, Chad Wood will deliver a one-hour talk on thermal IMS (insulated metal substrate). The term "IMS" refers to PCBs built on a metal (typically aluminum but also copper), which acts as a thermal substrate, while the dielectric adhesive (prepreg) provides high thermal transfer from the components while maintaining dielectric insulation. They can be used to replace direct bonded copper (DBC) substrates for power modules and devices.

The webinar takes place Feb. 27 at 1 p.m. EST. Register at https://attendee.gotowebinar.com/register/8917502632251720287.

Special Panel to Debate AI in Electronics

PEACHTREE CITY, GA – As use of artificial intelligence in electronics design and

manufacturing becomes a discussion point, it recalls a similar debate from 40 years ago on the impact of a new technology that promised to disrupt the industry norms of that era. On March 6, a special panel convened by PCEA will participate in a webinar where they consider the actual intelligence in these tools, and the ways – and how soon – they might impact the industry. (To register for the webinar, click here.)

Phil Marcoux, who is credited with installing the surface mount line in the US, will moderate the panel. He writes:

> I was blessed to be part of helping facilitate the acceptance of something called SMT, having co-founded and managed one of the first design and manufacturing companies devoted to SMT and trying to employ as much automation (and I guess early AI), as possible.
>
> Starting in 1982 industry sponsored panels (no webinars in that day!) comprised of several early adopters debated the need for collaborative data gathering to create the fundamental needs to successfully design and manufacture using the heretical idea of soldering components onto the surface of pcbs rather than in holes.
>
> Getting the experienced practitioners to share data was worse than pulling teeth. It wasn't until certain departments of the US government and two persuasive individuals in the IPC (Ray Pritchard and Dieter Bergman) coerced a gathering of 20 C-level executives that cooperation was needed. This led to the creation of The Surface Mount Council, of which I was a charter member and served for its entire 12 years.
>
> Handing off its duties in 2001 to a more international effort led by IPC, the Council published more than six white papers. The SMC has also participated in the SMART, SMI, IPC SMEMA Council's APEX and SMTAI technical conferences and initiated and sponsored joint standards for new technologies, including TR-001, "An Introduction to Tape Automated Bonding Fine Pitch Technology," J-STD-012, "Implementation of Flip Chip and Chip Scale Technology" and J-STD-013, "Implementation of Ball Grid Array & Other High Density Technology."
>
> Early in the SMC effort it was apparent that gaining industry wide acceptance depended on data sharing, particularly for design guidelines, especially land patterns,

metallization standards for components, and workmanship criteria. Without common knowledge of these the SMT effort would continue to flounder.

I think the same will happen with the effort to incorporate problem solving, process control, and early warning power, among other benefits, of the use of AI-assisted tools.

In addition to the challenge of creating adequate databases of information necessary for the intelligence in AI, we have the issue of how to communicate these data without compromising the data owner's needs. And just as with SMT, there's a large concern about the impact on jobs. If the history of SMT teaches us anything, it's that AI can help the industry create new and more productive jobs.

On March 6, one of the first gatherings of experts in AI for electronics will be held. Will this be the start of a new inflection point in the electronics industry, leading to the creation of many new products exceeding the marvels of those resulting from the use of SMT?

Attend and be a part of history.

PCEA CURRENT EVENTS CHAPTER NEWS

New England. The chapter plans a kickoff meeting on May 2, probably in the Andover (MA) area. Among the planned speakers are Gopu Achath of EMA Design Automation on supply chain-driven circuit design and Paul Yang of Jove PCB on embedded inductors. Contact Mike Buetow at mike@pcea.net for details.

Silicon Valley. The next chapter meeting is Feb. 14 from 11:30 to 1:30 PST. The meeting topic is Design Essentials to Maintain Signal Integrity, presented by Amit Bahl of Sierra Circuits. The meeting will be held both in-person at Sierra Circuits and online (Zoom). To attend in person, contact Bob McCreight for more information; bob.mccreight@outlook.com. To attend via Zoom, click here.

Meeting ID: 858 0414 0975
Passcode: PCEA

PCEA Training. Upcoming five-day training classes for printed circuit engineers, layout professionals, and other individuals currently serving in the design engineering industry or seeking to get into it will take place on the following dates:

- April 5, 12, 19, 26, and May 3
- June 14, 17, 21, 24, 28

These instructor-led classes are held online and cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

Registration fees include the 400-page handbook, *Printed Circuit Engineering Professional,* authored by Michael Creeden, Stephen Chavez, Rick Hartley, Susy Webb and Gary Ferrari. The course includes an optional certification exam recognized by PCEA.

For information about the instructors of the course and authors of the course material, visit pceatraining.net/instructors-authors.

For information about the course overview, class format, and materials to prepare in advance for the class, visit pceatraining.net/course-overview.

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PCB Design Tool Sales Set Record in Q3

MILPITAS, CA – Sales of design software for printed circuit boards and multichip modules rose 23.6% to $426.1 million in the third quarter 2023, the ESD Alliance announced in January.

The four-quarter moving average, which compares the most recent four quarters to the prior four, rose 14%.

Electronic design automation industry revenue rose to $4.7 billion, an increase of 25.2% from 2022, and the four-quarter moving average rose 13.8%.

"Electronic design automation (EDA) reported record revenue growth in Q3 23," said Walden C. Rhines, executive sponsor of the SEMI Electronic Design Market Data report. "This was the highest overall growth since Q4 1998. The computer-aided engineering, IC physical design and verification, printed circuit board and multichip module, and semiconductor intellectual property categories reported double-digit growth. Further, all geographic regions reported substantial growth."

Q3 2023 PCB Design Software Revenue

	Americas	EMEA	Japan	APAC	Q3 '23	Q3 '22	% Growth
PCB/MCM software	171	85.4	40	129.7	426.1	334.7	23.6

In $ millions

The companies tracked in the EDMD report employed 59,737 people globally in the third quarter, a 10.6% jump over 2022 and up 1% sequentially.

By product category, CAE revenue increased 22.4% to $1.7 billion and the four-quarter moving average increased 16.7%. IC physical design and verification revenue surged 45.3% to $904.5 million, with the four-quarter moving average increasing 29%.

Semiconductor intellectual property (SIP) revenue increased 22.1% to $16 billion. The four-quarter SIP moving average rose 5.3%. Services revenue slipped 3.9% to $138.3 million, and the four-quarter Services moving average rose 6%.

By region, the Americas procured $1.98 billion of electronic system design products and services in Q3, a 22.8% jump. The four-quarter moving average for the Americas rose 11.2%. Europe, Middle East, and Africa (EMEA) came in at $551.1 million, up 21.5%. The four-quarter moving average for EMEA grew 13.4%. Japan's demand rose 30.5% to $309.3 million, with the four-quarter moving average rising 9.4%. And Asia Pacific procured $1.86 billion, up 28.1%, with the four-quarter moving average growing 17.8%.

OK Computer

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	SEP.	OCT.[r]	NOV.[p]	YTD
Computers and electronics products	0.7	0.1	0.7	1.9
Computers	-2.9	5.0	4.8	13.1
Storage devices	-2.1	1.0	-1.0	13.3
Other peripheral equipment	3.4	-5.2	2.6	22.9
Nondefense communications equipment	1.5	-1.0	0.5	-1.8
Defense communications equipment	-1.5	4.0	-2.4	2.8
A/V equipment	-12.7	-7.8	0.2	16.4
Components[1]	2.8	-2.5	1.7	2.4
Nondefense search and navigation equipment	1.2	0.0	0.6	1.2
Defense search and navigation equipment	0.2	1.1	1.6	4.5
Electromedical, measurement and control	0.0	2.3	-0.2	1.2

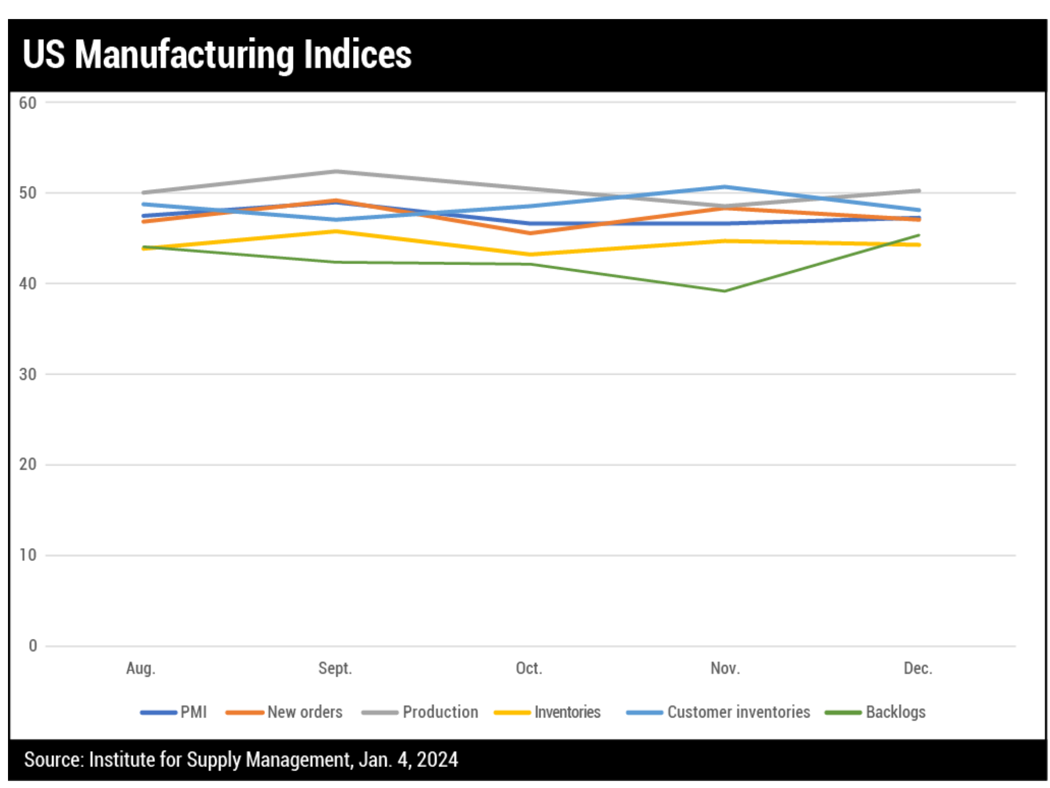
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Jan. 5, 2024

Key Components

	AUG.	SEP.	OCT.	NOV.	DEC.
EMS book-to-bill[1,3]	1.27	1.27	1.23	1.22	1.20

Semiconductors[2,3]	-6.8%	-4.5%	-0.7%	5.3%	TBA
PCB book-to-bill[1,3]	1.00	1.01	0.97	0.97	0.90
Component sales sentiment[4]	90.3%	86.7%	88.8%	83.3%	83.3%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA



Hot Takes

Worldwide **semiconductor revenue** in 2023 totaled $533 billion, a decrease of 11.1% from 2022. (Gartner)

Global **smartphone shipments** declined 3.2% year over year to 1.17 billion units in 2023. (IDC)

North American **electronics manufacturing services shipments** in December rose 1.3% over last year and 6.2% sequentially. Bookings fell 7% year-over-year and increased 2.3% sequentially. (IPC)

Worldwide **IT spending** is expected to rise 6.8% year-over-year to $5 trillion in 2024. (Gartner)

The downswing of **DRAM contract prices,** which had lasted for eight consecutive quarters since Q4 2021, reversed in the December quarter. (TrendForce)

A reduction in input tariffs could increase **India's smartphone exports** to $39 billion by 2027 from $11 billion in 2023. (India Cellular and Electronics Association)

Global investments in **space startups** jumped 31% sequentially in the fourth quarter. (Space Capital)

Despite facing a traditional low-demand season, buyers are continuing to increase their purchases of **NAND flash products** to establish safe inventory levels. (TrendForce)

North American **PCB shipments** fell 18.3% in December from a year ago. Bookings dropped 28.7% from 2022 and were down 14.1% compared to November. For the year, orders fell 10%. (IPC)

About 4,500 tech industry jobs have been lost so far in 2024, and tech job unemployment is 2.3%. (Layoffs.fyi, CompTIA)

The medium-term outlook is for **continued resilient expansion in the APAC** region, with robust domestic demand in many Asian emerging economies, supported by their global competitiveness in the electronics manufacturing supply chain. (S&P Global Market Intelligence)

Passive component manufacturers predict a market rebound after the second quarter and into the second half of this year. (DigiTimes)

Electronics industry sentiment took a dip in December with new order, shipment, and backlog indices falling, with only capacity utilization index holding steady. Despite the dip, overall demand sentiment remained in positive territory. (IPC)

Worldwide **PC shipments** plunged 14.8% year-over-year in 2023, totaling 241.8 million units. (Gartner)

Shipments of traditional PCs fell 2.7% to 67.1 million PCs in the fourth quarter. (IDC)

The French government is looking to create 18,000 **jobs in the electronics sector** in 2024. (France Ministry of the Economy, Finance and Industrial and Digital Sovereignty and the Ministry of Higher Education and Research)

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Striking a Balance

The tech industry – and world at large – could use some moderation.

MODERATION AND BALANCE seem in short supply throughout the world these days. Between war on two sides of the globe and political extremes in vogue all over, the proverbial pendulum is swinging wildly, rarely landing in the center. And business and industry are no exception to current trends.

In business and especially technology, the hot area is everything artificial intelligence (AI). Whether hardware or software, AI is the holy grail de jour. The regulatory environment is similarly out of balance. With security leaks, loss of privacy and potential pirating that could lead to everything from automobiles to aircraft and even weapons being manipulated by the "bad guys," layers of regulations, standards, audits and inspections have taken off in every segment of industry. Again, balance and moderation have given way to extremism.

In fact, industry has never needed balance and moderation more than now. "Reasonable" and "pragmatic" are two words that should be applied across a multitude of areas.

Technology could use a healthy dose of pragmatic balance. Take, for instance, the abandoning of gasoline vehicles for electric. Is recharging an electric vehicle's battery by plugging into an already overly taxed electric grid really the answer? Is it safer when a vehicle's controls reside on a touchscreen display out of the driver's typical line of vision rather than utilizing buttons and knobs closer to the hands on the wheel? And on a thousand-mile trip how many hours will be required to recharge the vehicle? Maybe a more balanced approach is to encourage small cars with energy efficient gasoline engines, hybrid vehicles and limiting the size/weight of energy inefficient SUVs to reduce owners' costs as well as be environmentally better.

Ditto the quest for AI. Maybe those efforts should instead be focused on improving individual education – especially with a STEM curriculum. Or focusing on a reasonable immigration policy so all those flocking to a country can be assimilated into the workforce to fill manufacturing jobs for which it is so difficult to find applicants. I would hate to think that the search of AI ends up finding artificial stupidity!

Security – especially cybersecurity – is another area requiring balance and pragmaticism. Adding protocols, two-factor authentication (2FA) and other "safeguards" only works if the likes of Microsoft, Apple, etc., better manage how and when they issue software updates to make sure they are both secure and compatible with the myriad of other software they interact with. Education is also needed so employees understand what they should and should not do when using a computer or a "secure" network! Finally, if the security protocol is not understandable and easy for non-IT employees to use, dangerous workarounds *will* occur. Security protocols are no place to deploy a Rube Goldberg approach.

Individuals, or more to the point, employees, is another area in need of balance, moderation and reasonableness. Young folks need to be taught that when they have a job, especially a career job in manufacturing, they need to show up on time every day. Not being in the "mood" isn't going to cut it. My guess is that all the people around the world trying to emigrate to a new country would be happy for any job where they must show up on time, all the time! Ditto thoroughness. Basic training in public schools should include "GAS" training, which is "Give A Sh*t!"

No matter the career or job pursued, if employees do not care, do not perform to the best of their abilities and do not strive for perfection, they will not be successful. If employers explicitly communicate to applicants the expectation that the applicant be reasonable in their requirements, balanced in how they interact with coworkers and pragmatic in how they approach the job, all will have a greater possibility for mutual success.

Expectations could also use a dose of balance. Setting goals is great. Expecting stretch goals to happen is something quite different. Thanks in part to social media, reasonable expectations are being inflated. More to the point, they are inflated either by those who know not of what they are saying or are trying to be misleading. Executives, management and employees alike

need to moderate and balance how much they believe on social media. Discerning fact from fake is becoming essential to survive in the workplace as well as in life.

In this new year, looking around at all the extremism taking place, it seems to me we need to recalibrate toward moderation, balance, reasonableness and pragmatism to truly enjoy success.

PETER BIGELOW is president of FTG Circuits Haverhill; (imipcb.com); pbigelow@imipcb.com. His column appears monthly.

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BOARD **BUYING**

2024 a Buyers' Market for PCBs

Capacity is about to peak, and demand has slackened.

PRINTED CIRCUIT BOARD buyers can capitalize this year on cost-saving opportunities if they're smart about it. Here are some factors to consider:

- Compared to a year ago, fluctuations in material pricing have settled.
- Worldwide semiconductor revenue declined by 11% and overall personal computer shipments fell almost 15% last year.
- Lead-times from Asia are relatively short compared to this time last year.
- PCBs manufactured in China and then imported into the US still face a 25% tariff. But the tariff exemption on two and four-layer rigid boards has been extended through the end of May 2024.
- Speaking of tariffs on boards made in China (as well as "Out of China" policies being adopted by some customers), new board houses are being built in India, Thailand, Vietnam and Malaysia to help offset those tariff costs and offer purchasers the option to buy elsewhere.
- Many companies in China are allowing employees to leave early to enjoy the Chinese New Year holiday because business there is down.

What does all this mean? Offshore capacity is, or very soon will be, at an all-time high, while demand is down. Pricing in these conditions becomes far more negotiable, and there are bargains to be struck.

And it's not just offshore board houses that are in the midst of a slowdown. Business at

domestic shops is not as robust, either.

This is the time to shop, PCB buyers. And the time to save.

Your company needs a solid board-buying strategy for 2024, or it will miss out on these cost-saving opportunities. Does your firm have one?

Here are some helpful hints to capitalize on 2024 spending:

Price checks. One way to do this is an activity I call "quoting for fun." Don't hesitate to give potential vendors a shot at quoting an ongoing project "for fun." Let potential vendors know it's an existing project and you'd like to see where they stand on pricing.

Also, let *all* your vendors know you will be testing the waters and comparing their pricing to others. A vendor that is too comfortable with your business may think twice about whether they could offer a better price when sending you that next quote. Be sure you follow through on checking out other vendors' prices. And don't be reluctant to bring on new vendors, if necessary.

While a few pennies per board difference in price is not worth switching vendors if you're happy with existing ones, it's wise to always keep your options open. This practice will also help keep your vendor base on its collective toes.

If you are happy with the delivery and quality of your vendor, that's great. Checking prices will still provide a useful benchmark. And if there *is* a significant per-board price difference, you can use your cost comparison as a negotiation tactic with the present vendor. Say something like: "Why is (XYZ company) 16% less than you, with all other things being equal? We are under pressure to reduce costs, and we are not necessarily asking you to meet or beat what was quoted. But how can we get closer?"

And just like that, you are likely to get a better price from a known quality vendor.

Vendor visits. Demand your vendors pay a visit to your operation. The more business they do with you, the more visits should be required. I can't tell you how much this helps in the

ongoing negotiation process. The more excited the vendor is about your operation, the better the service and pricing will be. If a vendor doesn't visit, this means they are too comfortable with your business, or they really don't want it. That may well mean you're paying too much.

Keep a scorecard. How often do you review the performance of your vendors? A vendor that is regularly evaluated for on-time delivery and quality acceptance in comparison to its competitors will generally also offer better pricing. Also, it is important that the pricing being compared is evaluated between like vendors. For example, pricing from one domestic PCB shop can be measured against another domestic house, and offshore pricing compared to another offshore manufacturer.

Pay on time. The one thing the vendor should never have to worry about is on-time payment. Consistent payment to vendors makes it easier for you to demand better service and pricing. There shouldn't be any excuse for a vendor to not jump through hoops for you.

I understand everyone is busy these days. But that ingrained habit of not looking outside the present cozy and comfortable PCB box is keeping many companies from saving money on bare boards, one of the most expensive items found on the bill of materials.

It's a core buyer responsibility to keep vendors competitive in pricing, and it is management's job to ensure buyers are not so overwhelmed with other responsibilities that they neglect that core duty.

This is a great time to look closely at what you're spending on PCBs and take advantage of the savings available in 2024.

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com) and can be reached at greg@directpcb.com.

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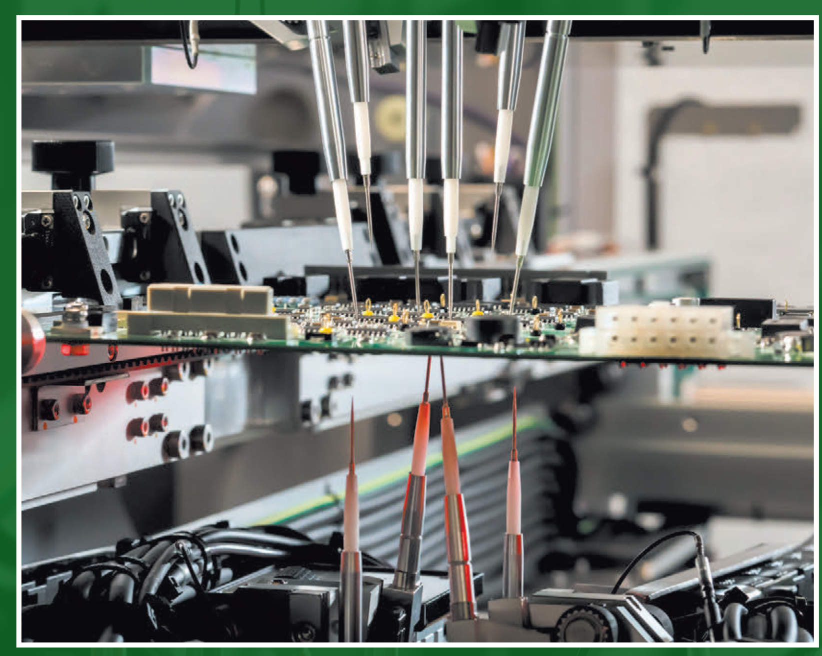

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FOCUS ON BUSINESS

Understanding Your Customers

A one-size-fits-all approach can lead clients to your competition.

RECENTLY I HAD an under-the-slab plumbing leak. I've been using a plumber who has deliberately kept his business small for over three decades. He is responsive, but complex jobs often take longer because he doesn't have all the tools the larger plumbing firms carry in their vans. He also doesn't have their overhead, so for most jobs he is more cost competitive. I called and he walked me through shutting off the water at the meter because he couldn't come until the next day. Part of my childhood was spent in Florida, so I applied my post-hurricane water management skills while I was without running water.

Sadly, when he arrived, he was unable to determine the source of the leak. Watching the meter spin, he mentioned it was a big one. He recommended a water leak detection firm. Its voice mailbox was full, however, and said it sometimes took a couple of days for them to return calls. My plumber reassured me he would come back after we found the leak. I got on the computer and found a water leak detection firm that operated 24/7. Fifteen minutes later they were at my house and 30 minutes after that we knew where the leak was. They were able to cut a hole in the wall and cut off the bad pipe so I could have water in the rest of the house. They couldn't fix the leak until the next day, and it would likely involve more demolition to reroute the pipe, so I had a decision to make.

Did I want to go with my reliable plumber who didn't have the same time-sensitivity or power tools as the team specializing in plumbing leaks, or did I want to pay the larger firm roughly double what my plumber would likely charge? I opted for the faster, more expensive operation. It was a good choice because they had to remove a tile I couldn't replace and cut through an exterior brick wall to do the repair. Their tools did the job in a way that was easy

to repair, and they installed an access panel in the brick wall, plus closed up all the wall and tub surround holes before they left. My regular plumber would have gotten the pipe reroute done, but the demolition and subsequent repair would not have been nearly as elegant.

I often draw parallels between electronics manufacturing services (EMS) providers and some of my business transactions, and this example has a clear EMS parallel. Many OEMs choose job shops or regional manufacturers for the convenience they represent and their ability to handle projects that don't fit well in larger EMS companies. Their lower overheads often translate to lower pricing, and the industry has evolved to a point where there isn't much difference in core capabilities among different tiers. In most cases, choosing a job shop or a regional EMS provider for product volumes that don't run well in a larger EMS provider is the best business decision. That said, when a smaller EMS company loses a customer, it is often over reasons like this plumbing example. Something was keeping the customer up at night that changed the dynamics of the relationship, and the EMS provider didn't recognize that the problem required a different approach. Or the way a project challenge was handled convinced the customer that more complex projects should go elsewhere.

Two lessons are to be learned from this. First, smaller EMS providers must be sensitive to customers' sense of urgency because ignoring an urgent issue can open the door to comparison with competitors with a broader range of services and a dual-sourcing strategy. Defining the response based on the criticality of the problem rather than taking a one-size-fits-all approach can help minimize this risk. Just as you would do an FMEA on product design, consider doing FMEA on key customer relationships. What situations should drive a different approach? How will you resource that? Having this game plan in place is particularly important when the issue involves a new project that could be sourced elsewhere.

The second lesson is for OEMs. Most relationships with smaller EMS providers have a convenience factor. There can be more flexibility, faster fixes on short notice and usually better prices for projects that have a lot of changeovers. If an unusual situation isn't handled well by a long-term source that has been reliable most of the time, switching suppliers may not be the best decision. A candid conversation about why a specific issue needs to be handled differently may be a better solution. If lack of responsiveness has been a trend driven by lack of resources, however, reevaluation of sourcing options may be the best choice.

I'm not replacing my plumber with a larger firm. I am now recognizing, however, that I am better served by a second source for complex projects, even if it costs more. In the EMS parallel, that customer mindset creates an account vulnerability.

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services.* She can be reached at smucha@powell-muchaconsulting.com.

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What is Wafer-Level Chip-Scale Packaging?

Should the ground connections share vias?

JUST LIKE IT says "on the tin," wafer-level chip-scale packaging (WLCSP) is a technology that shrinks the substrate down to a size quite close to that of the actual silicon, gallium arsenide or whatever material makes up the die. Rather than calling it a substrate, the WLCSP material is known as a redistribution layer, or RDL for short. It's a subtle but important distinction.

By definition, WLCSP devices exclude wire bonding, leaving flip-chip technology as the method of die attach. That means that there is no die cavity where a solid ground plane on the bottom of the die would normally act as the mating surface. Instead, the chip is mounted face down with BGA-style balls on a pitch that is typically less than 0.5mm. Right there, the challenge can be to maintain a good thermal path through the tiny connections **(Figure 1)**.

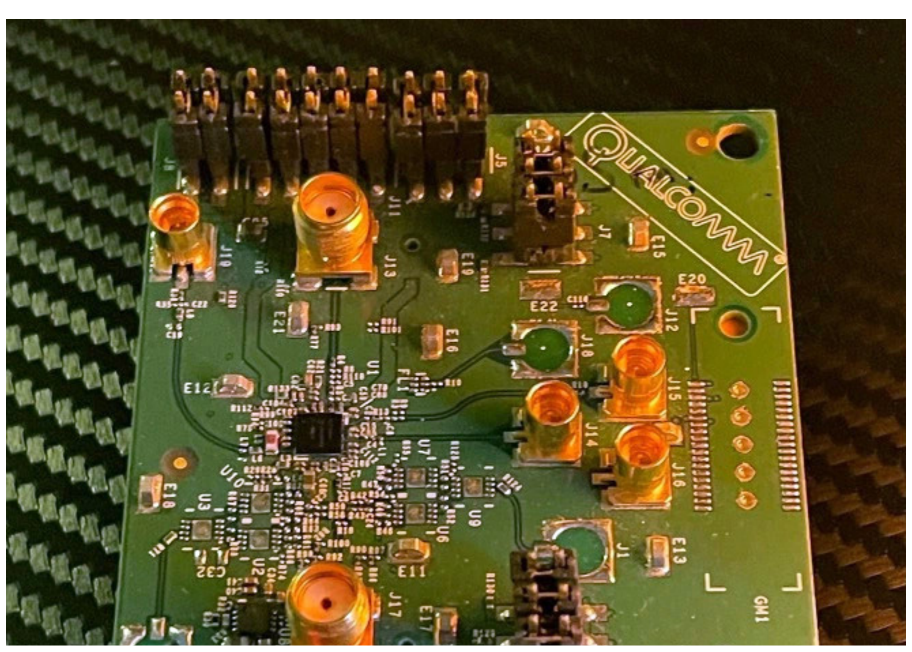

Figure 1. One of many iterations of a test board for a WiFi/Bluetooth/FM combo device in a wafer-level chip-scale package (Source: Author).

The solution is to have numerous ground balls to help dissipate thermal energy. The ground balls can be distributed around the device or gathered into a central square or rectangle, maybe both. Either way, it's best if every one of the ground connections gets a dedicated via rather than combining them to share a via.

Chip-on-board vs. WLCSP. This is the main operational difference between chip-on-board (COB) and WLCSP technology. When it comes to COB, you can mount either type of die on the PCB and then create the wirebond cage as required before potting the device within an encapsulant known as a glob-top.

Handling bare die is tricky. The coefficient of thermal expansion (CTE) of the chip is going to be different from the CTE of the printed circuit board. The encapsulant spreads out from the chip and holds the board in place against the local effects of thermal expansion.

So, while the bare die is marginally smaller than the WLCSP, the glob-top generally must expand well beyond the limits of the chip. That means that the COB solution ends up taking up more space that results in a circular keep-out around the die. The fragility of the bare die makes shipping and handling more likely to cause a defect at some point.

That's where the packaging helps. It protects the chip in transit and acts as an interposer to help prevent latent failure over the lifecycle of the product. COB may be used to "skip the line" when it comes to product development and the WLCSP would be cut in for the production cycle. As simple as they are, the packaging costs money and takes time to procure.

The slight increase in size from the die itself is to allow tolerance for the cap that goes over the substrate. Coming at this from a phone chip company, the difference between the size of the die and the final package is about 20% increase per side.

Why not just use a normal BGA package? Traditional BGA packages, whether flip-chip or wirebond style, are considerably larger. For one thing, a BGA or PGA can have more than one piece of silicon to create a multichip module. Further, the wirebond cage or flipped die is only the beginning.

From there, a traditional substrate has actual routing that spreads out the pitch of the pins to something that enables plated through-hole vias. This is still considered a leg up when it comes to high reliability for harsh environments such as those found in the automotive or aerospace industries.

On the other hand, the WLCSP package passes the signals more or less straight through from the die pads to the bottom of the device **(Figure 2)**. The term "redistribution layer" implies that the bumps on the die will not necessarily align with the package. The fact that smaller is better in terms of signal integrity and power consumption make this a compelling choice for both the marketing team and the SI/PI engineers.

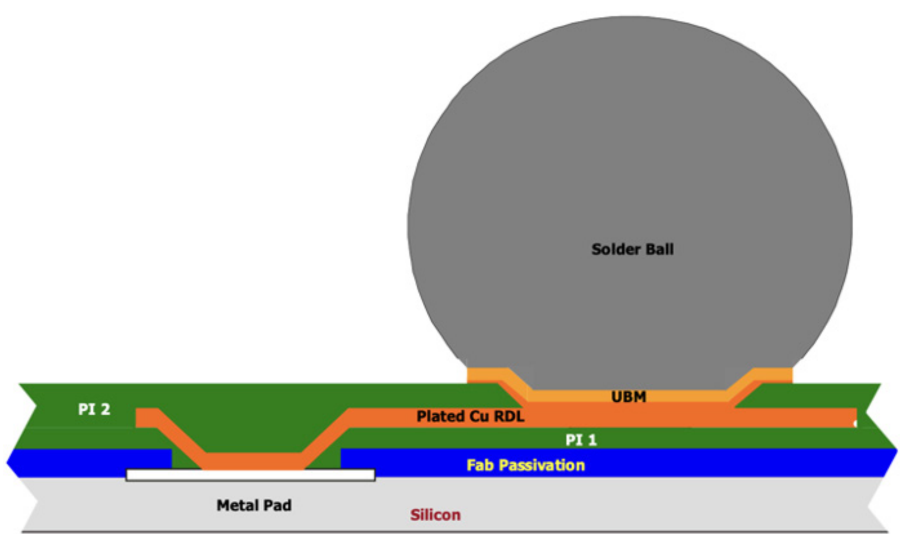

Figure 2. A cross-section of a WLCSP device showing polyimide in green and an optional under-bump-metalization layer (Source: Renesas).

Chip companies that want their devices in mobile applications as well as challenging environments often package the same chip in WLCSP, BGA and QFN packages to make them viable for every possible market. Once you have a working die, the development costs for the different applications are pretty reasonable in comparison.

This idea started way back when the only parts available were through-hole DIP packages using TTL or CMOS technology. They're still around. You can buy a hex inverter in a DIP-14 package that is either plastic or ceramic depending on the temperature requirements. It makes little difference to the PCB designer.

Fanout and routing of a WLCSP. This is where the fun starts. The job of spreading out the high circuit density of the device now falls on the layout person. Microvias are essential for anything with nine or more pins. There are plenty of four-pin devices with a 0.4mm pitch. The old-school PCB technology can still be used for regulators and sensors found in those miniscule packages.

As pin-count increases, so does the layer count required to get the job done. Approaching 100 or more contacts puts us on full HDI boards with stacked microvias throughout the board. You only need one such device to drive the PCB cost and lead time to that level. Precise placement requirements call for a pick-and-place machine rather than a hands-on approach.

Each year, it seems to get harder to find CODECs and WiFi modules or other popular circuits in the larger package types. Those chip foundries only have so much bandwidth, so they need to know that there is a demand for something before they try to fill the niche. The wafer-level chip-scale package is often first out of the chute, even if the others are on the roadmap. Plan accordingly and think small, my friends.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

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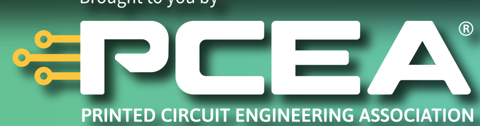

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DESIGN **BEST PRACTICES**

Multi-Board Systems Design

Integrating multiple boards clears the way for higher efficiency and power.

IN THE REALM of electronics systems, the demand for higher performance, increased functionality and enhanced connectivity has led to the evolution of certain design methodologies. One such approach that has gained prominence in recent years is multi-board systems design. This PCB design best practice involves the integration of multiple interconnected circuit boards, which paves the way for more efficient and powerful electronic systems.

Multi-board systems design enables designers to optimize each board for specific tasks, resulting in enhanced overall system performance. By distributing functionalities across specialized boards, designers can focus on achieving the highest efficiency for each subsystem. This specialization also allows use of different technologies and components tailored to the specific requirements of each board, ultimately leading to a more efficient and powerful system.

While the benefits of multi-board systems design are evident, increased reliance on interconnectivity introduces new challenges. The design of reliable and high-speed interconnections between boards becomes critical. Signal integrity, power distribution, and thermal management must be carefully considered to ensure seamless communication and prevent performance bottlenecks. Advanced technologies such as high-speed serial links, differential signaling, and impedance matching play a crucial role in addressing these challenges.

Efficient communication between boards is essential for the success of multi-board systems design. Various communication protocols, such as PCIe (peripheral component interconnect express), I2C (Inter-Integrated Circuit), SPI (serial peripheral interface) and others, are commonly employed to facilitate data exchange between boards. The choice of communication protocol depends on factors such as data transfer speed, distance between boards and the nature of the information being exchanged.

Today, we continue to see legacy methodologies where full system design is done in a vacuum and often by siloed teams. Systems designers today still largely use desktop drawing programs, spreadsheet editors and document editors. The processes still in use today depend on manual efforts, so the potential for human mistakes increases significantly. The lack of an integrated solution has become the elephant in the room.

A lot of complexity is at the hardware system design level. Current methods for managing this complexity have run into limitations in both capacity and process; there isn't enough time to manually define and manage today's complex product designs. The result is current methods of systems design are taking too long, introduce too many errors from manually handling data and require redundantly entering the same data at multiple points in the design process.

The result of the current methodology has been to insert unnecessary costs, in both time and money, into new product design. Errors cost time, money and result in lost opportunity. Failure to maintain the integrity of even a single interconnection could result in delay, thousands of dollars to resolve and perhaps even an expensive product recall.

The solution to addressing today's complexity at the hardware system design level is multi-board systems design. A multi-board systems design flow is a fully parallel collaborative design environment where global teams can work on the same design in real time. Systems where multiple boards are interconnected can be created and managed, starting with the logical representation of the design all the way to the physical implementation and layout, including net line connectivity showing between boards and 3-D. It supports cable connectivity, definition and optimization, and CAD integration and management through two BoM and manufacturing drawings. It is a single integrated environment that enables

multiple board system design including logical design, partitioning and connector and wiring management. Your entire hardware design from multi-board electronic system specification to completed PCBs and cables can be handled within one integrated flow.

Multi-board systems design goes beyond traditional single-board designs by distributing the functionality across multiple interconnected boards. Each board within the system is responsible for specific functions or subsystems, and they communicate seamlessly to achieve the overall system objectives. This distributed architecture enables a more modular and scalable design, offering numerous benefits in terms of performance, flexibility and ease of maintenance.

Today's multi-board systems design methodology offers modularity and scalability by taking advantage of model-based systems engineering for cross system optimization regarding size and performance. This approach removes siloed engineering teams. The value you would get from this best practice would be system-level integration and analysis, a digital twin, tightly integrated collaboration and cross-system optimization that removes potential for errors and reduces reschedules, respins and cost. One of the key advantages of multi-board systems design is its inherent modularity. Breaking down a complex system into smaller, manageable boards allows easier testing, troubleshooting and upgrades. Each board can be designed and optimized independently, simplifying the development process and reducing time-to-market. Moreover, this modularity facilitates scalability, as additional boards can be added to enhance system capabilities without requiring a complete redesign.

Multi-board systems design represents a significant leap forward in electronic systems development. By embracing modularity, scalability and specialization, this design paradigm addresses the growing demands for performance, functionality and connectivity in various industries. Having a single integrated environment that enables multi-board systems design, including logical design, partitioning and connector and wiring management, is key to success. This ensures that the entire hardware design, from multi-board system specification to completed PCBs and cables, can be handled with one integrated flow. While challenges related to interconnectivity must be carefully navigated, the advantages of this approach are evident in its widespread adoption across diverse applications. As technology continues to evolve, multi-board systems design is poised to play a pivotal role in shaping the future of

STEPHEN CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience and integrating the design-to-source Intelligence insights from Supplyframe into design for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com.

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Racing into Space

Durability in the heavens can lead to sustainability on Earth.

WE ARE INCREASINGLY reliant on satellite-borne services, as evidenced by the huge increase in launches in the past few years. The United Nations Office for Outer Space Affairs (UNOOSA) has recorded over 5,500 launches between 2020 and 2022 in its Register of Objects Launched into Outer Space. This contrasts with typically 100 to 200 per year from the early 1960s until 2016.

The vast majority of satellites in operation today support communication applications such as Internet services. Of the 6,718 operational satellites at the start of 2023, 4,823 are communication satellites. While their number has increased more than 50% since 2022, there are also over 1,200 Earth observation satellites, up by more than 13%. Others are used for technical development, navigation and positioning, and space observation.

We need the services these space vehicles provide. The Starlink constellation, delivering high-speed Internet services, operates in a low earth orbit at an altitude of about 550km. It can boast much lower latency than typical Internet satellites in higher, geostationary orbits needed to support streaming services and video calls. This enables high-quality services to reach areas where installing ground-based Internet infrastructure is not cost-effective or practicable.

Highly accurate position, navigation, and timing (PNT) data from GNSS constellations are, of course, another valuable service provided from space. Potential benefits are many, including improvements in oceanography that can protect the marine environment, precision farming for more efficient food production and better supply chain management resulting in lower emissions and accurate tracking of goods in transit to reduce losses. A recent study calculated

that drivers in the US alone have traveled more than 1 trillion fewer miles between 2007 and 2017 thanks to the effects of satellite navigation, saving billions of gallons of fuel and the associated emissions.

Space is arguably the most demanding environment for high-reliability systems. Whereas automotive or military systems can have redundant circuitry, the size and weight constraints for launching often mean there is no such luxury for satellites. With little or no opportunity to make any physical repairs, however, each unit must operate without maintenance its entire lifetime. This could be up to 15 years, although smaller, lower-cost satellites can allow shorter lives. Satellites also need to be controllable beyond their operational lifetime to permit deorbiting and responsible disposal, avoiding the accumulation of space junk.

As far as commercialization of space is concerned, increased reliability is critical to ensure services can be affordable as well as environmentally sustainable. In general, improving the reliability of electronics systems demands action on design, materials and processes. Where PCB manufacturing is concerned, pressure from the space industry, and the European Space Agency (ESA) in particular, has driven development of IPC-4101E Appendix A on contamination in substrate base materials. This provides supplemental inspection requirements for base materials used in high-reliability PCBs for critical applications, with particular reference to the prevention and detection of foreign material inclusions (FOD) early in the supply chain, effectively ensuring insulation performance comes within a narrower window than needed for typical terrestrial electronics applications. The support of the industry's leading materials suppliers, including Ventec, helped ensure adoption of ESA's proposals. Most materials suppliers have been obliged to improve their processes and invest significantly in automation and measures to mitigate contamination and be able to deliver materials that meet the higher specification. It's important for buyers to specify Appendix A when purchasing materials for space applications.

Of course, many more aspects go into designing and building reliable systems to operate reliably in space. Stresses experienced due to vibrations during launching are among the greatest threats to the integrity of electronics assemblies. In addition, when deployed on-orbit, the absence of atmospheric pressure encourages outgassing if any compounds that can become volatilized are present within the substrate. These can then recondense on the

surface of the assembly and adversely affect insulation performance. Thermal cycling is another hazard as the satellite can experience extremely low temperatures when obscured from the sun, rising significantly above 100°C when exposed. With glass temperature (Tg) typically in the range of 200°-250°C, polyimide-based formulas have served the space industry well in this respect for many decades. As system performance demands continue to rise, future generations of these materials must improve on parameters such as dissipation factor (Df) to reduce signal-power losses at high frequencies.

Although mission-critical, enshrining reliability has arguably slowed the adoption of innovative technologies and techniques. The explosion in demand for satellite-based services, however, could accelerate the pace of adoption in the future. On the other hand, the industry rightly continues to evaluate new technologies carefully. Wide-bandgap semiconductors are one example. Gallium nitride (GaN) power transistors have already shown how much smaller, more lightweight, more efficient and cooler running power-conversion circuits can be in numerous applications here on Earth. Those benefits would be keenly felt in space by making future generations of satellites easier to package, launch, maneuver and operate.

Wide-bandgap devices are known to be inherently more radiation-hardened than silicon in some respects, such as total dose and threshold energy. They can be vulnerable to single-event effects (SEE) like single-event burnout and single-event gate rupture, however. Researchers continue to investigate the effects and approaches to mitigate the problems. The NASA Electronic Parts and Packaging working group has published several body of knowledge documents on the radiation capabilities and general performance of wide-bandgap semiconductors for use in space.

While the opportunities are exciting and services hosted from space can help improve quality of life and sustainability here on earth, we would do well to ensure responsible development using durable – not disposable – equipment. The PCB industry can take a major role in ensuring future generations of satellites deliver the required performance and longevity.

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Pivoting to PCB Design

New entrants into the PCB industry are bringing their own skills to the table.

TRANSFERABLE SKILLS ARE bringing in new designers to the PCB industry because there aren't clear paths into it from the outside. Looking around and speaking with attendees at PCB West 2023, a significant number either identified themselves as an electrical engineer or an engineer of some type.

As a quick aside, as someone who studied electrical engineering, a certain amount of pride comes in identifying oneself as an electrical engineer, because it is known as one of the more challenging disciplines. A growing number of engineering programs are also dedicated to focusing electrical engineers toward signal integrity and power integrity, like Dr. Eric Bogatin's program at the University of Colorado Boulder.

So, it wasn't entirely a surprise that at PCB West, roughly 18% of attendees identified themselves as an electrical engineer, up from previous years. Several of the designers that I spoke with indicated they were seeing increased time allocations from their management to focus on designing printed circuit boards, which is something I always chuckle about because my first inquiries into printed circuit board design was met with a quick rebuff.

I still have my electromagnetic fields book from university sitting near my desk, but the extent of its content dedicated to printed circuit board traces is about two pages at the very beginning, and I can still recall Smith charts and Laplace transforms, etc. But when it came time for my senior design project, I thought it would be appropriate to investigate connecting the multitude of microcontrollers, memory chips, sensors and motor drivers together on a printed circuit board rather than a mess of wires on multiple breadboards.

I found that my professors were highly unsupportive, with responses along the lines of: “You are an EE, you’re destined to be designing silicon, not printed circuit boards. You will have a technician do that for you, so you don’t need to learn about that.” To their credit, Intel has a significant presence near my university, and I did have a strong motivation to agree. I find it humorous, however, that seven years after graduating, I would be teaching colleagues with doctorates in electrical engineering how to design printed circuit board traces to achieve impedance matching and reduce insertion loss.

As I trained customers, I encountered more and more electrical engineers entering the field of printed circuit board design, but sometimes I would encounter math teachers and those from other backgrounds. (Yes, a former high school math teacher!) In many cases, it seemed that it was due to a workforce shortage and a combination that those who studied electrical engineering were the closest to fill in the workforce gap. After all, we (electrical engineers) already have a firm understanding of circuits and components. Often the electrical engineer is the one doing a lot of the work leading up to the PCB design step, so why not add the next steps in the design process to their workload? One designer even shared with me that he felt if he did the preliminary steps well, it was easier for him to do the PCB layout as he had solved many of the layout challenges in earlier stages rather than creating problems for someone else to solve later.

Transferable skills pulling electrical engineers deeper into the PCB design stage go beyond just understanding circuits, but also include a soft skill that is often overlooked or when mentioned, considered a bad word, especially by designers. And that bad word is actually two: Project management.

I know from experience that most engineers, not just electrical engineers, have also picked up a significant amount of project management skills, and they don’t even know it! Buried in a number of excellent sessions at PCB West was a strong undercurrent of project management. Many examples focused on communicating the design’s needs with suppliers, management and other stakeholders. One presenter was even addressing design techniques specifically to assist in communicating with assigned formal project managers. But none of the engineers was using the official project management terminology!

Formal project management has defined terms to communicate certain ideas that I often hear others who haven't studied it use synonyms and talk around a concept without realizing there are formalized terms. Many times, engineers hear such language and dismiss it as buzzwords, but understanding the language of management and formalized project management can help any designer in both self-management as well as in communicating with formal management.

If you would like to add to your repertoire of transferable skills, I highly recommend *Fundamentals of Project Management* by Joseph Heagney. It was a book recommended to me by John Watson of Altium and Palomar College, where he teaches courses on PCB design.

If you are likely already doing project management daily and are only somewhat aware of it, I behoove you to consider spending some time to learn the formal language of project management to be able to articulate and effectively communicate with others the state of your projects and what they need to succeed. I started applying them to even my home projects and my fellow stakeholders (read: family) approve.

Please share your ideas of other transferable skills that you think are important and we should be looking for in PCB designers. I can be reached at geoffrey@pcea.net.

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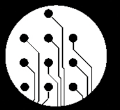

PRINTED CIRCUIT UNIVERSITY

THE FLEXPERTS

Aspect Ratio and Annular Ring

Coupling buried vias with microvias can solve many manufacturing challenges.

WHEN IT COMES to designs, we all make choices – material selections, feature sizes, via structures, components and more. Often, we also make tradeoffs.

Maybe the 0.8mm BGA you want allows standard vias, but the 0.5mm BGA takes up less space. Or you need impedance-controlled signals (which seems to be a requirement on almost all new designs), and line widths must be balanced with dielectric thickness and Dk values.

As packaging challenges mount, so does part thickness and layer count. For many designs, two of the biggest cost and risk drivers are aspect ratio and annular ring. These two attributes are often at odds with each other. There are ways to help them coexist.

Aspect ratio, or board thickness to drilled hole diameter, can be a limiting factor for a few different reasons. Keep in mind that there are **two** aspect ratios to consider. The first and most commonly thought of is the mechanically drilled through-hole. The second is the blind microvia.

The most common limitation is the ability to copper-plate the drilled hole. As the hole gets deeper, it gets harder for the copper plating bath to drive copper ions into the middle of the hole to provide adequate copper thickness in the hole. Not every manufacturer will have the same limits for aspect ratio. Depending on their product focus, they will have optimized their plating lines to support the products they build the most.

For through vias, aspect ratios can be higher because we can drive solution through the hole

and out the other side, providing a continuous supply of fresh solution and copper ions. For microvias, the aspect ratio is much lower because we are trying to plate a dead-end hole. It is more challenging to get solution to enter the hole, deposit copper and get out of the hole so new solution can take over.

Generally, if you can keep the through-hole aspect ratio below 10:1 (thickness to drill diameter) and the microvia ratio below 0.66:1, most suppliers can support your project. If you can't, however, what options do you have?

Starting with the microvias, the first suggestion is to reduce the dielectric thickness. Often the microvias will be 0.004″ (100µm) deep or less, so the dielectrics are quite thin. Sometimes there is a reason to go deeper, such as connecting to two layers down. If that is the case, the aspect ratio can rise quickly and risk manufacturability. The recommendation here is slow and steady wins the race. Rather than try to increase aspect ratio, consider a set of stacked or staggered microvias. This may mean an extra layer is needed to accomplish this. Most suppliers, however, will say they would rather make two shallow microvias than one deep one. An advantage here can be extra room to increase pad size and thus annular ring on at least two of the layers involved. An extra layer can aid with impedance or with extra plane for power distribution.

A lot of conversation is out there on microvia reliability. Some is fact, some is anecdotal. What is known for sure is that larger diameter microvias are more reliable than smaller ones, and that shallower aspect ratio is also better. Material selection and via offsets also have an impact. If you are pushing the envelope, invest the time to talk with your manufacturer to make the best choice you can.

For mechanically drilled vias, whether through-holes, blind or buried, there is a relationship in terms of drill diameter, aspect ratio and pad size. Most suppliers are comfortable with 0.008″ (200µm) diameter drills. Some will drill smaller – there are 100 and 150µm drill bits available. A couple of limitations come into play, however. As bit diameters get smaller, so does flute length. So there are limitations on how deep one can drill before running out of drill bit. Manufacturers have tricks to extend this, but they do reach limits.

Also, smaller diameter bits have a greater tendency to splay, meaning they don't go perfectly perpendicular through the board. This can cause annular ring issues on the bottom side of the board.

Finally, if the vias must be filled with epoxy, the smaller holes are a much bigger challenge to fill. Keep in mind a 200µm hole in a 2mm board is not 10:1 at the filling operation. After drilling, the hole is copper plated, reducing the diameter to something closer to 125-150µm, making the aspect ratio in the neighborhood of 13-16:1. This makes via filling much more difficult, as the manufacturer is trying to push a thick epoxy into a very narrow and deep hole. As a result, a supplier might permit a higher aspect ratio on one board, but not another, and the reason may be due to via filling requirements on one but not the other.

Interestingly, while layer count is certainly a factor when it comes to aspect ratio, it can often be offset by thinner dielectrics to limit aspect ratio. Manufacturers may prefer a thinner core and prepreg solution to help keep board thickness down. When impedance is involved, selection of lower Dk materials can help make this a possibility.

In addition, via structures or number of laminations are a big impact for being able to achieve annular ring. Use of buried vias can help distribute signals with smaller vias in thinner portions of the board. These smaller vias can include smaller pads, meaning much less real estate being consumed internally, and leaving more room on layers external to the buried vias for larger pads on through-holes.

Coupling buried vias with microvias can eliminate through vias altogether. On boards using a buried via coupled with just microvias, the through-hole is eliminated altogether, and most of the annular ring and aspect ratio challenges disappear.

This can be a great way to solve manufacturing challenges while achieving your design goals.

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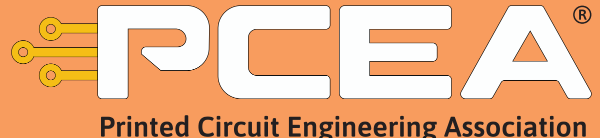

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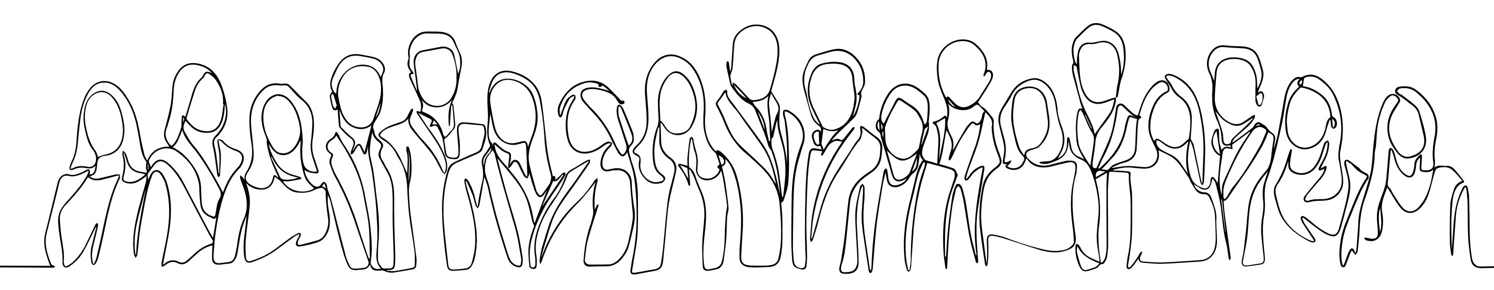

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CONDUCTIVITY

Do Trace Coatings or Via Fillings Improve (Thermal or Electrical) Conductivity?

Coating traces or filling vias is usually a wasted expense.

by DOUG BROOKS, PH.D. and DR. JOHANNES ADAM

We are often dismayed by the number of individuals (and especially board manufacturers) who suggest that coating a trace or filling a via cavity can result in significant thermal and/or electrical conductivity improvements. Herein we will try to explain why, in almost all cases, this is not true.

Individual trace coatings. Often users (especially board manufacturers) suggest trace thermal or electrical conductivity can be improved by coating the trace with some conducting material. It sort of makes intuitive sense that additional material can provide more benefit. Trace coatings are typically limited in a practical sense to plated copper or a solder coat. We suggest that such a coating can be analyzed by looking at the separate elements (bare trace and coating) as two parallel conductors.

An easy way to look at the effects of adding a coating is through simulation (Note 1). Consider a model of a copper trace (ρ = 1.8µΩ-cm) that consists of:

1. a 20 x 200mm board, 1.7mm thick, of typical FR-4 material
2. a 150mm long, 1.5mm wide copper trace, 0.037mm thick
3. with conducting cross-sectional area of 1.5*0.037 = 0.0555mm^2

We can calculate the expected resistance of this trace with the formula (remember electrical conductivity is the inverse of electrical resistivity):

$$R = \rho * L/A = (1.8 * 10^{2} * 150)/(0.0555\ ) = 0.0486 = 48{,}860\mu\Omega$$

Eq. 1

We ran three simulations of this model, and looked at the resistance of the trace and the temperature of the trace under each of the three conditions. The first simulation just looked at the individual bare copper trace. The second was with a plated copper coating with the same thickness as the trace. The third was with a solder coating with the same thickness as the trace. In each simulation we passed a current of 7A down the (combined) trace. The temperature and resistance results are tabulated in **Table 1**.

Table 1. Measured Temperature and Resistance

Model	Max trace Temp, °C	Measured Trace R (Ω)
Single trace	81.9	0.0489
With Copper coating	47.8	0.0243
With Solder coating	76.4	0.0441

Adding a copper coating to the underlying copper trace clearly helps. It is exactly like doubling the thickness of the trace itself. The resistance falls in half (within model error), and the trace temperature drops dramatically. But the solder coat offers little benefit **(Figure 1)**. That is because the resistivity of the solder (although it varies considerably by formulation) is approximately 10 times higher than that of the copper. Thus, approximately 90% of the current still flows through the copper layer, and there are relatively minor improvements to the temperature and the total resistance of the trace.

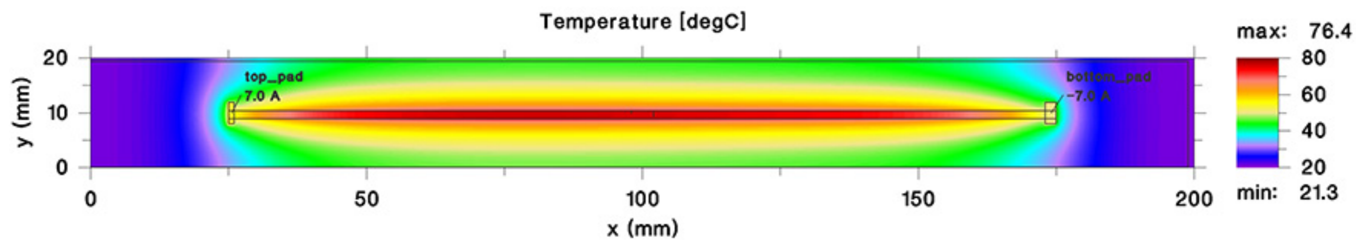


Figure 1. Thermal image of solder coated trace. The model images (other than temperature itself) show no visual evidence of whether the trace is coated or what coating is used.

Table 2 shows the current density (J, in A/mm^2) in the various coatings in the various models. The current splits equally between layers (within model error) in the copper coating case, and approximately 90:10 in the solder coating case. While we intuitively think of solder as a material that conducts heat and current well, when paired with a copper layer it actually contributes little additional benefit.

Table 2. Measured Current Densities (J, A/mm^2)

Model	J, Base	J, Coating	J, Total	Total Current, A = J Total *.0555 mm^2
Single Trace	126.9		126.9	7
With Copper Coating	63.3	63.14	126.4	7
With Solder Coating	115.35	11.5	126.4	7

So, coating a trace with the intent of improving electrical conductivity performance is going to offer little practical improvement unless the coating is another layer of copper.

Via filling, electrical. We simulated the electrical effects of a via with the same model as above. We split the trace at the center midpoint and put half of it on the top layer of the board and the other half on the bottom layer. We connected these trace segments with a via whose outer wall was 0.40mm in diameter (R_0 = 0.20mm) **(Figure 2)**. We plated its wall with 0.05mm-thick copper. That left the inner cavity with a radius (R_1) of 0.15mm. The inner cavity could be left unfilled, or we could fill it with a conductive material.

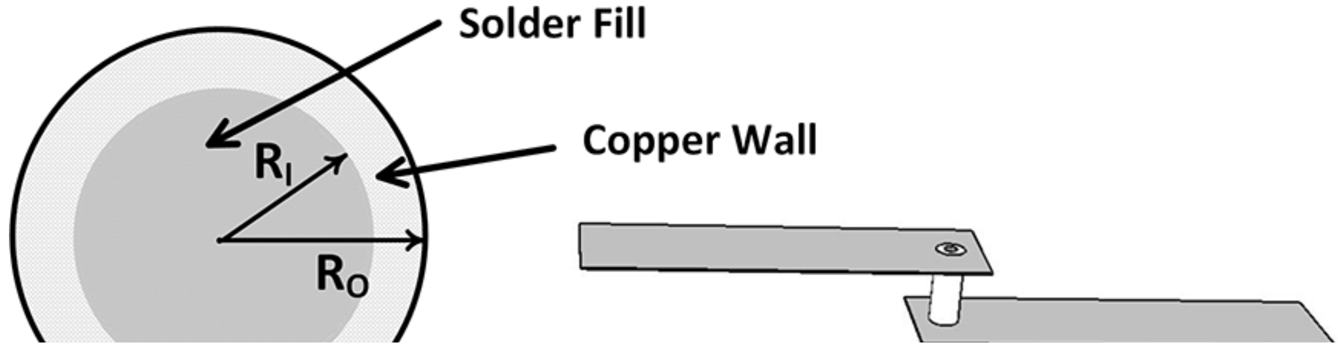


Figure 2. A via with an outer wall diameter of 0.40mm filled with solder.

The formulas for the relevant thickness and areas are:

Entire drilled area:	πR_0^2	$= 0.1257mm^2$
Inner core:	πR_1^2	$= 0.0707mm^2$
Conducting width	$R_0 - R_1$	$= 0.05mm$
Conducting area:	$\pi R_0^2 - \pi R_1^2$	$= 0.055mm^2$

You will note that this simulation has been intentionally constructed so that the conducting cross-sectional area of the via equals the conducting cross-sectional area of the trace. The length of the via is the thickness of the board, 1.7mm, so the resistance of the via is:

$$R = \rho * L/A = (1.8 * 10^2 * 1.7)/(0.0555\ ) = 551.35\mu\Omega$$

Eq. 2

This compares to the trace resistance of 48,860μΩ. In fact, the relationship between the trace resistance and the via resistance is even easier than that to compare: If the conducting cross-sectional area of the via and the trace are equal (or even nearly so), then the ratio of their resistances is:

$$R_{via}/R_{trace} = L_{via}/L_{trace}$$

Eq.3

In this case, that is 551.3/48860 = 1.7/150 or approximately 0.01 = 1.0%.

Now there are an infinite number of via/trace combinations. And filling the via with plated copper would lower its resistance further. But the bottom line is this: the resistance of a via is already so small compared to the parent trace that it is (almost) never advantageous, from a practical standpoint, to fill the via with anything to improve its electrical conductivity. Only in the cases of extremely short traces (say an inch or less) should the option even be considered.

Via filling, thermal. Some individuals and fabricators advocate filling the cylindrical core with a material designed to improve the conductivity of the thermal path. The cylindrical surface and its filling (if any) can be thought of as separate components and analyzed separately, their separate thermal conductivities being additive. The first step would be to calculate their respective volumes and then compare those volumes. But since the via length is the same (a constant) between them, the lengths cancel and it is only necessary to compare the relevant cross-sectional areas. Using the same via structure as above, the respective cross-sectional areas are:

Drilled area = $0.1257mm^2$

Copper via wall = $0.055mm^2$

Inner core = $0.0707mm^2$

The thermal conductivity of any component is given by:

$$\text{Thermal conductivity} = k*A / L$$

Eq. 4

where k = the thermal conductivity coefficient of the material. In the case of copper this is 0.350W/mmK (Watts per millimeter per degree Kelvin). So, the thermal conductivity of the outer wall = 0.350 * 0 .055 = 0.019W/unit length.

The next question is, with what do we fill the inner core? If we filled it with copper plating, there would be an obvious benefit. We can tell intuitively the plating would add more than

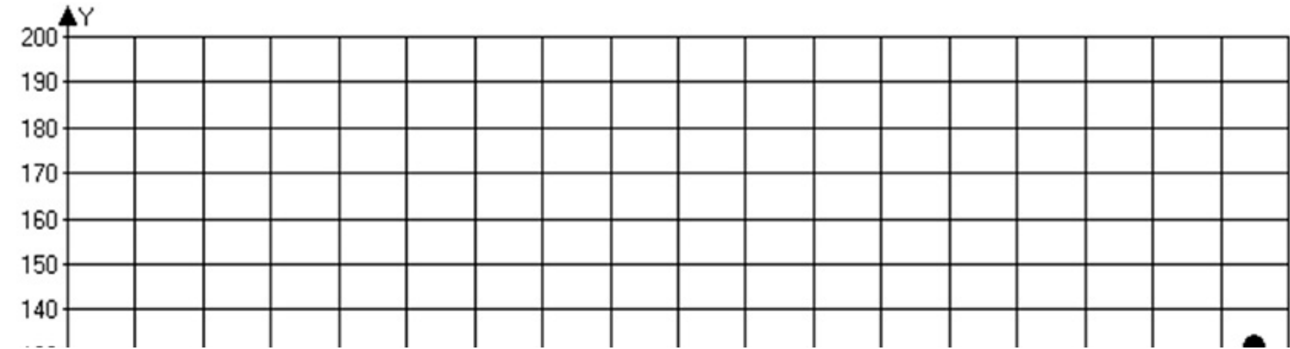
twice as much additional conducting copper to the structure, and the total conductivity would be 0.1257 * 0.350 = 0.044W/unit length. This would increase thermal conductivity by (0.044-0.019)/0.019, or about 132%.

Perhaps we could fill it with solder. The thermal conductivity of solder depends, of course, on the specific solder formulation. But a reasonable value for it might be around 0.060W/mmK (Note 2). This would result in the inner core having a thermal conductivity of 0.0707*0.06 = 0.0042W/unit length. Adding an inner core of solder would increase the thermal conductivity of the via structure by 0.0042/0.019, or just over 22%.

But what about other materials? Very few material candidates for via filling have thermal conductivity coefficients better than solder. Most available materials have thermal conductivity coefficients *much* lower than copper and solder. One board fabricator suggests, on its website calculator, materials with thermal conductivity coefficients in the range of 5 to 10W/mK, or 0.005 to 0.01W/mmK. **Table 3** summarizes the results using a sample of via filling alternatives. These results are graphed in **Figure 3**.

Table 3. Comparative Material k-Values

Material	k-value (W/mK)	Improvement over unfilled via (Approx. %)
Some epoxies	10	3.7
Solder (approx.)	60	22
Nanya NPG 170	75	28
Copper	350	132



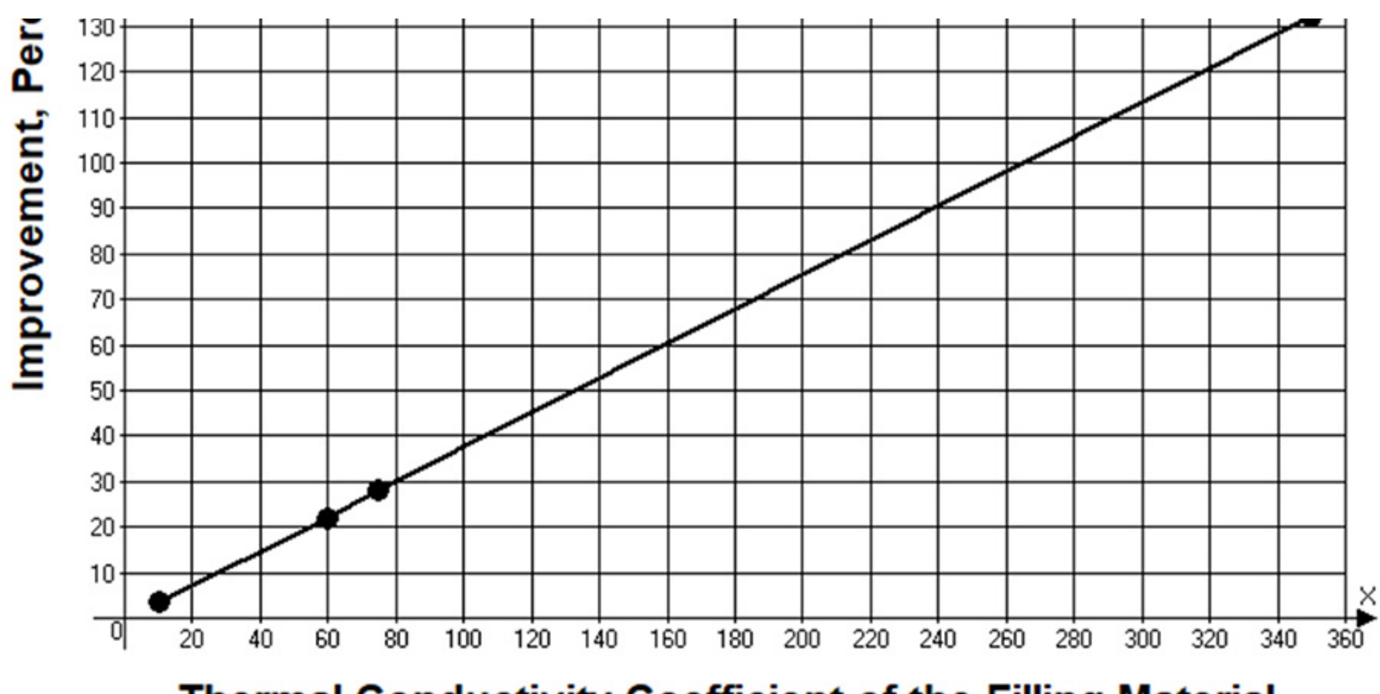


Figure 3. Impact of various via filling materials on effective thermal conductivity.

Filling a via makes a theoretical improvement, as shown in these data. But does it make a practical improvement? We modeled the trace with a via, using the same 7A current as before, and simulated three conditions: simple copper walled via, solder filled via cavity, and copper filled via cavity. The results are as shown in **Table 4**.

Table 4. Comparative Via Temperatures

Model	Trace Max T, °C	Via Mid T, °C
Simple Via	87.9	87.3
Solder Filled	85.3	84.5
Copper Filled	84	81.7

Filling the via, even with additional copper, helps reduce the trace temperature by only a small amount.

Via Conclusion

Filling a via with copper gives significant thermal conductivity improvement, and filling it

with solder gives some improvement. But using any other materials provides negligible improvement from the basic via structure itself.

But we question why anyone would go through the via filling step at all (for thermal conductivity reasons). If the purpose is to have improved thermal via structures for cooling heated pads, we have already shown that thermal vias are so inefficient at this task that they are next to worthless (Note 3). Watch for a future article that will explore this in even more depth.

Going through the via filler step (for thermal conductivity reasons) simply adds additional cost, perhaps misleads the customer in terms of added benefits, and provides benefits smaller than some calculational round-off errors!

NOTES

1. We used a simulation program called TRM (Thermal Risk Management), which was originally conceived and designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation. TRM is available at https://www.adam-research.com.
2. See Jim Wilson, "Thermal Conductivity of Solders," *Electronics Cooling,* Aug. 1, 2006. https://www.electronics-cooling.com/2006/08/thermal-conductivity-of-solders/.
3. See, for example, Brooks, Douglas and Adam, Johannes, *PCB Design Guide to Via and Trace Currents and Temperatures*, Artech House, 2021, Section 8.7, "Thermal Vias."

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DR. JOHANNES ADAM, CID, is founder of ADAM Research, a technical consultant for electronics companies, a software developer, and author of the Thermal Risk Management simulation program. View their recent video on Thermal Via and Trace Currents and Temperatures on the PCEA YouTube channel or at Printed Circuit University.

SIGNAL **MODELING**

How Interconnects Work: Anatomy of Crosstalk

Models for understanding sources, quantification and mitigation of crosstalk.

by YURIY SHLEPNEV

Crosstalk in PCB and packaging interconnects is arguably one of the most complicated phenomena that may cause signal degradation. It is caused by unwanted coupling between signal links and between signal links and power distribution systems. The effect is deterministic, but very difficult to predict in many cases – too many variables and uncertainties. Crosstalk effects can be treated statistically as a deterministic jitter with a bounded distribution, but the distribution is usually not known and just guessed.

A direct analysis of a worst-case crosstalk scenario may lead to a system overdesign. Neglecting it in design may cause a system failure that is difficult to find and fix later in a design process. On top of that, distortions caused by crosstalk cannot be corrected by signal conditioning techniques at the receiver side. Thus, it is very important to understand the sources of crosstalk, how to quantify it and how to mitigate it efficiently. This is the first part of the paper with an overview of crosstalk sources and terminology – just a slice through the complicated phenomenon. The second part will describe and compare different ways to quantify, compute and measure crosstalk. This paper continues the "How Interconnects Work" series.[1-4]

Crosstalk in the Balance of Power

The best way to describe "what happens to a signal on the way to the receiver" is to use the

balance of power, which can be written for a passive interconnect as follows[4]:

P_out = P_in – P_absorbed – P_reflected – P_leaked + P_coupled

This is applicable to both the time domain and the frequency domain over the bandwidth of a signal[1]. **P_in** is the power delivered by a transmitter to the interconnect (useful signal) and **P_out** is the power delivered to a receiver (degraded useful signal + noise). All other terms in the balance of power equation describe the signal distortion. The absorption and reflection terms (**P_absorbed** and **P_reflected**) were discussed in the previous papers of the "How Interconnects Work" series.[2-4] This paper is about **P_leaked** and **P_coupled** or the crosstalk parameters:

P_leaked is power leaked into other coupled interconnects, into the common mode and possibly, into power distribution network (PDN is just another type of interconnect) and into free space (radiated) – that leak causes signal distortion and is a possible source of crosstalk in addition to being source of EMC/EMI.

P_coupled is power gained from the other coupled interconnects, common mode, PDN and free space – this is the crosstalk.

Crosstalk in general is just unwanted noise from the coupled structures (**P_coupled**) caused by unwanted signal leaks (**P_leaked**) that degrade the useful signal and may reduce the data transmission rate and even cause complete link failure.

Crosstalk Types

Unwanted coupling in PCB and packaging interconnects can be separated into local and distant couplings:

1. **Local coupling** between closely spaced traces and vias:

    - Coupling in closely routed signal traces – the most common source of crosstalk

- Common to differential mode interference and crosstalk due to modal transformations in differential pairs (caused by bends, asymmetry in routing, fiber weave effect)
- Local couplings through slots and cutouts in reference planes
- Local coupling between vias and between vias and traces due to proximity.

2. **Distant coupling** through parallel planes and split planes (slots), and through surface dielectric layers and PCB enclosure (multipath propagation).

Local couplings can be accurately simulated in general and taken into account during pre- and post-layout signal integrity analysis. Coupling in parallel traces can cause not only crosstalk and interference (unwanted noise), but also additional losses due to signal energy leaks to adjacent links (suck outs) – this is P_leaked in the balance of power. Leak losses may be significant in traces routed on the surface of PCB (microstrips). They are usually negligible for traces routed between parallel planes (striplines), however.

The distant coupling may cause a system-level interference and requires complete PCB or package analysis. The distant system-level coupling is very difficult to model and predict with sufficient accuracy. It can, however, be avoided (no rouging over split planes) or easily reduced by enforcing the localization for each structure that may potentially be coupled to parallel planes (transmission planes), surface dielectric layers or to the enclosure. Such coupling occurs at locations of changes in reference conductors. Unlocalized vias are the major source of leaks and crosstalk that can be easily avoided with the use of more stitching vias closer to signal vias, for instance. The system-level interference must be avoided by use of only the structures that are predictably localized up to the target frequency (conditional localization).

Crosstalk Origin

PCB and packaging interconnects, such as striplines, microstrip lines and coplanar waveguides, are open waveguiding structures. This means that the signal energy propagates along the PCB and packaging traces mostly in dielectrics around the signal conductors. It can

be illustrated with the peak power flow density (vector product of electric and magnetic field) for a typical PCB stripline interconnect shown in **Figure 1.** This is the peak power flow density (PFD) of a signal with 0.5V magnitude normalized to maximal value and expressed in dB as 10*log|P|.

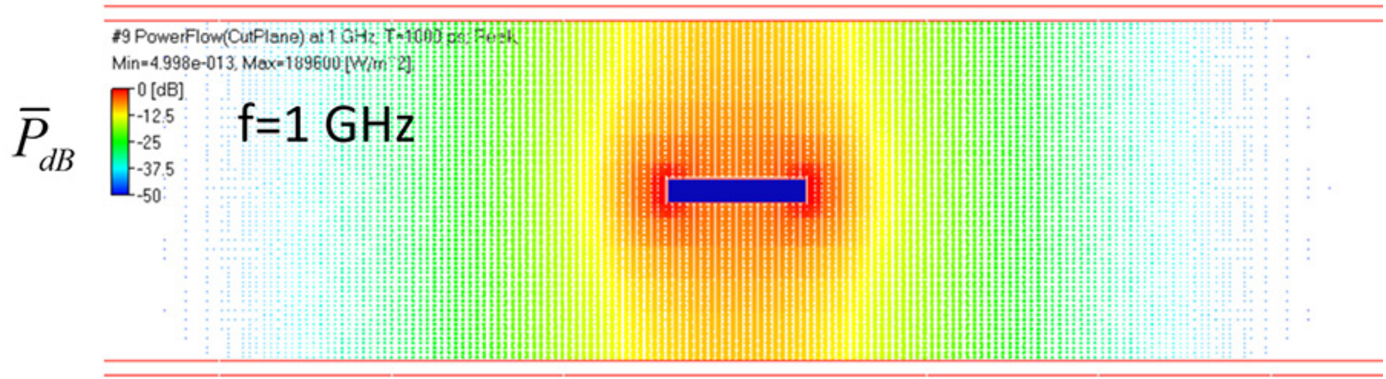


Figure 1. Power flow density in stripline 1.2 mil thick, 7 mil wide, DK=3.76, LT = 0.006 @1GHz, planes 0.77 mil thick, 17.2 mil apart, color scale is used to plot peak power flow density in W/m^2; computed with Simbeor THz.

As you can see, there is no exact localization of the signal energy. The power flow density or signal energy concentrates near the strip edges and between the strip and planes. The red and yellow area is where most of the signal energy propagates. But it is also nonnegligible in in the green area of two to three strip widths in this case. Everything that gets into zone with green PFD (-25 to -30dB level, two to three widths of strip on both sides) becomes coupled, and that coupling may cause interference or crosstalk and signal leaks. In addition, the coupling changes the strip impedance. The image in Figure 1 is for the dominant strip line mode that has equipotential reference planes.

The signal energy spreading around a signal conductor is even worse in traces routed on a surface of PCB (microstrips) as we can see from **Figure 2.**

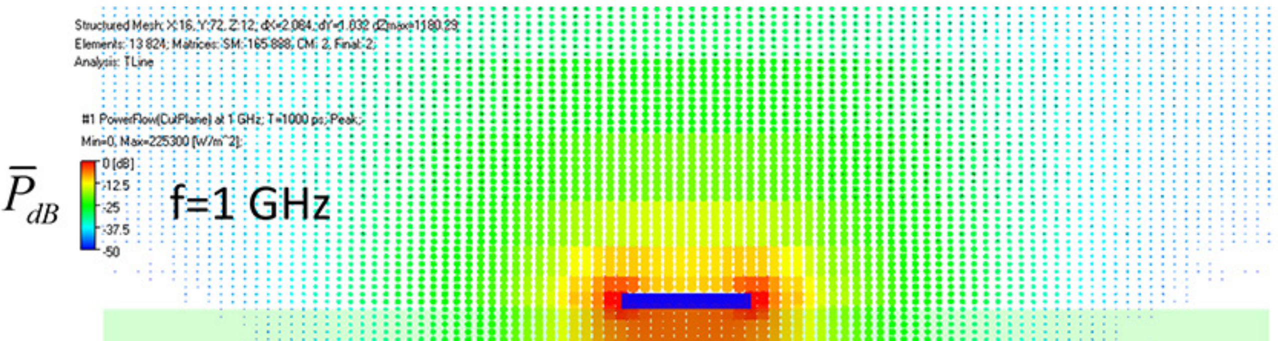


Figure 2. Peak values of power flow density at 1GHz in microstrip line with 8.256 mil wide trace on 4.5 mil FR-4 substrate.

As we can see, the area of potential coupling is larger in the air as well as in the substrate – the trace can be effectively coupled to nearby traces as well as to any external objects in the area with green PFD (-25 to -30dB).

Similar or even worse extension of the coupling area can be observed in unsymmetrical strip lines as illustrated in **Figure 3.**

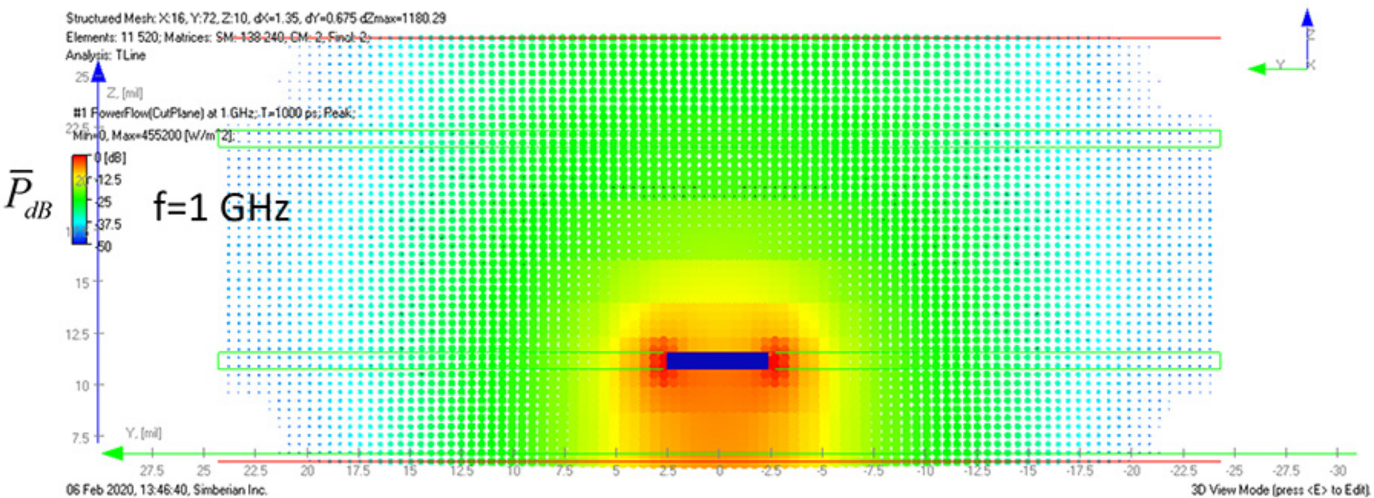


Figure 3. Peak values of power flow density at 1GHz in unsymmetric strip line with 5.4 mil trace, distance from strip to top plane 9.77 mil, distance to bottom plane 4.5 mil, Dk = 4.2 (~50Ω).

The differential mode in loosely coupled differential traces has signal energy spread similar to the single-ended case as illustrated by the peak power flow density for a typical differential microstrip in **Figure 4.** Peak PFD for a differential mode in a differential stripline with unsymmetrical reference planes is shown in **Figure 5.** As we can see, the distant reference planes may substantially increase the area where strips can be coupled even in the differential cases. The PFDs in Figures 4 and 5 are for the differential modes with excitation +0.5/-0.5V. The power of the differential mode flows around each trace in the same direction mostly along the traces.

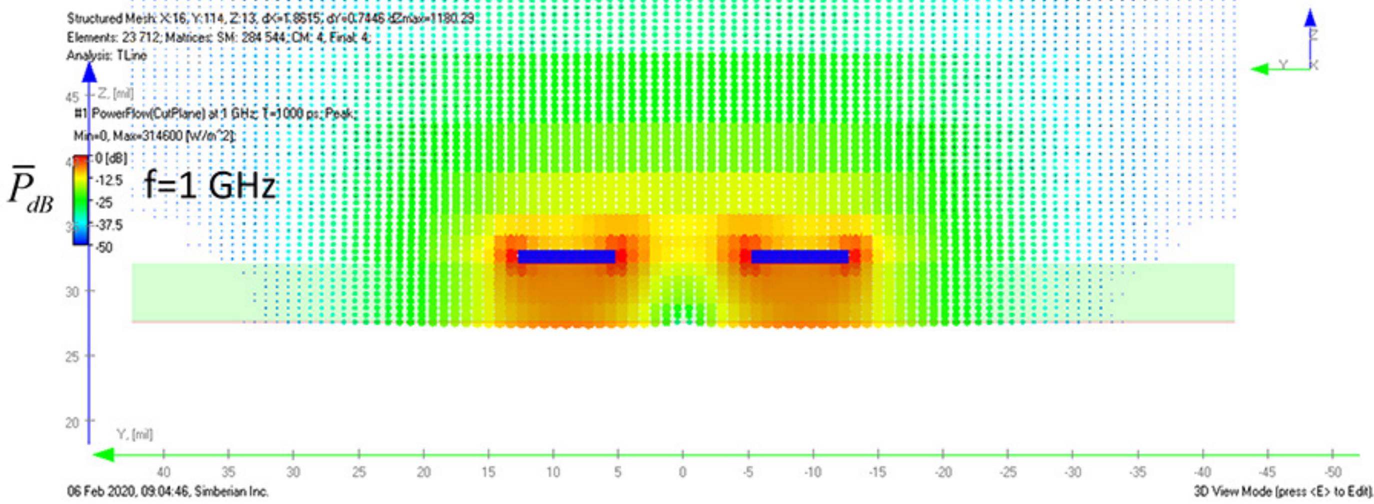


Figure 4. Peak values of power flow density at 1GHz of differential mode in differential microstrip line with 7.446 mil traces on 4.5 mil on substrate Dk = 4.1 (~100Ω).

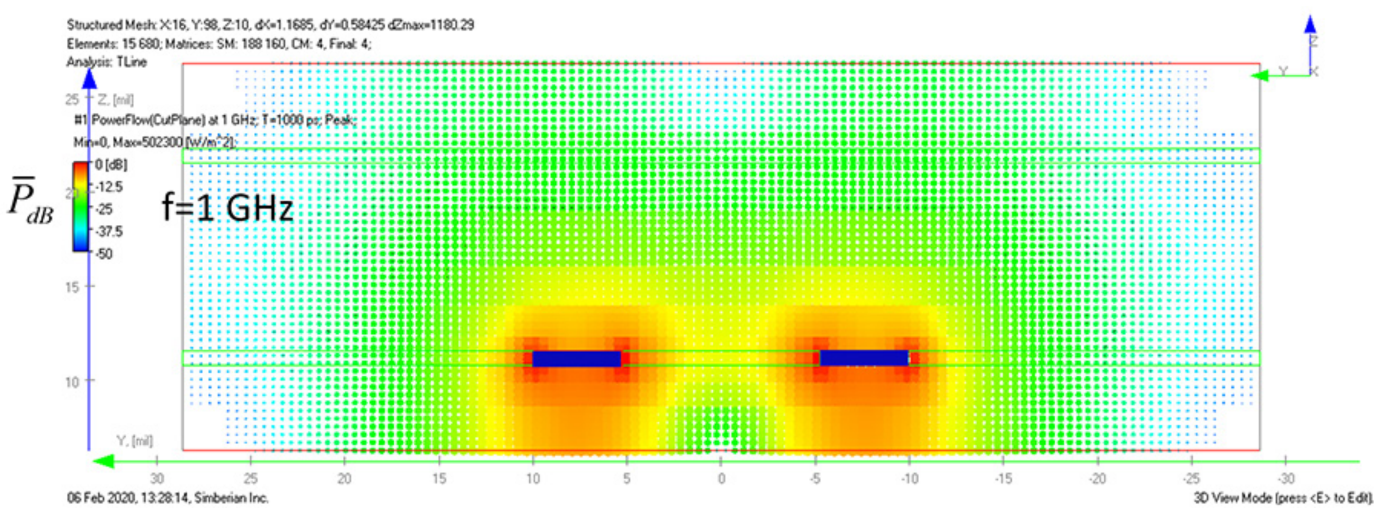


Figure 5. Peak values of power flow density at 1GHz of differential mode in unsymmetrical stripline with 4.674 mil wide strips, distance from strip to the top plane 9.77 mil, to the bottom plane 4.5 mil, Dk = 4.2 (~100Ω).

The currents at microwave frequencies are not "flowing" and not "returning" anywhere – they are just a part of the wave propagation process and conductor energy absorption. The power flow density is the best way to visualize the physics of a signal propagation. The surface currents in the reference conductors can be used to evaluate possible coupling areas, yet it is not so intuitive and obvious as with the PFD.

In general, it is important to understand that a single trace is a two-conductor transmission line or waveguiding structure: the second conductor is always the reference plane (microstrip) or two planes (stripline). Differential traces are a three-conductor transmission line and the currents in the reference conductor are also spreading beyond the traces, similar to the single-ended cases. Reference conductors or planes in the signal energy propagation area are as important as the traces themselves. In a case of two reference planes, the equipotentiality of the planes along the signal propagation must be ensured with more stitching vias and even via fences, to avoid coupling to the dominant mode of the parallel plane structures; such coupling may occur at discontinuities such as vias and at dielectric inhomogeneities. Enforcement of the reference equipotentiality for coplanar transmission lines is even more complicated.

The bottom line is that the PCB and packaging interconnects are the open waveguiding structures with the signals propagating in space around the signal traces. Getting a signal with spectrum in microwave and millimeter-wave bandwidth from one component to another through an open waveguiding structure and without interaction with other signals is always a challenge.

Useful Crosstalk Terminology

Before proceeding with crosstalk modeling and quantification, let's define some common terms.

- **Stripline** – model for traces routed on the internal layers of PCB/PKG with two reference planes and mostly homogeneous dielectric
- **Microstrip line** – model for traces routed on surface of PCB/PKG with one reference plane and inhomogeneous dielectric
- **Coplanar line** – model of traces with additional reference conductors in the same layer with the signal traces
- **Aggressor** is a transmitter (Tx) or a link with a signal that may cause interference in other links

- **Victim** is a receiver (Rx) or a link that may pick up unwanted interference caused by an aggressor link
- **NEXT** – near end crosstalk is interference observed at the link side that is closer to the aggressor link transmitter or signal source
- **FEXT** – far end crosstalk is interference observed at the link side opposite to the aggressor link transmitter or signal source.

There are many more terms for the crosstalk characterization. PSXT, MDXT, ICN, ICR and some others will be introduced and explained in the next section on crosstalk quantification.

Crosstalk in Parallel Traces

To illustrate interference of signals in parallel segments of microstrip line (surface trace), we will use two single-ended links routed at a distance equal to one trace width over 1.0″ distance. The characteristic impedance of each single trace is close to 50Ω. In the first case a signal propagates in the top trace from port p1 to port p3 as illustrated in **Figure 6**.

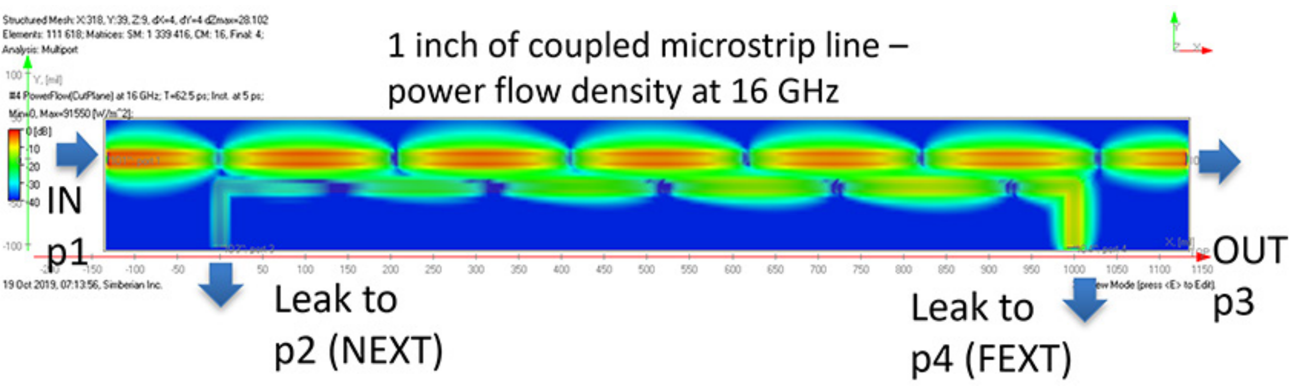


Figure 6. Instantaneous values of power flow density in dB with 16GHz 0.5V signal propagating from p1 to p2. 16 mil traces on 8 mil substrate with Dk = 3.9 coupled over 1" with 16 mil separation.

As we can see, the bottom link with ports p2 and p4 is literally in the “signal space” of the top trace. As the consequence, the bottom trace is coupled and “sucks out” some signal energy. Some useful signal power leaks into port p2 near the signal source (NEXT) and into port p4 on the side opposite to the signal source (FEXT). The leak is the result of the wave energy redistribution over the length of the coupled segment. How much energy is leaked and what

are the consequences of that leak if there is a useful signal propagating in both links?

The most fundamental and convenient way to describe this energy redistribution phenomenon is with scattering parameters or S-parameters.[5,6] It is very important to be familiar with the S-parameters. In fact, practically all other interconnect quality metrics including crosstalk quantification parameters are simply derived from the S-parameters. Magnitudes of the S-parameters describing the process of the energy redistribution for the structure from Figure 6 are shown in **Figure 7.**

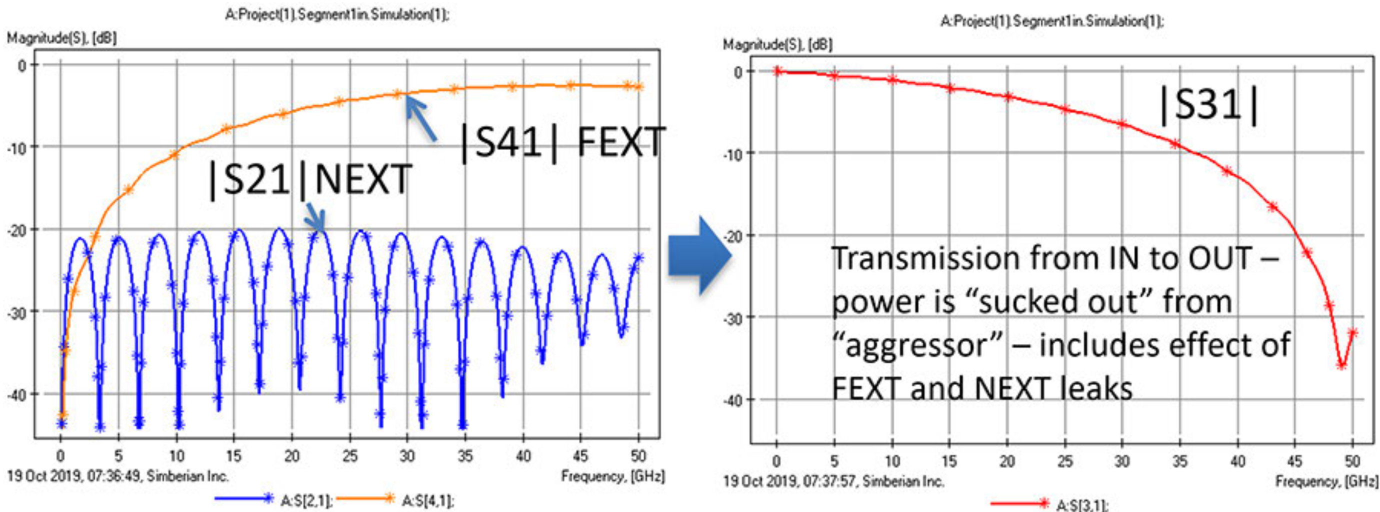


Figure 7. Magnitudes of coupling S-parameters (|S41|and |S21|on the left graph) and transmission parameter (|S31| on the right graph) for microstrip traces with 1" coupled segment from Figure 6.

Parameter S31 on the right graph of Figure 7 is the transmission of the useful signal from port p1 to port p3. Parameters S41 and S21 are the leaks and potential crosstalk parameters. The transmission|S31| is decreasing with the frequency, but with the slope that is much steeper than expected due to the material absorption losses.[2] The reflection or return losses are very small in this case. The reason for this is a leak into port p4 that is described by S-parameter S41 on the left graph in Figure 7. The leak into port p2 is much smaller in this case. With a useful signal at port p4, parameter S41 becomes far end crosstalk, or FEXT. It is frequency-dependent, and the maxima and minima are defined by difference of propagation velocities of the even and odd modes in the coupled segment and by the segment length. There is no FEXT if this difference is zero or close to zero.

FEXT can be observed in any lossy multi-conductor transmission line in general, but it

becomes substantial only in cases of transmission lines with inhomogeneous dielectrics – microstrip lines for instance. Striplines with dielectric layers with different properties also have observable and not-negligible FEXT. FEXT increases with the length of the coupled traces up to some level and then decreases, until it reaches minimum. Then minima and maxima repeat periodically with the frequency. In general, more energy from an aggressor link may leak into a victim link on links with longer coupling sections. The leak can interfere with the victim signal and degrade it. On the other hand, the leak also degrades the aggressor signal; it causes additional losses that can be comparable or even larger than the reflection and the material absorption losses. In fact, there might be conditions when almost all energy of the aggressor signal becomes FEXT. In the case above, almost complete suck out happens around 50GHz. For the same traces coupled over a longer 5″ segment, the complete suck out would happen around 10GHz, as illustrated in **Figure 8**. This is the Nyquist frequency for a 20Gbps signal. Extensive simulations must be used to detect and avoid such conditions early in the design process.

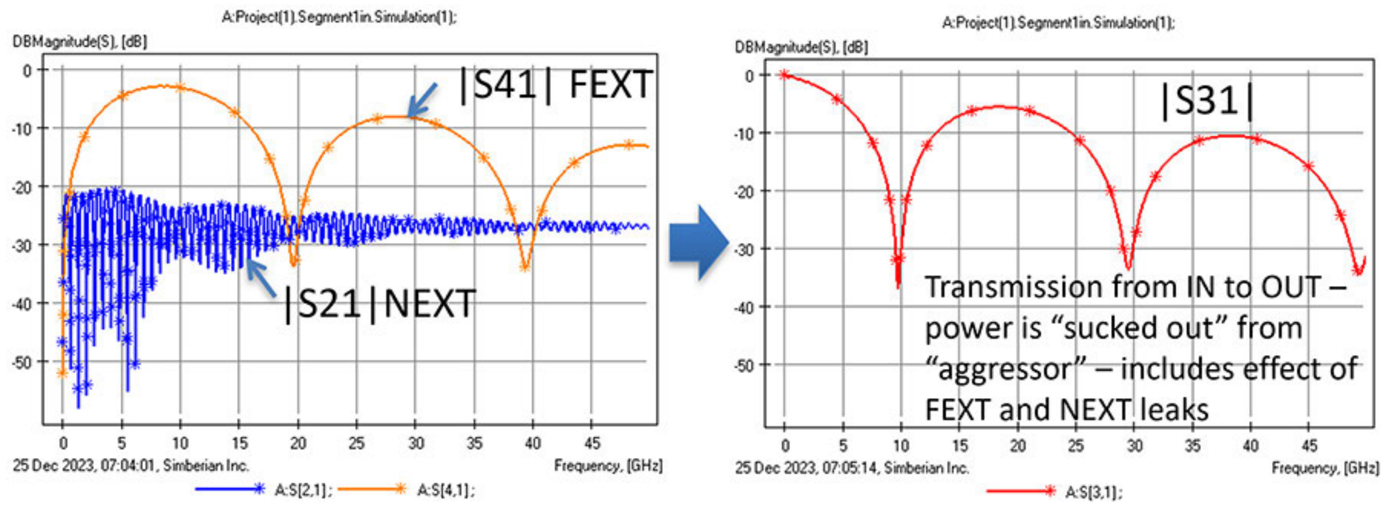


Figure 8. Magnitudes of coupling S-parameters (|S41|and |S21|on the left graph) and transmission parameter (|S31| on the right graph) for microstrip traces with 5″ coupled segment.

Note that S-parameters of passive interconnects are reciprocal. It means that transmission from port i to port j is always equal to transmission in the opposite direction from port j to port i. This is not a very intuitive property. Applying it to crosstalk, we can state that S41=S14, S21=S12; if the aggressor and the victim are switched, the crosstalk does not change. If the bottom link in Figure 6 has a useful signal, then that link becomes the aggressor for the top link as illustrated in **Figure 9.** The top link is the aggressor for the bottom link and the

bottom link is the aggressor for the top link. The result is the superposition of signals in both links and both links have FEXT.

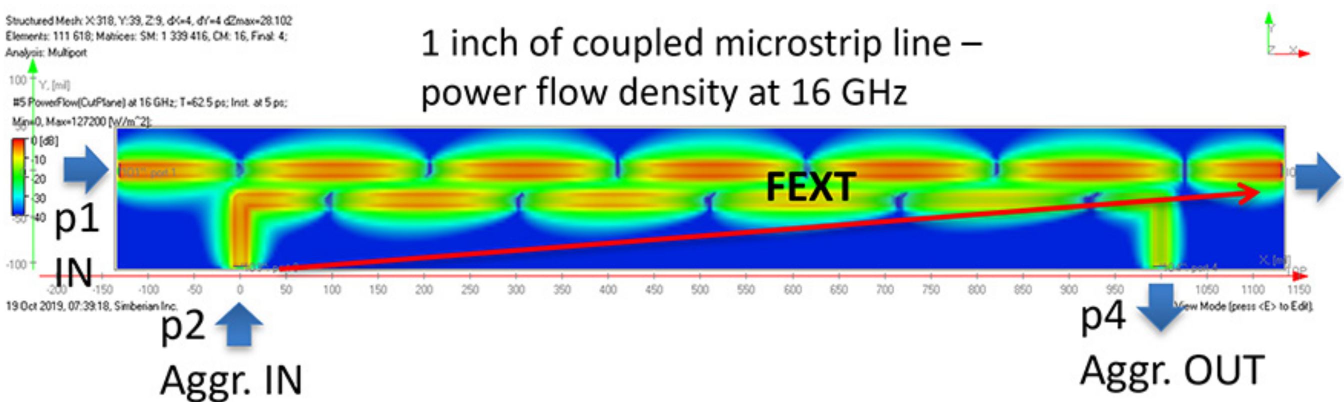


Figure 9. Crosstalk power flow density in coupled microstrip line segment from Figure 6 with two 16GHz signals propagating in the same direction from p1 to p3 and from p2 to p4.

Up to this point we have investigated the coupling in the frequency domain or for the time-harmonic signals. Digital signals are usually transmitted by pulses, however.[1] Let's take a look at crosstalk in the time domain. To do that, a pulse response can be computed from the S-parameters of the 4-port structure **(Figure 10).**

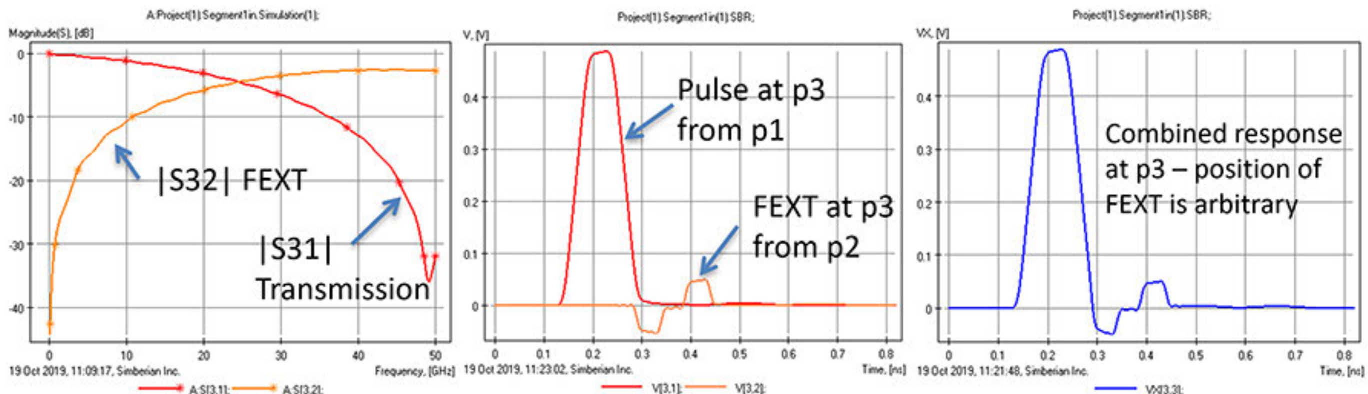


Figure 10. Frequency-domain FEXT and transmission parameters (left graph) with corresponding pulse responses (middle graph) and superposition of the pulse responses (right graph).

Transmission from port p1 to port p3 is characterized by S-parameter S31 on the left graph and corresponding pulse response shown in the middle graph in Figure 10. The bottom link is a potential aggressor in this case – it has leak to port p3 as illustrated with S-parameter S32 in Figure 10. If the bottom link has similar pulse propagating from port p2 to p4, some part of

the pulse energy is going to be leaked into port p3 of the top link. Corresponding pulse response for the crosstalk parameter is also shown in the middle graph in Figure 10. If both links have signals propagating in the same direction over the coupled segment, the signals at port p3 will be a superposition of the link pulse response and the crosstalk pulse response as illustrated on the right graph in Figure 10. Because the timing of the pulses at ports p1 and p2 is not synchronized, the crosstalk position is arbitrary with respect to the link pulse. That is what makes the crosstalk difficult to quantify. We can find the worst-case relative timing, but it may never happen.

Let's return to the near-end crosstalk. S-parameters S21, S12, S34 and S43 describe the near-end crosstalk or NEXT in cases when the signals in the top and bottom links are propagating in the opposite directions as illustrated in **Figure 11**. The NEXT is frequency-dependent and has nulls at frequencies where the coupled segment is about a multiple of a half of wavelength as illustrated on the left graph in **Figure 12**. The maxima in NEXT are approximately at frequencies with the wavelength equal to odd multiple of a quarter of wavelength. The near end coupling depends on the length of the coupling section. Though the frequency-domain pattern of the NEXT is considerably different from the FEXT.

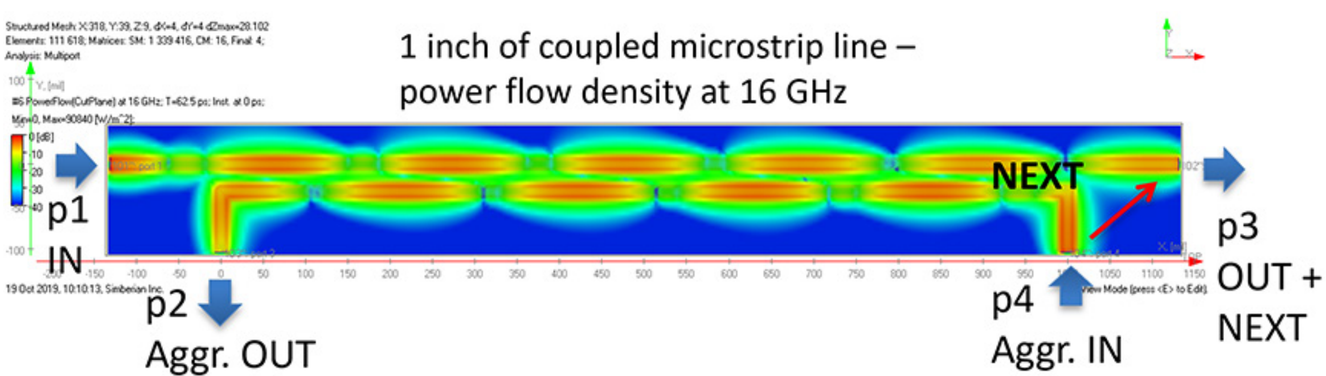
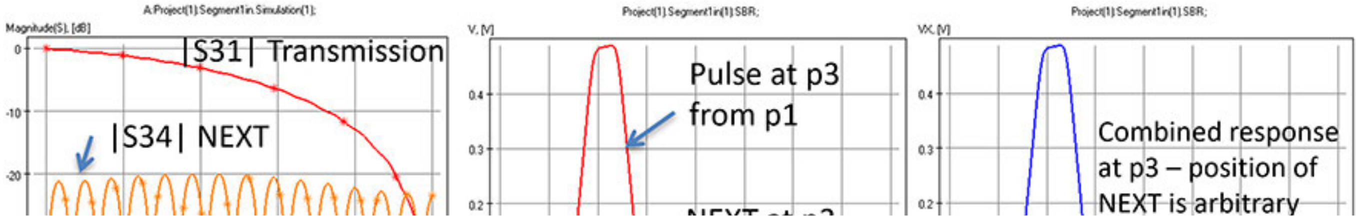


Figure 11. Crosstalk power flow density in coupled microstrip line segment from Figure 6 with two 16GHz signals propagating in the opposite directions from p1 to p3 and from p4 to p2.



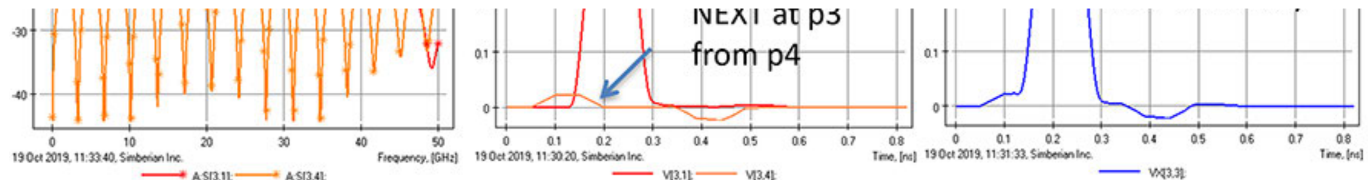


Figure 12. Frequency-domain NEXT and transmission parameters (left graph) with corresponding pulse responses (middle graph) and superposition of the pulse responses (right graph).

As we can see the level of maxima of NEXT in this case is about -20dB. That gives a relatively small crosstalk pulse response (smaller than FEXT in this case) as shown on the middle graph in Figure 12 together with the pulse transmitted from port p1 to port p3. It comes in two parts: the first appears at the victim port p3 almost immediately, and the second part appears with a delay. There might be no second part for a longer links with substantial attenuation. A superposition of the useful signal and crosstalk at the port p3 is shown on the right graph in Figure 12. As in the case of FEXT, timing of the NEXT with respect to the pulse of the useful signal is also arbitrary. Note that the signal in the victim link may be substantially attenuated at the received end – that means that much smaller values of NEXT can cause failure of the victim receiver. All coupled nets have NEXT. Though, it is important how close to the victim receiver it appears.

Finally, here is how crosstalk in coupled transmission lines can be "explained". A signal in multi-conductor interconnects propagates as a superposition of multi-conductor line modes – this is a model presentation, but it reveals what happens there and what to expect. For instance, differential signal on the NEXT or FEXT aggressor side becomes a superposition of four waves in coupled two-conductor transmission line segment. Those are the even and odd modes propagation in both directions. The signal cannot remain on just one trace due to the coupling. The waves propagating toward the aggressor side are observed as the NEXT. The waves propagating forward from the aggressor are observed as the useful signal in the aggressor link and as the FEXT at the victim port. If all modes have identical propagation velocity (which never happens in real lossy lines), there will be no FEXT. If the modes are not ideally terminated at both ends, however, the waves forming NEXT are reflected and may appear at the other end as the FEXT. Waves that compose FEXT can be also reflected and become NEXT. To understand different coupling outcomes, a lattice diagram with the transmission line modes superposition can be used, but advanced modeling is an easier way

to account for all those reflections.

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The PCB Podcast

Building the Efficient Design System

EMA founder Manny Marcano lays out his strategy for untethering methodology and technology.

by MIKE BUETOW

EMA Design Automation has for years been exclusive distributor of Cadence's OrCad products in North America and Europe. Through acquisitions and internal development EMA now has a series of its own software products for library management, component supply chain data, and other areas.

Late last year EMA announced it would spin off those CAD-agnostic products into a standalone company.

We spoke in January with Manny Marcano, president and founder of EMA, on the PCB Chat podcast. The following transcript has been edited for clarity.

Mike Buetow: The last time we spoke on PCB Chat, EMA had just purchased Trilogic EDA. Now you are sharing what I think is bigger news: the spinoff of your IP content and services offerings into this new subsidiary. You're calling this Accelerated Designs, which is also the name of the parts library business you acquired back in 2016. You have developed numerous products over the years, all under the EMA logo. So why a separate company and why now?

Manny Marcano: It's a great question, Mike. I've been doing this a long time, as you know, and the tools are what they are. They all have their way to go to market and capabilities.

But the real emphasis in the market in my opinion is not so much technology as it is

methodology. It's more about how to get the job done than how many clicks or how efficient your router is. Those are all important, but the grand vision is time to market and that's what we're addressing with Accelerated Designs. It's all about getting it right the first time, shift left, instantiate the right part in the schematic so that it's orderable and deliverable with the life cycle that you need at the procurement level.

It's really adjusting to the needs of the market and not just one particular vendor. Everybody's got the same problem, and this is something I've observed over the years; something we've addressed at EMA as far as selling a methodology versus tools. I'm just taking that to the next level as a supply-chain provider and addressing time-to-market issues.

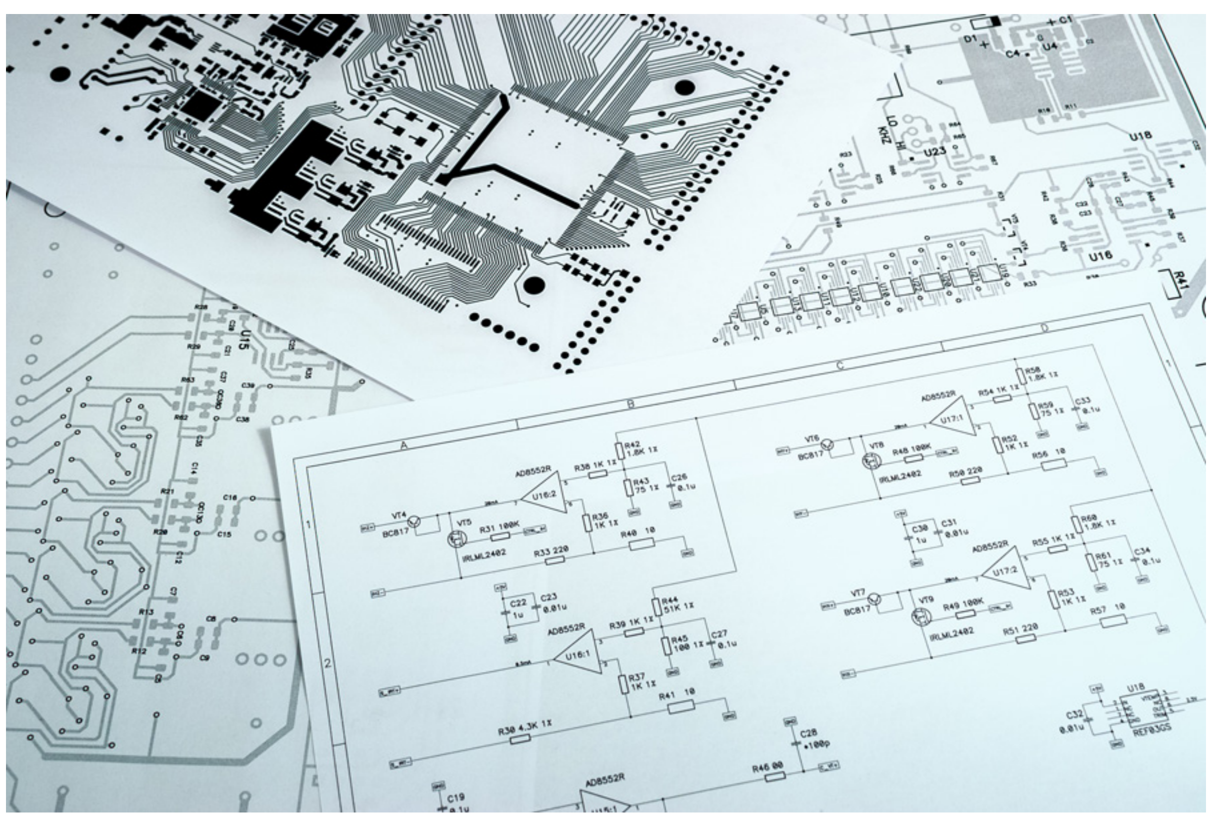

Figure 1. The spinoff of Accelerated Designs underscores Marcano's goal to synchronize the schematic, footprints and models, and procurement.

MB: Let's go through the list of properties included in the spinoff. I know that Ultra Librarian, which is your EDA library product, is prominent among this but it goes beyond that.

MM: Absolutely. Much credit goes to Frank Frank (Ed: Frank was founder of the original

Accelerated Designs). We're old friends, and seven or eight years ago we got together and agreed to merge. I found out very quickly that the library is not just for one vendor; it is tool-agnostic. The VXL that Frank invented essentially is a generic format that can go to any EDA tool. That's pretty much the foundation of what we're doing.

From there we're building an intelligent library. Ultra Librarian right now is a schematic symbol, a PCB footprint and STEP models. But we're also starting to grow rapidly into the simulation models, intelligent models. This to me is the baseband for the intelligence for NBSC or AI. We're building that foundation as fast as we can.

When you do that you have to look at what are the needs of other EDA users. They have exactly the same design requirements. They use the same parts. There's nothing unique about your library other than the specific format for your tool. So we grow from there into things like our component information portal that is a direct integration to (component distributors), so inside your schematic tool you can look at what's available in inventory at DigiKey and many other distributors.

We also have an integration of SiliconExpert. Now you can get your geometries, your parametrics for that particular part number from DigiKey, and obsolescence and lifecycle information via a SiliconExpert license, and all of that is shifted left to the engineer at their desktop. It's a pure productivity environment. We believe that this is the future.

MB: Was this something that the marketplace directly suggested you do or was it just your feeling that potential customers felt that you may have been too identified with one CAD vendor and it may have been holding back all the other products that EMA offers?

MM: Absolutely it was holding us back. That was the driver, to just expand to being vendor-agnostic.

MB: Were you kicking this around for a while? I've known you for years, and you have lots of ideas and visions. You really think ahead. But when you make up your mind, Bang! It's done.

MM: I appreciate that, but like most lessons in life I learned the hard way. So yeah, specifically on the library issue, we lost a big deal because we didn't have a library and it wasn't about my schematic beating their schematic. The other vendor had a library and I didn't and literally that was a pretty big bump in the road. That's when I reached out to Frank and we did our deal.

That hard lesson convinced me to move forward but over the last five years or so we've been selling methodology. We've been selling solutions. We have lots of multinationals that have multiple EDA systems that need to talk to each other. A common library for a global account … our customers say this is what they need. We just address the need.

MB: Who will make up the management of Accelerated Designs?

MM: That's a work in progress. [laughs] We're not venture-funded or private equity. We're doing it the old-fashioned way, a little bit at a time. I'm doing a lot of the heavy lifting and I borrow staff from EMA now and then. It will eventually evolve to getting some degree of funding, either from customers or outside, but this is a slow work in progress.

MB: I imagine your bookkeepers must not be happy with you right now.

MM: That's why I travel more.

MB: As I understand it there's a distribution agreement with Accelerated Designs as well. How will that work?

MM: What we're looking at, as you pointed out earlier, we do have a vast network of EMA sub-VARs, if you will. I merged with Flo-CAD a couple years ago, so I have my own entity in Europe. We've got the UK, Ireland, South America, India, and so on. Accelerated Designs would be available to all of those folks, depending on what their areas of interest are, and if that particular team isn't specifically interested in that strategy we can still sell it directly ourselves. We've already built an ecommerce platform worldwide and we have a network of people that can sell and support these products anywhere. We've got well over 250,000 registered users of Ultra Librarian alone worldwide. We've got a hell of a good base to build on.

MB: Does the library tend to act as a pull through for the CAD tool or is it usually the other way around?

MM: It really is a pull through for the CAD tool. The better your methodology, the more pristine your library, the better your CAD tool is going to behave. We go through these exercises with a customer where they want to import all their legacy library into the new CAD system. You don't want to do that. We explain to them that it's hazardous because you're bringing in garbage. Some of these obsolete parts number in the thousands. You still have to maintain that library.

Our initial pass is to help the customer understand to cleanse the library, and get it in the format they need for their tool. Now you have a pristine library to move forward and that's very applicable to multinationals that have five different geographic locations, and five different libraries. You've got to be able to converge that to one corporate library, for lots of good reasons, not the least of which is economies-of-scale.

MB: What was Cadence's reaction to all this?

MM: I think they're generally very supportive of it. I think they've even mentioned some different strategies of their own. For example, the Autodesk play; they see the need to be more agnostic than just a monolith of technology.

MB: Are there other areas where you see that you can build off the new subsidiary?

MM: Absolutely. Simulation is probably the biggest one, so we're also at Sovar; we're selling the simulation products from them. Most vendors say, "Here's your simulator but you're on your own for your content, your models." We're aggressively pursuing aggregating vendor-approved models … the simulator's an engine, but the engine's useless without the fuel. The library becomes the fuel and if you don't have simulation models – PSpice, IBIS models or thermal models, even to the extent of RF models for AWR … you have to have all that stuff tied in if you want to have an efficient system.

All this is available, but an engineer spends an inordinate amount of time searching websites

for a model, so just like in UL they could search millions and millions of parts and get the one they want, but now I want to have the extension of that simulation model attached to it.

MB: I reached out to you late last year to address some of the market trends in the EDA industry. There's only been three down quarters over an extended period. Now that the Consumer Electronics Show is just wrapping up and you see some of the products coming out of there – transparent TVs, IoT, medical wearables, electric vehicles – all sorts of products are driving the marketplace, would you agree there is reason to be very optimistic about what the future holds for electronic design?

MM: I think it's an understatement everything is going to be electrified. There is no end to it. When you look at wearables and EVs or any level of technology, everything is going to be electrified. And no matter how fancy or how leading-edge your chip is, you know the saying is "chips don't float without a board." What are you going do with your chip? Whether it's a reference design or production design. it's got to go on a board. That board may be something that's implanted in your body but is still a printed circuit board. There's no end to it.

MB: Care to share your expectations for 2024?

MM: I think 2024 is going to be absolute chaos. But you know in our mainstream world, there is no end to the opportunities and really the key is our ability to execute and reach out and find those folks in pain. And we just start doing the best we can.

I'm always the optimist. I see lots of upside for everything we're doing.

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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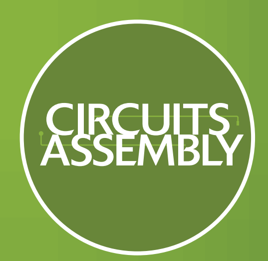

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MINIATURIZATION

High-Density Interconnect Technology: An Overview

Design and manufacturing considerations for HDI PCBs.

by AKBER ROY

High-density interconnect (HDI) technology has been a major enabler of advancement in the electronics industry, providing the dense interconnections and intricate circuitry needed to create state-of-the-art electronic devices that are tightly packed with miniaturized components and 2.5-D/3-D semiconductor packages. Miniaturization at the semiconductor level has driven miniaturization at the PCB level, with manufacturers striving to shrink the size of devices while maintaining or enhancing their capabilities. This has led to the development of compact smartphones, slim laptops, and wearable gadgets that seamlessly blend into our daily lives **(Figure 1)**. Alongside miniaturization has been a constant push for faster processing speeds. As technology evolves, the processing power of electronic devices has skyrocketed, enabling quicker data processing, seamless multitasking, and smoother user experiences.

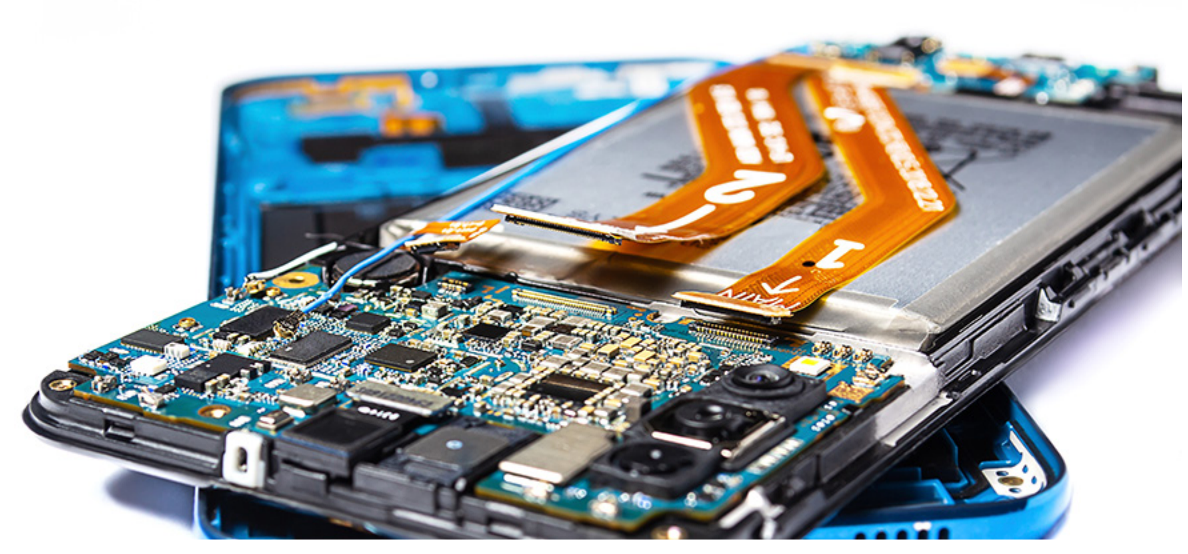


Figure 1. Miniaturization demands for electronics have driven developments at the semiconductor and PCB levels.

Production and assembly of HDI PCBs comes with unique technical challenges centered around reliability and quality. Achieving the intricate high-precision conductive patterns and traces needed to ensure reliability, efficiency and performance requires specialized manufacturing capabilities, particularly where high-layer-count PCBs are required. PCB manufacturers with expertise in HDI technology are helping customers successfully navigate the complexities of designing and fabricating HDI circuitry and enabling the industry to push the boundaries of miniaturization and functionality.

The following provides an overview of standards and best practices for designing and building HDI PCBs.

Guidelines and Standards

Following international guidelines and standards provides manufacturers of HDI PCBs with many advantages. From improved efficiencies and process controls to enhanced product quality and customer satisfaction, adopting international standards as a guide can reduce costs and help gain access to new markets with strict quality requirements.

Among the important IPC and JPCA standards concern HDI PCBs:

- IPC/JPCA-2315, "Design Guide for High Density Interconnects (HDI) and Microvias," which outlines design recommendations for HDI PCBs;
- IPC-2226, an extension of the generic guidelines for PCB design (IPC-2221), which provides in-depth standards and guidance for HDI PCB design;
- IPC/JPCA-4104, "Specification for High Density Interconnect (HDI) and Microvia Materials," which specifies material sets appropriate for HDI PCBs, covering various

conductive and dielectric materials that can be used;

- IPC-6012, "Qualification and Performance Specification for Rigid Printed Boards."

These IPC standards collectively provide guidance on HDI PCB design and manufacturing.

2.5-D and 3-D Packaging

Modern semiconductor packaging within the concept of heterogeneous integration plays an important role in miniaturization. Due to challenges of ensuring high yield with larger monolithic silicon processors, heterogeneous integration emerged as a concept for placing multiple diverse semiconductor dies into the same package and connecting them within the package. This essentially consolidates the diverse functionality of two or more components into one smaller package. 2.5-D and 3-D packaging technologies are enabling smaller and more advanced devices through the integration of multiple heterogeneous features and functions into a single component.

2.5-D packaging involves stacking multiple dies or chips on an interposer, which in turn is bonded onto a substrate. 3-D packaging takes miniaturization further by vertically stacking multiple layers of components on a package substrate **(Figure 2)**. These advanced packaging technologies increase functionality while enabling a smaller device footprint. HDI PCB fabrication technology is needed to create the multilayer boards with intricate electrical connection paths that link 2.5-D and 3-D semiconductor packages, and together these technologies have enabled many of the consumer electronics we enjoy today.

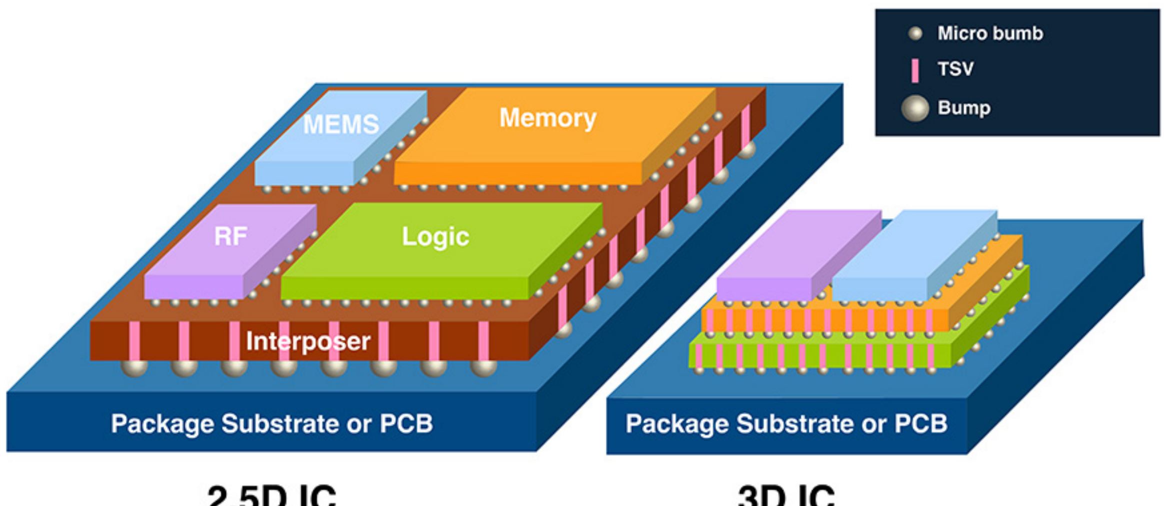


Figure 2. Examples of 2.5-D packaging and 3-D packaging.

Design Considerations

Designing HDI circuit boards necessitates careful consideration of several critical factors to ensure optimal performance, functionality and reliability.

- First and foremost, the layout and placement of components demand meticulous planning to make the most of limited board real estate while preventing signal interference. This includes selecting the right package types and strategically locating critical components.
- Keep track of minimum trace widths and spacing, which can be incredibly narrow, measuring just a few mils (thousandths of an inch) or even less. For example, HDI PCBs commonly feature trace and space widths in the range of 2 mils (50µm) or smaller.
- HDI PCBs use multiple types of vias to make vertical electrical connections. From microvias, and blind and buried vias to stacked and staggered vias, choose via types and placements wisely. Each serves a unique purpose and influences the routing density and signal integrity.
- Pay attention to impedance control, as HDI circuits often handle high-speed signals. Proper impedance matching and controlled trace geometries are crucial to minimize signal reflections and losses.
- Thermal management is another vital consideration, given the higher component density, processing power and speed in HDI boards. Effective heat dissipation strategies, including the use of thermal vias and copper pours, are essential to prevent overheating and ensure long-term reliability.
- Material selection is critical, with consideration of material characteristics such as dielectric constant, thermal properties, and mechanical strength. All materials used to fabricate and assemble the HDI PCB can significantly impact signal performance and

board reliability, especially the choice of substrate material.

- Finally, optimize for fewer layers. Boards with higher layer counts require more assembly steps and increase manufacturing costs.

Overall, HDI circuit board design necessitates a comprehensive understanding of the application's specific requirements, precise planning, and a deep knowledge of advanced PCB manufacturing techniques to achieve the desired level of miniaturization, signal integrity and reliability in today's high-performance electronic devices.

Vias Types

All PCBs use layer-to-layer connections, including HDI PCBs. Typical HDI PCBs use more layers than traditional PCBs, however, and require multiple types of vias to create connections between the various layers. From microvias, blind vias, and/or buried vias to via-in-pad, via tenting and plugging, wise selection of via types and their placements requires an understanding of component pin pitches and how electrical signals are designed to flow in the device **(Figure 3)**. This will drive the manufacturing processes used to build the board, as well as the feature sizes placed in the board.

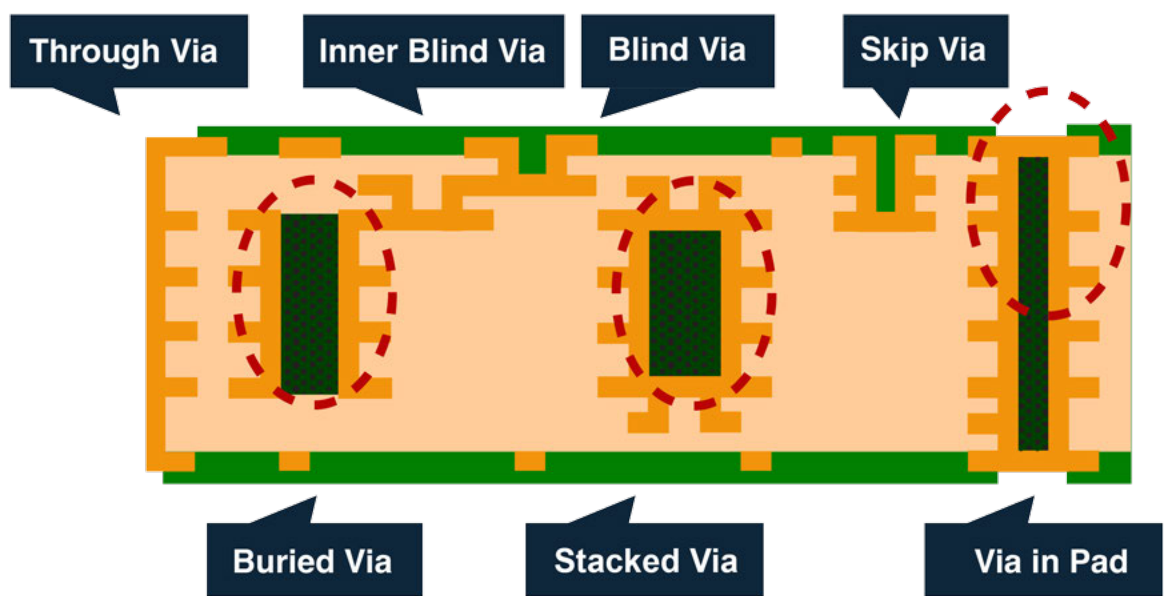


Figure 3. HDI PCBs use multiple types of vias to create connections between various layers.

Through-hole vias (THVs) are the standard via type used to connect different layers in a PCB, including in HDI PCBs. These vias, as their name suggests, traverse the entire thickness of the board, allowing for electrical continuity between top and bottom layers. THVs are well-suited for most applications, including high-power and high-speed designs. They are also preferrable with large components with pin leads such as connectors, where mechanical strength and reliability are paramount.

In addition to THVs, various other via types are used in HDI PCBs, but these other types do not span through the entire layer stackup. Other via types include:

- Blind vias, which connect the outer layers to one or more innerlayers without traversing the entire PCB
- Buried vias, which link innerlayers without extending to the board's surface.

Blind and buried vias are constructed by means of mechanically or laser drilling, depending on the hole diameter required. In general, the smallest mechanical drilling diameter available for use in HDI PCBs is 6 mils. Smaller via diameters must be laser drilled. These smaller vias are called microvias due to their small diameters. In very dense, high layer count boards with many fine-pitch components, microvias may be the only way to route signals in and out of a component.

The advantages of laser drilling are numerous. NC laser drilling provides high precision and fast fabrication, making laser drilling suitable for high-volume production. Laser drilling is also compatible with a wide range of HDI PCB materials, including organic substrates, ceramic-filled PTFE materials and glass-epoxy composites, making laser drilling an ideal choice for diverse PCB applications.

Compared to the smallest mechanical drilling available at 6 mil, the key advantage of laser drilling is faster processing speeds and reduced need for frequent tool replacements. This is what permits laser drilling to be cost-competitive with traditional mechanical drilling. While lasers can provide drilling to varying depths, keep in mind that we are looking for a hole that can be reliably plated. That is why microvias should not exceed a 0.010″ depth with an aspect ratio of 1 to 1 (diameter to depth). Larger ratios and depths will likely result in plating defects.

That's why we recommend that laser drilling only be used on thinner HDI buildup layers. Mechanical drilling is better suited for use on thicker layers.

Via-in-Pad

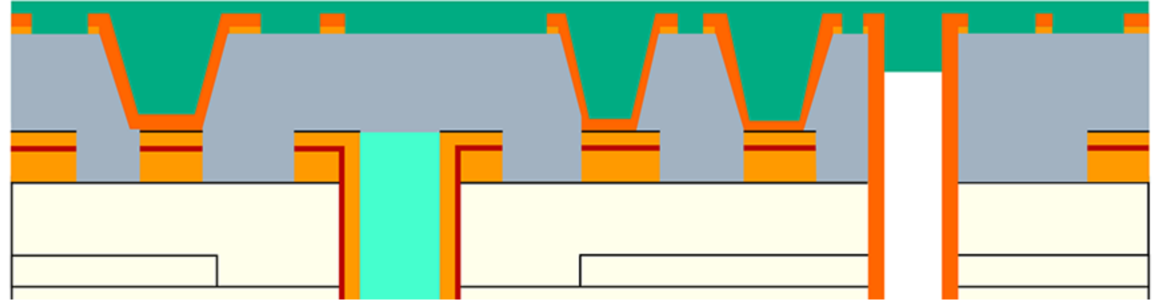
An important design practice in HDI PCBs is via-in-pad, which is the placement of vias directly under surface mount component solder pads, instead of routing the trace around the pad. Via-in-pad serves to miniaturize the PCB size by reducing the amount of space required by trace routing.

Normally, solder would wick through to the back layer of the PCB. To prevent this, via-in-pad requires filling and capping of vias. Filled vias are fabricated by filling traditional through-holes or blind vias with a conductive or nonconductive material. Microvias can also be filled and plated and used as VIP in HDI PCBs.

Conductive filled vias are typically filled with conductive epoxy. The use of conductive materials permits higher current carrying capacity in a PCB. On the other hand, nonconductive filled vias are filled with an insulator that blocks solder flow through the via but does not impact the DC electrical characteristics. To ensure the PCB can be assembled while preventing solder wicking during assembly, filled vias that are used as via-in-pad must also be capped, or plated over with copper. This provides a metal surface where components can be mounted and soldered.

Via Tenting and Plugging

Via tenting and plugging are two processes that involve sealing or covering vias, either partially or completely, to serve various purposes **(Figure 4)**.



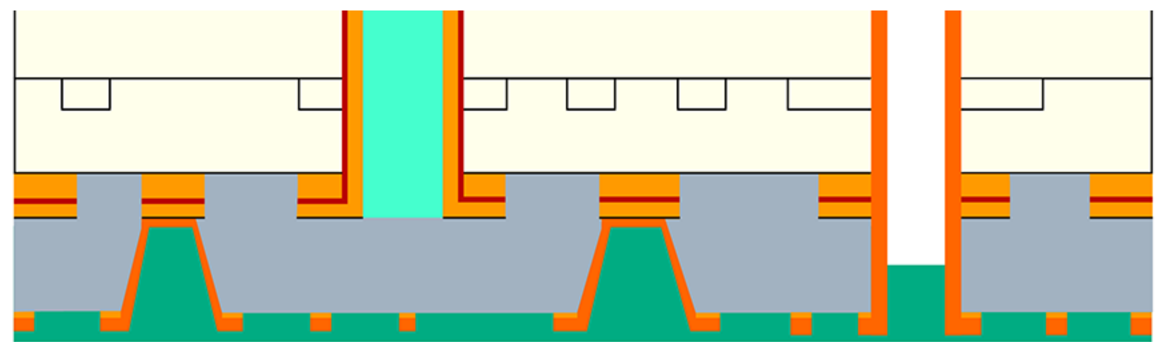


Figure 4. Example diagrams of via tenting and plugging.

Via tenting refers to covering a via with solder mask, whether on one side or both sides. This helps protect against unintended solder bridges or solder wicking occurring during assembly. Tented vias are not to be used with via-in-pad, but they are typically used close to solder pads as an extra precaution against unintended bridging.

On the other hand, via plugging involves filling the via with a nonconductive material to completely seal it (typically without capping). This technique is particularly useful for via protection against environmental factors, such as moisture and dust. Plugged vias will still have an exposed copper ring on the top layer, but solder mask can be used to conceal the leftover copper on the surface.

Direct Metallization

The past decade has seen a notable shift in the preferred method for plating via holes in PCB manufacturing. For many years, electroless copper plating was the dominant approach employed by most PCB manufacturers. This technique involves chemical deposition of a thin layer of conductive copper into the drilled through-holes of multilayer PCBs before electroplating. While the traditional electroless copper process is well established and known for its reliability in creating interconnects, it consumes large amounts of water and energy, uses toxic chemicals and is a significant source of hazardous waste, raising serious environmental and health concerns.

In response to these challenges, innovative electrolytic alternatives to electroless copper plating, often referred to as direct metallization processes, have emerged. Direct metallization

involves direct deposition of a thin metal layer onto the inner surface of holes, without the need for prior electroless (chemical) plating. Compared to electroless copper plating, direct metallization provides shorter cycle times, improved hole wall reliability, while dramatically reducing chemical and water usage. Simultaneously, direct metallization processes can reduce costs, energy consumption and carbon footprints.

Direct metallization technologies are transforming the way conductive electrical pathways are fabricated within PCBs and support HDI technologies that produce significantly finer traces with tighter spacing.

For instance, we recently manufactured a 20-layer HDI PCB for a commercial aerospace company. We used a modified semiadditive process (mSAP) as an alternative to subtractive etching to form the conductive circuit patterns. This approach offered better pattern geometry, permitting finer traces and tighter spacing, as narrow as 3 mils (75µm). Having incorporated mSAP helped reduce layer count and cost without compromising signal integrity or reliability.

The market for HDI solutions reflects a continuing opportunity for PCB designers and fabricators. And on the near horizon is ultra HDI (UHDI) PCBs, which are defined as products with conductor widths and spaces of less than 50µm and microvia diameters of less than 75µm.

Those that embrace the trend for smaller, sleeker and more functional devices can position themselves as agile leaders in the HDI (and UHDI) PCB fabrication industry and realize the rewards of participating in groundbreaking innovations while remaining competitive and profitable.

Note: PCEA will sponsor an all-day forum on UHDI & Substrates: Design to Package during PCB East in June in the Boston suburbs.

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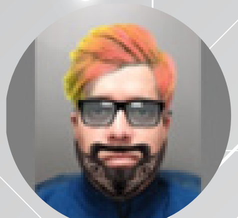

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ASSEMBLY **SERVICES**

Windy City Tour

Chicago's EMS companies place an emphasis on responsiveness.

by TYLER HANES

While major manufacturing centers in Mexico, plus the more than 250 EMS companies in the Silicon Valley, draw much of the attention when it comes to electronics assembly, the greater Chicagoland area is alive and well.

CIRCUITS ASSEMBLY visited a trio of EMS companies last fall, each of which specializes in different niches. The firms, which include Imagineering, BEST and BESTProto, have taken different paths to success, but they have a common recognition of the need for responsiveness in a demanding customer environment.

Imagineering: From Fabrication to Assembly

Our first stop was Imagineering. The 38-year-old company offers fabrication services through partners in Taiwan, China and the US, and began offering assembly in 2011 as an additional service for customers.

Originally a printed circuit fabricator, Imagineering in 2013 installed its first in-house SMT line, which permitted the company to maintain its strict quality standards, CEO and managing partner Khurrum Dhanji said.

Figure 1. Khurrum Dhanji has led Imagineering's expansion into SMT.

"We wanted to be sure we could maintain the quality clients were used to," he said.

Dhanji ran the initial SMT line himself after visiting Mycronic to get an up-close look at the process, and within the first year of offering in-house assembly, Imagineering had a handful of employees to work the line, he said.

"We rapidly grew assembly in the first three to five years," Dhanji said.

Today, the company has 70 employees spread between two locations, a 27,000 sq. ft. assembly facility in the Chicago area and its 15,000 sq. ft. headquarters in Fort Worth, TX, which was added in April of 2021 and offers assembly services.

The company's revenue split is currently around 60% fabrication and 40% PCBA, and the assembly side of the business has continued to grow more even with the fab side, Dhanji said. Part of that growth has been spurred by the company's fabrication customers turning to Imagineering for assembly.

Figure 2. Imagineering's assembly services have grown to include four SMT lines at its facilities in Elk Grove Village, IL, and Fort Worth, TX.

The company offers consignment assembly using a customer's pre-made parts, but it also has a large network of PCB suppliers that permit Imagineering to offer lower prices on full turnkey projects – from ordering the components and manufacturing and assembling the PCBs, to testing and shipping them out.

Imagineering has a lot of flexibility in its manufacturing capacity and can offer customers the options of producing as little as one piece per day up to thousands per day, Dhanji said.

In 2023, Imagineering had around 1,500 customers, and averaged around 50 unique part numbers per day after having 10,000 unique part numbers in 2022.

The company doesn't provide design work, but its engineering team provides DfM support

and can make minor changes to Gerber files sent by a customer to make sure any issues are resolved in the pre-fabrication stage.

"Customers really like the engineering support," said Roy.

He said the engineers receive each job the same way, with no idea of the priority of the work or what they're helping with, and that allows them to provide the same level of service to each customer, big or small.

"They treat every single job as it is the most important job for our customers," Roy said. It may explain why the company took home five CIRCUITS ASSEMBLY Service Excellence Awards in 2023.

Imagineering's network of fabrication suppliers encompasses all existing substrates on the market – including flex and rigid-flex – and the company performs all assembly to class 3 standards, Dhanji said.

Through the Great Recession, the Covid-19 pandemic and the current post-pandemic recession, Imagineering has continued to grow. Dhanji said he wants to see the company continue that growth path and navigate through the wave of consolidation that has been taking place in the US PCB industry and will likely continue in coming years.

While he had no specific plans to share, he said the company is always on the lookout for opportunities to see its assembly business blossom.

"My goal is to consolidate PCB assembly in the US," Dhanji said.

BESTProto: When You Need It Quick'

A repeat winner of the CIRCUITS ASSEMBLY Service Excellence Awards (including the recipient of the Highest Overall Customer Rating), Chicago-based EMS provider BESTProto prides itself on its flexibility.

The Tier IV EMS firm specializes in prototype assembly, and can handle bookings ranging

from a single piece to a couple thousand, with most orders numbering around 20 pieces, said director of business development Garth Cates.

The firm averages around 50 customers a year at its 17,000 sq. ft. facility in South Elgin, IL, and its 15 employees run one shift on its three SMT lines.

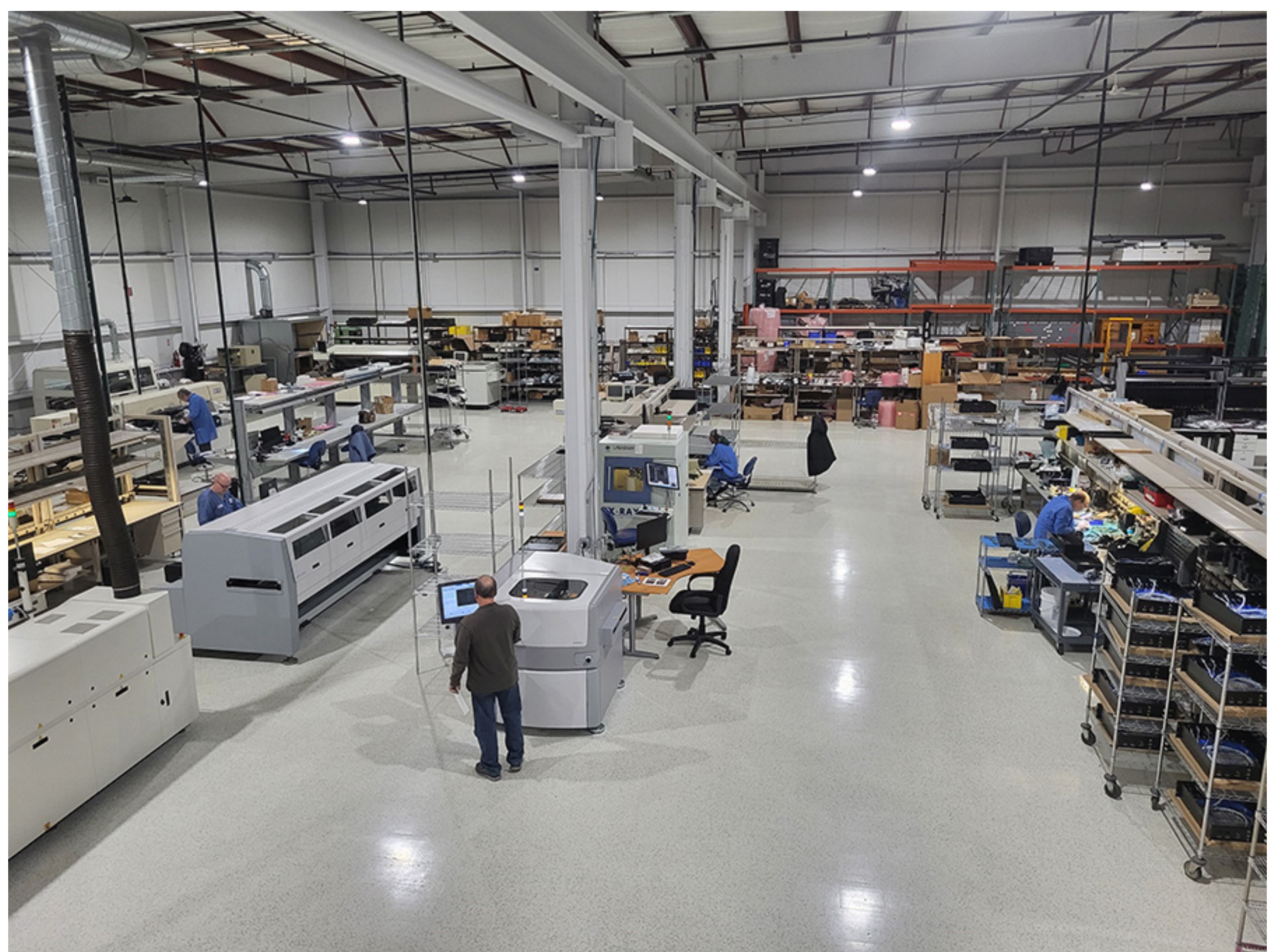


Figure 3. BESTProto's 17,000 sq. ft. facility in South Elgin, IL includes three SMT lines.

BESTProto offers five-day, 10-day and 20-day services – but has also done one-day turns when customers needed it, Cates said.

That flexibility also applies to customers that have their own parts or need their supplier to source them.

“We will do 100% consignment to 100% turnkey and anywhere in between,” Cates said.

While the company doesn't offer its own design and layout services, it has industry contacts and can make introductions for those services. In addition, BESTProto performs documentation verification and can provide DfM and DfT feedback to customers to help the process.

"It's almost rare that we don't catch a problem," he said.

BESTProto can provide SMT placement of components down to 0201 sizes, as well as through-hole assembly, LGAs and QFNs and BGAs down to 0.4mm pitch components. It also offers wire and cable assembly and box build services.

Figure 4. BESTProto offers five-day, 10-day and 20-day assembly services.

Everything assembled by the company goes through a thorough inspection and testing process, including x-ray inspection and AOI.

When we visited in November, the supply chain had been improving – although some ICs still had some long lead times – but the challenges of the pandemic provided an opportunity for BESTProto to flex its knowledge and connections to dig up some tricky materials, Cates said.

"We've been pretty good at coming up with materials that others can't seem to find," he said.

BESTProto is more of a boutique shop than the average mail order "throw it over the wall" provider, and offers plenty of customer assistance and a personal touch coupled with speed and accuracy, he said.

"If you need it done quickly and need it done right, that's what we do," Cates said.

BESTProto has seen good growth in the past couple of years through the pandemic and ensuing recession, and the company is looking to continue that path and diversify its customer base.

"2023 has been excellent, and we're looking to keep going and maintain that momentum," he said.

BEST: 'Solder University'

Our final stop was to BEST, which offers PCB rework and repair and solder training courses out of its 30,000 sq. ft. facility in Rolling Meadows, IL, and it recently added a new facility in Lansing, MI, to host more training courses.

The company's 26 personnel include 15 full-time employees who remove and replace components and perform board-level repairs of any physical damage to populated and unpopulated boards – including flex and rigid-flex. One of its specialties is also the ability of complex BGA repair and reballing, said president Nash Bell.

Figure 5. BEST president Nash Bell came aboard the firm a year ago after a buyout of its founders

The company sometimes gets requests from individuals for rework or repair for consumer devices, but for now, BEST has stuck with working directly with manufacturers.

Another service offered is salvaging, and demand for that really picked up during the pandemic and the supply chain issues that arose – including some customers who needed to get one specific part off old boards to be used in new ones, Bell said.

With the easing of the procurement issues, that service has seen a drop in demand, but is still getting business, he said.

“We still get them, but a lot lower than the prior two years,” he said.

BEST’s master IPC Training and Solder Certification courses are also gaining momentum as people see the benefit in learning to solder or improving their skills to keep up with new technology, Bell said.

Figure 6. BEST's 26 employees specialize in repair and rework at the solder and board levels.

Before adding the Michigan location, the company had been traveling directly to companies using its Mobile Training Center or renting out hotel conference rooms to host classes, but securing a set location through 2024 should enable the continued growth of BEST's training business, he said.

Bell joined the company at the beginning of 2023 after a new ownership group took over operations, and one point of emphasis since the changeover has been growing a culture of continuous improvement, he said.

"We really have grabbed onto the idea that we're always growing and learning," Bell said.

He said employees are encouraged to cross-train between the different services offered by the company to grow and refine their skills, and with the training resources already at hand within BEST, it would be a waste to not allow employees to take advantage.

"We came into a really great product here," he said. "It's almost a Solder University."

Right now, BEST's revenue mix is around 50% from operations, 35% from training and 15% from its products like repair kits and stencils that are available for purchase, Bell said.

Figure 7. Along with its rework and salvaging services, BEST offers x-ray and optical inspection.

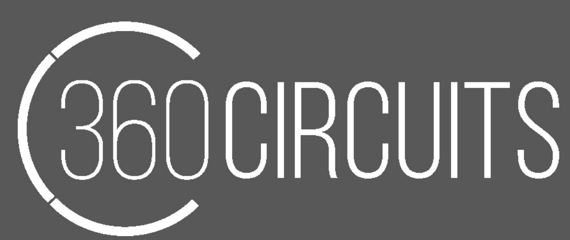
He said training and products have seen growth over the past year, and continuing that path is important to make sure the company does not grow overly reliant on one department.

"I'm very happy with how things are going," he said.

Bell said he and the rest of the company have a lot of excitement for 2024's prospects, and he wants to see BEST grow into the expert resource that people think of first when they need help.

"We want to be the best of the best," he said. "Almost the Navy SEALs of soldering."

TYLER HANES is managing editor of CIRCUITS ASSEMBLY/PCD&F; tyler@pcea.net.



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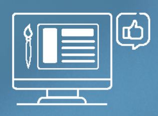

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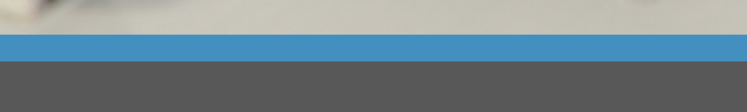

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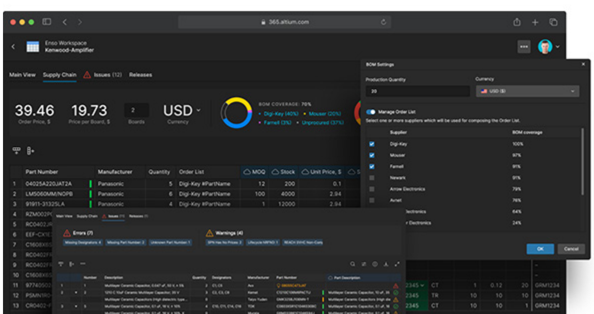

ALTIUM 365 BOM PORTAL

BOM Portal within the Altium 365 platform is designed to enhance collaboration among engineering and procurement teams and offer a unified approach to managing bills of materials (BoMs). Gives users visibility into upcoming designs before their release to catch issues early in the development process. Provides access to real-time, detailed component information from Octopart, S&P Global (formerly IHS Markit), SiliconExpert, and soon Z2Data, and equips users with tools for efficient BoM management, including automatic data enrichment with part details and lifecycle information. Proactively identifies potential supply chain disruptions and component obsolescence.

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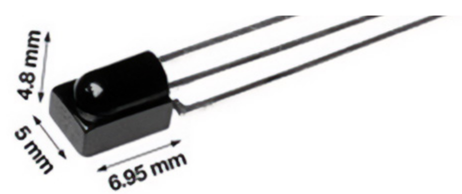


VISHAY IR RECEIVER MODULES

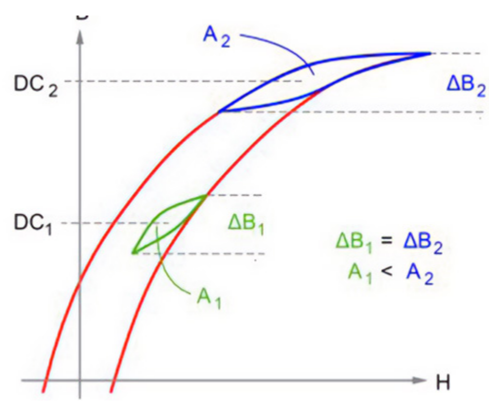
TSOP18xx, TSOP58xx, and TSSP5xx series of IR receiver modules now feature the company's latest in-house IC technology. Offered in Minicast packages and provide drop-in, plug and play replacements for existing devices in the series while offering 50% lower current consumption, improved ESD robustness to 12kV, a wider supply voltage range from 2.0V to 5.5V, 20% higher dark-ambient sensitivity and improved performance under strong DC light. Consist of a photodetector, preamplifier circuit, and IR filter in a single package, and feature reduced current consumption over a wider voltage range to increase battery life in mobile devices while being robust under bright sunlight to enable outdoor applications.

TSOP18xx and TSOP58xx series are designed for IR remote control in televisions, soundbars, video game systems, set-top boxes (STBs), appliances, air conditioners, and more. Provide increased robustness against disturbances such as IR emissions from different kinds of lamps and are insensitive to supply voltage variations and ripple noise. Are available with carrier frequencies from 30kHz to 56kHz and in six automatic gain control (AGC) versions for short and long burst codes.

TSSP5xx series delivers long range proximity and presence sensing to 2m and can be paired with the TSAL6200 emitter for light barrier applications to 8m. Sensitive to a carrier frequency of 38kHz – and offering a peak sensitivity of 940nm – are said to be ideal for sensing the distance to objects for toys, drones and robots, object approach detection for the activation of displays, user consoles and garage door light barriers.

Vishay Intertechnology

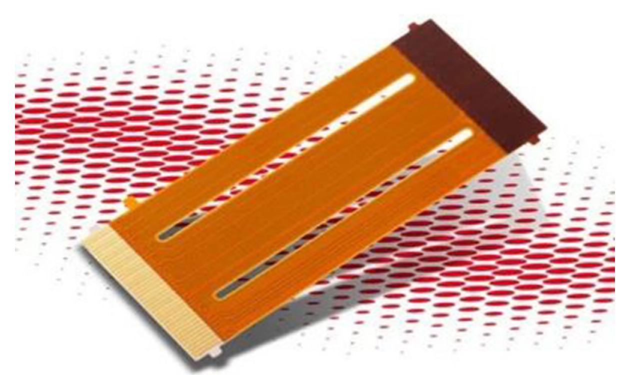
vishay.com



WÜRTH REDEXPERT DESIGN PLATFORM

Redexpert online design platform now includes the effects of DC bias on the AC losses. AC core losses increase when the AC ripple is DC biased, which is the normal operating condition for power converters like the buck regulator, and new features include the ability to trace the effect of DC bias resulting in more accurate AC losses.

Würth Elektronik
we-online.com



YAMAICHI YFLEX FPC

YFLEX flexible PCB is now also available as a high-heat resistant version for extreme environments. Meets requirements for automotive, semiconductor manufacturing and test and measurement technology. Features an improved insulating layer that has increased adhesion from the use of a special cover layer. Retains electrical properties for over 3,000 hr. under temperatures of up to 150°C. Maintains continuity resistance within a rate of change

of ±10% and insulation resistance is 500MΩ or higher. Can be produced in both single-layer and double-layer configurations, and insulation substrate base can be selected from liquid crystal polymer (LCP) or polyimide (PI). Also features a reinforced GND design that is suitable for high-heat-resistant and for noise-resistant FPC applications.

Yamaichi Electronics
yamaichi.de

CA

DELVITECH 3IS AOI

3iS AOI system is designed to ensure scalability and inspection repeatability on all production lines by deploying identical hardware and software technology for each inspection phase. Uses neural networks to identify complex components and provides the capability to analyze the soldering process as well as the management of automatic adaptation to allow use of a mix of components in production. Self-programming feature allows user to speed up and increase quality of programming process. Predictive analysis anticipates possible product failures. Has MES interfaces for Delvitech SPC and user management tool integration.

Delvitech
delvi.tech

EXCELITAS OMNICURE S1500 PRO CURING SYSTEM

OmniCure S1500 Pro UV spot curing system is an enhanced version of the OmniCure S1500. Includes lamp-based light source leveraging Intelli-Lamp 2.0 technology to deliver optimized lamp life (2,000 hr. guaranteed) while maintaining optimum performance. Is also equipped with StepCure 2.0 to enable precise programming of multiphase curing profiles directly from the system with a simple user-friendly interface, and a selection of user-interchangeable optical filter and lamp types provides flexibility for a range of applications. Also features USB Type B and SD card compatibility to allow seamless connectivity and data storage, plus a 4.3" high-resolution LCD touchscreen display interface to simplify operations. Additional features include identical optical output power and spectrum to previous generation OmniCure S1500, PLC control with one programmable PLC output channel that is configurable to simplify more advanced workflows, NFC (near field communication) for advanced process control with NFC-enabled keycards (Admin, Supervisor), and is cleanroom ready with dedicated duct attachment area that simplifies connections for cleanroom use.

Excelitas Technologies

excelitas.com

HITACHI HIGH-TECH XRF ANALYZER

FT210 analyzer includes a proportional counter detector for routine measurements of common platings and incorporates features designed to enhance high-volume testing needs. Includes the largest-in-industry sample view, wide view camera, auto-focus and auto approach, and a smart recognition feature called Find My Part that automatically recognizes features to be measured and chooses correct analytical method. Also includes an updated version of FT Connect software for all FT200 Series models, with enhanced usability features for reporting, creating calibrations and data handling. Expands the RoHS screening capabilities of the FT230 and is compatible with new and existing instruments.

Hitachi High-Tech Analytical Science

hitachi-hightech.com

STACKPOLE TMJ JUMPER CHIPS

TMJ series electrically isolated jumper is said to provide thermal conductivity with low capacitance and high insulation resistance between terminals. Utilizes an aluminum nitride substrate to provide thermal conductance up to 216mW/°C while maintaining isolation for components that can't be electrically grounded.

Stackpole Electronics

seielect.com

YAMAHA VP-01G-Y SPI

VP-01G-Y solder paste inspection system uses advanced algorithms in 2-D and 3-D modes to aid focusing and contour extraction. Analysis includes 3-D solder-paste and adhesive inspection, foreign-matter detection and board warpage to assist screen-printing, dispensing, and component-placement processes. Compensates for board warping and handles inspection of flexible PCBs, and advanced features include a ring light source that provides 360° illumination to ensure reliable inspection and accurate three-dimensional measurements. Features one-head design to permit continuous, changeover-free inspection, with 25µm, 20µm, or 15µm lens and software-controlled multiple-resolution switching for additional settings. Resolution is switchable for each visual field, enabling optimum throughput when inspecting boards with areas of high interconnect density and mixed-size parts including ultra-small components down to 0201 and 03015 SMDs. Features board-size range from 50mm x 50mm to 510mm x 510mm to fulfil production demands across sectors including automotive, medical, industrial and consumer electronics manufacturing.

Yamaha Robotics

yamaha-motor-robotics.eu

TECHNICAL **ABSTRACTS**

In Case You Missed It

Solder Materials

"Effect of Sb and Ag Addition and Aging on the Microstructural Evolution, IMC Layer Growth, and Mechanical Properties of Near-Eutectic Sn-Bi Alloys"

Authors: Hannah N. Fowler, *et. al.*

Abstract: Low-melting-point Sn-Bi solder joints (melting point: 139°C) show remarkable resistance to damage accumulation during aggressive thermal cycling. In this study, the authors used isothermal aging at 85°C of near eutectic Sn-Bi solder joints to determine the effect of Sb in solid solution and Ag_3Sn intermetallic on microstructural evolution and the resulting mechanical properties to explain the thermal cycling behavior. Most importantly, the Sb in solid solution in these alloys resulted in higher strength and improved creep resistance compared to eutectic Sn-Bi. In contrast to SnPb and SnAgCu Pb-free alloys, all the near-eutectic SnBi alloys tested showed significant age hardening. In both unaged and aged conditions, both Sb and Ag additions individually increased saturation stress of the eutectic SnBi solder joint, but Ag had a more significant effect. However, when both Sb and Ag were added to eutectic Sn-Bi, the saturation stress was lower than when 1 wt.% Ag alone was added. In terms of relative behavior, the Sb-free 42SnBi1Ag aged for 250 hr. had the highest saturation stress of all tested alloys, while as-reflowed eutectic SnBi had the lowest saturation stress. These results suggest that the alloy design strategy for SAC alloys; i.e., assuming that the effects of individual alloying elements are additive and independent, is not valid when Sb is added to SnBi low-temperature solder. (*Journal of Electronic Materials*, December 2023, https://doi.org/10.1007/s11664-023-10866-0)

Stencil Printing

"Effect Of PVD-Coated Wall Aperture Roughness on the Life Span of Fine-Pitch Stencil Printing"

Authors: Mohamed Sunar, *et. al.*

Abstract: This paper aims to investigate the effect of physical vapor deposition (PVD)-coated stencil wall aperture on the life span of fine-pitch stencil printing. The fine-pitch stencil used in this work is fabricated by electroform process and subsequently nano-coated using the PVD process. Stencil printing process was then performed to print the solder paste onto the PCB pad. The solder paste release was observed by solder paste inspection (SPI) and analyzed qualitatively and quantitatively. The printing cycle of up to 80,000 cycles was used to investigate the life span of stencil printing. The finding shows the performance of stencil printing in terms of solder printing quality is highly dependent on the surface roughness of the stencil aperture. PVD-coated stencil aperture can prolong the lifespan of stencil printing with an acceptable performance rate of about 60%. (*Soldering & Surface Mount Technology*, January 2024, https://doi.org/10.1108/SSMT-05-2023-0025)

Wave Modeling

"A Segmentation Approach for Predicting Plane Wave Coupling to PCB Structures"

Authors: Shengxuan Xia, *et. al.*

Abstract: Evaluating the far-field radio frequency (RF) susceptibility of electronic devices often depends on extensive testing or full wave simulations. These methods are effective when complete system information is available but require substantial time and resources to evaluate a large number of variations in system configurations, where trace routings, IC package styles, trace terminations, arrival angle, and polarization of incoming wave, etc., vary from one configuration to another. The goal of the study was to develop simulation techniques for studying the statistical characteristics of coupling to typical PCB structures. Simulation time can be reduced by breaking the structure into small segments, determining

the coupling and transmission characteristics of each segment analytically or in a full-wave model, and then determining the coupling to the overall structure by assembling the individual segments in a circuit simulation. Reusing premodeled segments of commonly occurring structures (e.g., IC package, trace, etc.) allows estimates with minimal computational effort even for a complicated PCB design. Simulation time is estimated to improve by a factor of 40 or more over traditional full-wave modeling using this approach. This methodology enables the analysis of statistical electromagnetic coupling to random PCB geometries. (*IEEE Transactions on Electromagnetic Compatibility*, January 2024, 10.1109/TEMC.2024.3349911)

Wireless Power Transfer

"Improved Design of PCB Coil for Magnetically Coupled Wireless Power Transfer"

Authors: You Fu, *et. al.*

Abstract: In recent years, wireless power transfer (WPT) has progressed rapidly in both theory and commercialization. However, existing research into WPT coil design for low-power devices to mitigate the coil offset is limited. A dual-layer printed circuit board (PCB) structure is proposed in this paper to mitigate the coil offset while retaining manufacturing simplicity for practical uses. Specifically, the impacts of key geometric parameters on the coil quality factor and coupling coefficient are analyzed through models and simulations. Equivalent PCB coils were formed for mutual inductance models, and four basic compensation circuits were analyzed. The impacts of changes in coil thickness, line width, turn spacing, and number of turns on the quality factor of PCB coils were analyzed with a fixed outer diameter of the coil. Eleven types of PCB coils were manufactured to verify the simulation results. The offset transmission efficiency can reach 46.6% with an output power of 14.4W. The PCB coil with improved design could offer remarkable improvements in the WPT system for low-power electronic devices. (*Electronics*, January 2024, https://doi.org/10.3390/electronics13020426)