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April 2024

CIRCUITS ASSEMBLY

Beating the Heat

Are Thermal Vias Holding You Back?

- **HDP** Looks to its Past – and its Future
- **AI's Effects** on the Electronics Industry
- Reviewing Solder **Paste Mixing** Methods

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APRIL 2024 • VOL. 41 • NO. 4

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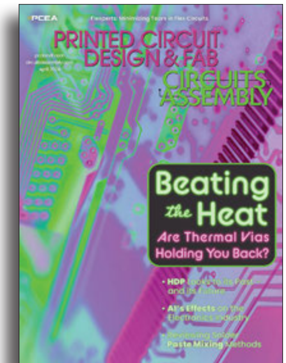

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PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by Printed Circuit Engineering Association, Inc., PO Box 807 Amesbury, MA 01913. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

Mega Mergers, Mega Headaches?

ARE THE DAYS of the mega-merger over, or are we just about to experience a new wave?

A good case could be made for either. Which we should root for is another matter.

In Europe, GPV's merger with its slightly larger competitor Enics in late 2022 created a $1.5 billion entity, sending the combined entity barreling up the CIRCUITS ASSEMBLY Top 50 list. Then consider Kontron and Katec, another rollup that now exceeds a billion dollars plus in sales. When it comes to M&A, Europe at least seems to have it "going on."

Asia isn't playing second fiddle. China Electronics Corp., one of the mainland's largest entities, helps underwrite Nanjing Huadong Electronics, which bought top 15 EMS company TPV Technology in a reverse merger in 2021. TPV's annual revenues are in the $7.5 billion range. That's serious cabbage.

If we look back to the late 1990s, there was an extended period of end-market sluggishness. And what we saw was venture capital showing up, taking advantage of lower valuations and the "old guard" (read: the first generation of board shop and EMS assembly owners) looking to cash out.

Think back to 2002, when Sanmina bought (the much larger) SCI in a $6 billion stock swap that resulted in a then-record $14 billion EMS/PCB company. Flextronics's purchase of Solectron was another good one. It resulted in a $30 billion entity, which even unadjusted for inflation is almost the same size of Flex today.

Celestica had a couple good scores: Singapore-based EMS provider Omni Industries, with its annual revenue of about $1 billion, in 2001, followed a couple years later by Manufacturers' Services Ltd., (MSL), another global EMS, with revenues of over $800 million.

Those deals, and others like them, were often made possible in large part because of the robust market capitalizations of the acquiring companies. (Indeed, the Kontron acquisition of the much larger Katec is reminiscent of the Sanmina-SCI deal.)

What happened next was the inevitable exit strategy. I sat through many a presentation and market analysis session in the 1990s and 2000s, and every one of them, it seemed, reminded business owners and investors to keep the end-game high on their mind. It was as if they were out to convince the partygoers to grab their coats and head for the doors while the hors d'oeuvres were still being passed.

There were lots of IPOs at that stage. Companies that had been only in the tens of millions in revenue just years before were going public. The industry had only a few billion-dollar players at that point, but it didn't seem to stop Wall Street from convincing enterprising owners there were far more riches to be made, and with less risk, if they floated their company on the open market.

We all know what happened next. Not long after the dot-com implosion of 2001, investors fled. Bankruptcies ensued. And the Street didn't give the industry much of a glance for more than a decade.

The PE folks are nothing if not clever at spotting undervalued assets, however. And so long after the industry had been lulled to sleep with little hope of new investment and most of the new money had holed up in Asia, in particular China and Taiwan, here we are again. Investment capital is everywhere we look. There are more financial assets tied up in the electronics manufacturing industry today than ever before. In fact, it's not even close.

Market watchers Lincoln International reports that fewer than 10 M&A deals were completed last year, and only a couple by larger tier firms. In my estimation that significantly understates what's really happening, but the actual figures are less significant than the basic trends. At a certain point the PE firms are going to run out of money or interest or time or some combination thereof, and there won't be anyone else left to sell to. And that's when the public offerings will start again.

Maybe they are starting already. The EMS industry has added a few new public players in Asia in the past few years, although they were offset in part by delistings in Europe (Neways, Katek).

I'm not considering BYD's purchase of Jabil's mobility unit as a milestone, because from my perspective that's a divestiture, not a consolidation. In the transfer of assets among firms, no newly single (and larger) entity was created.

We industry-watchers love deals because they give us the opportunity to gain better insight into what's truly going on behind the corporate marketing collateral and press releases. But in truth, they also create issues for the industry in that there's always the potential that the next downturn will lead once again to mass exodus. Boom/bust cycles aren't good for anyone, be they investors or personnel. Boom/bust cycles that are exacerbated by investors heading for the exits are that much harder to recover from. So perhaps we shouldn't wish for the days of the billion-dollar marriages.

But they sure were fun.

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P.S. See us at the Del Mar Electronics Show in San Diego on April 24, where our San Diego chapter is sponsoring a pair of talks on PCB design and CAD library development. Thanks to Siemens Digital Industries and PCB Libraries for sponsoring this event.

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Cadence to Buy Beta CAE Systems for $1.2B

SAN JOSE, CA – Cadence Design Systems will buy Beta CAE Systems, a maker of software for analyzing car and jet engine designs, for $1.24 billion in cash and stock, the company announced.

Cadence said it will pay for the acquisition with around $744 million in cash and the rest in stock, and while it will take on debt to pay for the deal, it will pay that down with cash generated from operations.

Beta CAE's software is used to analyze designs in automotive and aerospace industries, with customers such as Honda, General Motors and Lockheed Martin. Over the last several years, Cadence has expanded its system analysis portfolio to build out a comprehensive multiphysics platform including electromagnetics, electrothermal and computational fluid dynamics solutions, and with Beta CAE, Cadence will enter structural analysis, the largest system analysis segment, the company said.

"Cadence entered the multiphysics space several years ago through organic innovation and acquisitions. This strategic acquisition reaffirms our commitment to continued growth in this critical domain," said Anirudh Devgan, president and CEO, Cadence. "Combining our computational software expertise with Beta CAE's rich technology and talent will enable us to offer a more comprehensive portfolio to customers, while opening significant new opportunities for Cadence by tapping into the structural analysis segment. These solutions are particularly important in automotive, where convergence of electrical and mechanical designs is further driven by an increasing shift toward electric vehicles, requiring deeper design team collaboration in integrated workflows."

The transaction is expected to close in the second quarter of the year and Cadence expects Beta CAE to contribute about $40 million to its 2024 revenue, the company said.

Rogers Announces New Facility in Mexico

CHANDLER, AZ – Rogers Corp. has signed a lease on a factory in Monterrey, Mexico, for advanced busbar manufacturing and engineering services.

The first phase of the new site is slated for completion in late 2024 and continues Rogers' manufacturing footprint strategy of supporting customers in the regions where they operate, the company said.

"We are excited to expand our presence in North America to better support our global customers and the growing EV/HEV and renewable energy markets in this region. Our new factory in Monterrey will enable us to better support our customers with deeper technical collaboration, and local prototyping and supply capabilities that reduce lead times and improve service levels," said Jeff Tsao, Advanced Electronic Solutions (AES) senior vice president and general manager.

TTM to Expand in Ohio

NORTH JACKSON, OH – TTM Technologies is planning an expansion at its PCB manufacturing plant here that will add 50 jobs to the existing 200 at the facility.

TTM Technologies' investment will help produce essential components for many industries that have a large presence in the region, including aerospace, automotive, medical devices and industrial controls and automation, said Team NEO, an economic development organization for Northeast Ohio that worked with TTM to receive a tax credit for the expansion.

"TTM Technologies is pleased to bring this expansion of capability and opportunity for workforce growth to North Jackson, Ohio. The engagement by Team NEO, the Ohio Department of Development and JobsOhio to understand our extensive workforce training requirements was invaluable in our decision to grow this facility," said Phil Titterton, COO, TTM Technologies. "This successful process has allowed all involved to develop a better understanding of the importance and criticality of US-made printed circuit boards."

Ge-Shen Acquires Stakes in 3 EMS Firms

KUALA LUMPUR – Malaysian contract manufacturer Ge-Shen will purchase a 40% stake in EMS firm Local Assembly to expand its presence in electronics manufacturing.

The RM48 million ($10.2 million) transaction will be partially funded via proceeds from a private placement exercise, Ge-Shen said in an exchange filing.

"The board believes the acquisition will complement the existing business, enabling cross-marketing of products with diverse designs and specifications to a broader clientele. This will also drive synergistic value across the company through shared technology know-how," Ge-Shen said.

Local Assembly is primarily a manufacturer of electronic, electrical, and plastic injection molded components, and a subcontract assembler of electrical appliances and equipment.

The transaction is expected to be completed by the second half of 2024, subject to requisite approvals and barring unforeseen circumstances, Ge-Shen said.

Ge-Shen also signed agreements to purchase 60% stakes each in Amity Research & Development and Amity Technical Services & Consultancy for RM13.5 million ($2.6 million).

Amity Research & Development is an engineering and consultancy services provider for the electronics industry, and Amity Technical Services & Consultancy is a manufacturer of PCBAs, box builds and cable and wire assembly.

Ge-Shen said it expects the transaction to close by the third quarter of 2024.

"This proposed acquisition will expand Ge-Shen's scale of operations and facilitate the group's presence in such a market. It is also in line with the group's objective of acquiring strategic stakes in companies involved in high value-added industries with potential for future growth," the company said.

Cicor Acquires TT Electronics IoT Solutions

BRONSCHHOFEN, SWITZERLAND – Cicor Group in March announced its acquisition of TT Electronics IoT Solutions and its three production sites in the UK and China.

Cicor is paying GBP20.8 million ($26.5 million) on a cash and debt-free basis, subject to normal working capital adjustments. The transaction is expected to close in the first quarter of 2024, has received all required regulatory approvals and is subject to customary closing conditions.

The sites acquired from TT Electronics will combine with Cicor's own Axis Electronics and STS Defence to create a new leader in the UK EMS market and make Cicor a European market leader in the production of high-end electronics for aerospace and defense applications, the company said in a release announcing the transaction.

TT Electronics employs more than 500 staff at its sites in Hartlepool and Newport in the UK and Dongguan in China and has a total production area of around 25,000 sq. m. In the last financial year, the company reported sales of GBP70 million ($89 million).

The acquired production sites provide much-needed growth reserves for local production in the UK, Cicor said, and the production site in Dongguan will be integrated into its Asian production network.

Celestica to Expand TX Operations, Add 155 Jobs

RICHARDSON, TX – Celestica has signed an economic development deal here that will see the company redevelop a 30,000 sq. ft. office into a manufacturing facility and add 155 jobs.

The expanded facility will produce equipment based on AI learning systems for Celestica's US-based customers across multiple industries.

As part of the agreement, Celestica must invest at least $5.5 million into converting the newly leased space, which is located near its current operations in Richardson, and the city government will pay a total of $250,000 as the company reaches certain milestones. Celestica must also create 155 new jobs with an average annual salary of $67,200 at the expanded facility.

"Richardson has proven to be a great location for us to expand to meet unique customer demands," Robert Paiva, general manager of Celestica's Richardson operation, said in a release. "Between its educational advantages and built-in infrastructure, we are excited about growing in the community and benefiting from the competitive advantages this location offers."

"Celestica's growth in our community further strengthens the work we are seeing here for AI learning systems," said Richardson Mayor Bob Dubey. "This expansion builds on the growth we are seeing for this type of work and adds to the synergies available in Richardson for global technological innovators like Celestica."

Altium Acquires Valispace Software Platform

SAN DIEGO – Altium has acquired Valispace, a systems and requirements engineering software platform, for $15.6 million.

Valispace's capabilities in Systems and Requirements Engineering will complement the Altium 365 cloud platform for product and electronics design, the company said in a release announcing the acquisition, and together the solutions connect electronics hardware design and development with systems engineering, encompassing everything from initial requirements definition to PCB design and verification.

Altium's experience in developing tools for thousands of engineers with essential electronics design software will ensure that the Valispace team can continue to bring the best collaborative and AI-assisted systems and requirements experience to engineers, the company said.

"We're grateful for everyone who has supported and encouraged us on this journey, amongst others our family, friends, and investors," Valispace said. "And we're now excited to, together with Altium, continue our mission of empowering engineers to build great products, accelerating the path to the future in which new technologies and products improve people's lives."

Scanfil Updates Growth Strategy, Outlines New Business Segments

OULU, FINLAND – Scanfil in March announced a new growth strategy that will seek acquisitions, as well as a division into three new business segments.

Over the past three years, the company has pushed for organic growth, but it is now shifting to seek a balance between organic and inorganic growth, and grow through potential acquisitions that would complement its customer base and factory network in Asia (outside of China), North America and Eastern Central Europe.

The company will also work to accelerate its organic growth by moving to three business segments: Industrial, Energy & Cleantech and Medtech & Life Science. Industrial was formed by combining its previous three segments: Advance

Consumer Applications, Automation & Safety and Communications.

"Segmentations clarify roles and further enhance sales growth for all business segments. To drive factory specific sales, we still have local sales people," said CEO Christophe Sut. "We can drive our sales more efficiently by re-organizing it and also incentivizing it through specific customer groups."

Scanfil said it is also placing an emphasis on sustainability and is committed to the Science Based Targets in the short-term 2030 and long-term "Net Zero" 2050, as well as preparing for the Corporate Sustainability Reporting Directive (CSRD) and the European Sustainability Reporting Standards (ESRS) with full speed.

DoD Awards $12M to Ensign-Bickford to Expand PCBA Production

WASHINGTON – Ensign-Bickford Aerospace & Defense received $11.7 million from the Department of Defense to expand PCBA production at its Simsbury, CT, location.

The company received the award through the DoD's Defense Production Act Investment (DPAI) Program, and will use the funds to increase its existing capacity and manufacturing processes to reduce cost and accelerate PCBA production for use in hypersonic weapons.

"This effort is a key component of the DoD's strategy to accelerate the development and fielding of hypersonic systems and deliver cutting-edge capabilities to our armed forces," said Dr. Laura Taylor-Kale, assistant secretary of defense for industrial base policy. "This award also represents another investment in domestic manufacturing in accordance with the National Defense Industrial Strategy to help build a modernized defense industrial ecosystem."

JEDEC Publishes GDDR7 Graphics Memory Standard

ARLINGTON, VA – JEDEC has published JESD239 Graphics Double Data Rate (GDDR7) SGRAM, which offers double the bandwidth over GDDR6, reaching up to 192GB/s per device, and is poised to meet the escalating demand for more memory bandwidth in graphics, gaming, compute, networking and AI applications.

JESD239 GDDR7 is the first JEDEC standard DRAM to use the Pulse Amplitude Modulation (PAM) interface for high frequency operations. Its PAM3 interface improves the signal to noise ratio (SNR) for high frequency operation while enhancing energy efficiency. By using three levels (+1, 0, -1) to transmit 3 bits over 2-cycles versus the traditional NRZ (non-return-to-zero) interface transmitting 2 bits over 2-cycles, PAM3 offers higher data transmission rate per cycle resulting in improved performance.

Additional advanced features include:

- Core independent LFSR (linear-feedback shift register) training patterns with eye masking and error counters to improve training accuracy while reducing training time.
- Doubles the number of independent channels doubles from 2 in GDDR6 to 4 in GDDR7.
- Support for 16Gbit to 32Gbit densities including support for 2-Channel mode to double system capacity.
- Address the market need for RAS (Reliability, Availability, Serviceability) by incorporating the latest data integrity features including on die ECC (ODECC) with real time reporting, data poison, Error check and Scrub, and command address parity with command blocking (CAPARBLK).

"JESD239 GDDR7 marks a substantial advancement in high-speed memory design," said Mian Quddus, chair of JEDEC's board of directors. "With the shift to PAM3 signaling, the memory industry has a new path to extend the performance of GDDR devices and drive the ongoing evolution of graphics and various high-performance applications."

"GDDR7 is the first GDDR that not only focuses on bandwidth but addresses the market needs for RAS by incorporating the latest data integrity features that allow GDDR devices to better service existing markets such as cloud gaming and compute and extend into new applications such as AI," said Michael Litt, chair of the JEDEC GDDR Subcommittee.

Jinlu Electronics Begins $320M Expansion Project

QINGYUAN, CHINA – Chinese PCB fabricator Jinlu Electronics has begun construction on a 2.3 billion yuan ($320 million) expansion project that will add an additional 3 million sq. m. of production capacity for multi-layer rigid boards and high-density interconnect boards.

The company purchased approximately 63 acres adjacent to the company's existing factory in the Guangdong Qingyuan High-tech Industrial Development Zone, and plans to build two factories, a wastewater station and chemical warehouse, and worker dorms.

Jinlu said the project will be constructed in three phases, with construction and production at the same time. Over the planned 60 months for construction, the first phase construction period (including preliminary planning) is expected to be 18 months, and is expected to be put into operation in July this year, with a planned production capacity of 1.2 million sq. m.

The second phase construction period is six months, and is expected to be completed and put into operation in July 2026, with a planned production capacity of 1.2 million sq. m. The construction period of the third phase is 12 months, with plans to be completed and put into operation in January 2028 with a planned production capacity of 600,000 sq. m.

Toppan Plans Singapore Chip Package Substrate Plant

TOKYO – Toppan Holdings will build a semiconductor package substrate plant in Singapore, with plans to begin operations at the end of 2026.

The company said it anticipates the factory to create 200 jobs, with a capacity that will likely increase in line with demand and a total investment of 100 billion yen with the planned growth. Toppan will bear the majority of the initial 50 billion yen investment of the plant, while capacity expansions later could receive financial support from the company's main customer, Broadcom, the company said.

Toppan currently produces package substrates only at its plant in central Japan's Niigata prefecture. The planned Singapore factory will be near many back-end processing contractors that handle semiconductor assembly and testing in Malaysia and Taiwan. The company looks to boost its overall substrate production capacity 150% by fiscal 2027 compared with fiscal 2022 by expanding the Niigata facility and opening new facilities.

Apple Acquires AI Inspection OEM

WATERLOO, ON – Apple has acquired artificial intelligence startup DarwinAI as it looks to add technology for a push into generative AI, Bloomberg reported. Financial and other terms were not disclosed.

Dozens of DarwinAI's employees have joined Apple's artificial intelligence division, including Alexander Wong, an AI researcher at the University of Waterloo who helped build the business, who joined Apple as a director in its AI group, according to the report. Apple is not expected to maintain the assembly inspection equipment that DarwinAI developed, however.

DarwinAI is a Canadian startup that has developed AI technology for visual inspection of components, and it also has a stated goal of making AI systems smaller and faster.

During Apple's earnings call in February, CEO Tim Cook said that Apple will share details on its AI work later this year, and during the company's shareholder meeting a few weeks later, he teased that Apple will "break new ground" in generative AI this year.

Kemppi Forming Electronics-Focused Subsidiary

LAHTI, FINLAND – Kemppi Group is splitting its electronics business into its own company, Kemptron, to strengthen its position in the electronics industry.

The newly formed company will manufacture circuit boards, subassemblies, modules, transformers and chokes, Kemppi said, and will operate as a subsidiary of the group.

"Kemptron Oy will strengthen the positioning of Kemppi Group's electronics business and enable business growth," said Jari Takala, general manager of Lahti operations, Kemptron. The company will take into account the specific needs of its customer industries. Kemptron Oy will provide power electronics components for Kemppi Group companies' products."

Once the demerger takes place, Kemptron will be one of the largest contract manufacturers of electronics for power electronics and related control electronics and assembly in Finland, the company said.

Katek to Delist Following Agreement with Kontron

MUNICH – Katek will enter into a delisting agreement with Kontron following Kontron's acquisition of a controlling stake in the company earlier this year.

In January, Kontron announced the acquisition of 59.4% of Katek's shares by its subsidiary, Kontron Acquisition, which is obliged to make a mandatory offer to the shareholders of Katek SE in the coming weeks in accordance with the provisions of the German Securities Acquisition and Takeover Act.

Katek's board has decided that the delisting is in the interests of the company since the stock market listing has lost its significance, and the delisting is therefore advantageous from a strategic and financial perspective, the company said in a release.

As part of the intended delisting agreement, Katek is to apply for revocation of the admission of its shares to the regulated market following publication of the mandatory offer by Kontron Acquisition, which is also to be structured as a delisting tender offer.

Conversely, Kontron Acquisition is to offer the Katek shareholders a consideration in accordance with the statutory minimum price rules as part of this offer. Kontron Acquisition had already announced in its control notification that the price offered in the context of this offer would be EUR15 per Katek share. In addition, Kontron Acquisition is also working on an exchange offer with shares of Kontron AG, its listed parent company, which will be open to Katek shareholders as an alternative.

VDL to Build Vietnam Manufacturing Facility

EINDHOVEN, NETHERLANDS – VDL is planning to build a new manufacturing facility in Vietnam, with an anticipated opening in early 2025.

The company said its global customers have asked for more local production for local markets, and the new facility is part of a larger plan to invest in Europe, America and Asia. VDL Emerging Technology Group, its high-tech cluster, also has Asian locations in Singapore and Suzhou, China.

"Being able to deliver anywhere is a major advantage for VDL's existing and new customers," the company said in a release.

VDL said 60 employees will initially work at the facility when it opens, which is expected to be at the end of the first quarter or beginning of the second quarter of 2025.

Mycronic Makes Optical Fab Acquisition

TÄBY, SWEDEN – Mycronic's Global Technologies division signed an agreement in March to acquire Vanguard Automation, a German company that has developed a technology and automated equipment for 3-D microfabrication of optical interconnects.

Karlsruhe, Germany-based Vanguard Automation's area of expertise complements the Mycronic's die bonding business line and enables the offering of a wider range of die bonding and optical packaging-related solutions, Mycronic said.

"Joining the Mycronic group marks a pivotal milestone for Vanguard Automation in its mission to deploy 3-D nano-printing solutions in volume production for cutting-edge photonic devices," said Vanguard Automation CEO Thorsten Mayer. "We are looking forward to joining forces with Mycronic's Global Technologies division, enriching the offerings for our global customer base."

"Megatrends such as AI, cloud computing and augmented reality are boosting demand for computational power, leading to larger, more energy-intensive data centers," said Magnus Marthinsson, senior VP of Global Technologies, Mycronic. "Vanguard Automation's unique solutions will help speed up optical interconnects and cut energy consumption at the same time."

Vanguard Automation's net sales amounted to EUR5.2 million ($5.6 million) in 2023. The company has 26 employees.

The transaction is expected to be finalized in April 2024, after which Vanguard Automation will form a new business line within the Global Technologies division.

PCD&F

Alpha Circuit installed a **Gardien** G90L flying probe.

Bomin Electronics is expanding its annual PCB production capacity by 1.72 million sq. m., increasing its shipment of high-count multilayer boards, HDI boards and IC carrier boards.

Cadence Design Systems is collaborating with **Arm** to deliver a chiplet-based reference design and software development platform.

Calumet Electronics received an Industrial Facility Tax Certificate to assist in the building of its $51 million advanced substrate factory in Michigan.

PCB distributor **DirectPCB** opened an office in Barcelona, Spain.

Nano Dimension received a patent for technology developed by its DeepCube AI group that enables better training and optimization of decentralized deep learning-based AI models.

NCAB has given its approval to factories specializing in IMS – insulated metal base PCBs.

Rex Electronics broke ground on an HDI PCB production facility in Kunshan, China.

Siflex, a South Korean flexible PCB manufacturer, will supply **Samsung Display** with rigid-flex PCBs for the iPhone 16 OLED.

Varioprint signed a strategic partnership with **Fortify** to introduce RF materials and applications to its European customers.

Ventec Giga Solutions has started offering a refurbishment service for separator plates used in PCB lamination processes.

Wazam New Materials said it plans to invest up to $60 million to build a copper-clad laminate factory in Thailand.

Yijia will invest $20 million to establish a subsidiary in Malaysia to produce rigid and flexible circuit boards and other components for the automotive industry.

CA

Absolute EMS installed its second **Hanwha Techwin** TRNeF103 reflow oven.

AIM Solder named **Cornerstone Technical Marketing** sales representative in California and Nevada and **Solder Connection** representative in Ireland.

CE3S opened a distribution center in Orlando, Florida.

Cutera will pay $19.5 million in a settlement deal to **Jabil** after it decided not to renew their manufacturing service deal, according to a filing with the US Securities and Exchange Commission.

Emerald Technologies purchased an **Ersa** Versaflow 4/55 selective soldering machine for its Saline, MI, location.

Escatec purchased a **Delvotec** M17S automated wire bonder.

Europlacer signed a global partnership agreement with **Siemens** to integrate Valor Process Preparation software into its surface mount assembly platforms and products.

Fabrinet will produce **Aeva's** 4-D LiDAR chip module.

Foxconn is rapidly growing its electric vehicle business, one of the three industries where the ODM strives to position itself. The company also plans to use proceeds from the IPO of its Foxconn Industrial Internet subsidiary to fund 7.3 billion yuan ($4 billion) in smart manufacturing platforms, cloud computing services and 5G solutions.

Green Circuits purchased an **Anda Technologies** iCoat-5 JetSelect conformal coating machine.

Heraeus Printed Electronics and **SUSS MicroTec** signed an agreement to develop digital inkjet printing of metallic coatings for semiconductor manufacturing.

Incap Slovakia upgraded its second SMT production line with advanced machinery.

Intel has postponed plans to invest in Italy after a project to build an advanced packaging and chip assembly factory was never finalized.

Jabil and **OpenLight** announced a strategic partnership to streamline and facilitate a backend manufacturing system ecosystem for PICs.

Kaynes SemiCon is shelving its plans to set up a chip assembly unit in India's Telangana state and is instead moving it to Gujarat.

Kubler US named **PMR Representatives** sales representative in Southern California.

May & Scofield purchased a **Promation** Quick 9434 robotic soldering platform.

OSI Electronics opened a new manufacturing facility in Tecate, Mexico, to expand its capabilities in North America.

Padget Electronics, a subsidiary of **Dixon Technologies**, entered a contract with **Compal Smart Device India** to manufacture mobile phones.

Panasonic has begun an expansion project at its SMT machine factory in China's Suzhou Industrial Park.

Q Source was named distributor for **Gentex's** PureFlo air purifier.

Rocka Solutions will distribute **Static Control Solutions** products in the US.

Sacral Industries is opening a consumer electronics and home appliances assembly factory in Lagos, Nigeria.

Samsung West Africa has partnered with **New Home Distribution Africa** to assemble its electronics in Nigeria.

Silicon Forest Electronics purchased a **Hentec Industries/RPS Automation** Vector 600 selective soldering system.

Signal Hound is expanding its southwest Washington headquarters by 11,000 sq. ft.

StenTech completed a major technology update at its Photo Stencil Specialized Products division in Golden, CO.

TopLine has filed for a patent for solder columns for electronic components intended to operate in cryogenic environments.

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sales@XDry.com

PCDF


Rafael Padilla


David Spehar


David Warner


Russ Schwartz


Steve Medd


Leigh Eastwood

AT&S named **Rafael Padilla** senior manager, business development.

Incap appointed **David Spehar** to its management team.

PCB Technologies announced **David Warner** as account manager, East Coast.

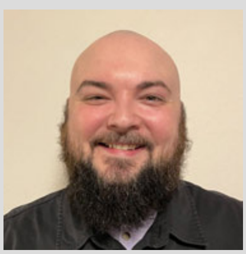
Uyemura promoted **Russ Schwartz** to project engineer and appointed **Steve Medd** support engineer.

Ventec appointed **Leigh Eastwood** technical sales engineer.

CA


Chris Matthews


Ian Linn


Nicholas Chase


Rahul Bilakanti


Ken Reilich


Heriberto Cuevas


Wayne Ellis


Emilio Ramirez


Leo Gibbs


Jason Appleton

AIM Solder named **Chris Matthews** business development manager.

ALL Circuits named **Stephane Klajzyngier** group strategy and development director.

BAE Systems named **Ian Linn** operations manager.

ECD hired **Nicholas Chase** as senior software engineer and **Rahul Bilakanti** as manufacturing engineer.

Intraratio named **Ken Reilich** senior vice president of worldwide sales and marketing.

Koh Young appointed **Heriberto Cuevas** sales team leader for its Mexico and South America operations.

Microboard named **Wayne Ellis** vice president of supply chain.

NEOTech promoted **Emilio Ramirez** to chief technology officer.

PDR Rework appointed **Leo Gibbs** commercial director.

STI Electronics appointed **Jason Appleton** master instructor.

Unigen named **John Burke** chief of manufacturing.

PCEA Training Announces June and September PCB Design Classes

PEACHTREE CITY, GA – PCEA Training is offering a pair of five-day training classes in June and September for printed circuit engineers, layout professionals, and other individuals currently serving in the design engineering industry or seeking to get into it. The classes include an optional certification exam recognized by the Printed Circuit Engineering Association (PCEA).

The dates of the classes:

- Class 1: June 14, 17, 21, 24, 28
- Class 2: September 16, 17, 18, 19, 20

These instructor-led classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

There are no prerequisite requirements to enroll. Upcoming classes will be held online. All courses are led by experienced instructors.

To apply, visit pceatraining.net/registration for the next available class or contact Mike Buetow at pceatraining@pcea.net for additional information.

Registration fees include the 400-page handbook, *Printed Circuit Engineering Professional,* authored by Michael Creeden, Stephen Chavez, Rick Hartley, Susy Webb and Gary Ferrari.

For information about the instructors of the course and authors of the course material, visit pceatraining.net/instructors-authors.

For information about the course overview, class format, and materials to prepare in advance for the class, visit pceatraining.net/course-overview.

Denver. Those interested in attending a meeting in the Denver area on May 13 should contact Mike Buetow (mike@pcea.net). The meeting will feature a talk on PCB design and time for networking.

New England. The chapter will have its kickoff meeting on May 2 on the campus of the University of Massachusetts-Lowell. Featured speakers are Gopu Achath of EMA Design Automation on supply chain-driven circuit design and Paul Yang of Jove PCB on embedded inductors. Contact Mike Buetow at mike@pcea.net for details.

Portland. The next chapter meeting is scheduled for April 18 at 12 pm. Contact Stephan Schmidt for details (stschmidt@outlook.com).

San Diego. The San Diego chapter will hold a pair of technical talks in conjunction with the Del Mar Electronics Show on Apr. 24. Stephen Chavez of Siemens will speak on designing complex PCBs and Tom Hausherr of PCB Libraries will talk on component library development and management. We will have several special giveaways as well, including two free licenses for PCB Libraries. For information, contact Luke Hausherr (luke.hausherr@freedomcad.com).

Silicon Valley. Our March meeting topic on Design Essentials to Maintain Signal Integrity was given by Amit Bahl and Atar Mittal of Sierra Circuits. Attendees were treated to a tour of Levi's Stadium, home of the San Francisco 49ers.

Some attendees and Sierra Circuits' staff at the site of the Silicon Valley chapter meeting in March.

europlacer HIGH MIX PRODUCTIVITY

Europlacer Adds Two New Machines to iineo Platform Range.

FOR MORE THAN 15 YEARS, the legendary Europlacer iineo pick & place machines have led the surface mount assembly industry in exceptional real-world functionality and unmatched flexibility. Now the company has announced the launch of two brand new pick & place machines that become part of its iineo platform line-up.

The new ii-N1 and ii-N2 machines build on the iineo-I and iineo-II, featuring single and twin tornado turret heads respectively – each of which can be specified with eight or twelve nozzles. The ii-N1 is pitched as best-in-class for prototyping; the ii-N2 as the ultimate in high-mix flexibility. Placement rates are 14,770 cph and 29,540 cph.

Nothing that made the iineo platform pre-eminent in its field has changed. For instance, the groundbreaking 264 x 8mm reel feeder capacity remains with space for up to 10 Jedec trays in the ii-N1. But enhancements to the flexible turret-head-based platform concept abound in both these new models.

Among the most significant is an intelligent conveyor system that eliminates mechanical board stops completely. Until now, this technology was exclusive to Europlacer's high-end atom range. Why is an intelligent conveyor important? The productivity benefits are extensive. When a board can be halted under software control with absolute precision at any position within the machine, the entire placement process can be optimized. In addition, Europlacer customers can automatically optimize the board stop position for maximum productivity. Both machines also feature motorized auto-width adjustment as standard

Looking ahead. Supporting the productivity drive is a re-engineered machine vision system featuring higher-resolution 'on-the-fly' cameras for turret components and optional fixed upward-looking cameras for large and QFP components. Looking to the future of device miniaturization, the turret cameras are designed to image components down to 03015m dimensions that are increasingly being deployed in high functional density designs for wearables. Yet these smart new cameras can still address devices up to 99mm x 99mm in size and 34mm in depth with pinpoint accuracy. For the twin-turret ii-N2 machine, only the camera on the first turret validates the PCB fiducials, which eliminates the need for the second turret to do so, thereby saving time and delivering further productivity improvement.

Another key feature appropriated from Europlacer's premium atom range is Auto Adaptive Sequencing (AAS). As well as defining placement priorities to set up a sequence that maximizes productivity, AAS intelligently accounts for component shapes and dimensions, nozzle profiles, PCB characteristics (including board warpage) and turret head trajectories to avoid collisions. Both new machines also deploy Europlacer's 3DPS technology that adjusts each placement nozzle's Z-axis travel in real-time to compensate for board warpage, removing the need for support tooling.

CFX naturally. As would be expected from Europlacer as a key contributor to the IPC's CFX standards, both the ii-N1 and ii-N2 are certified CFX 1.7 compatible. That facilitates easy connectivity between these new machines and all other CFX-compatible equipment in a production line.

The real benefits of integrated CFX functionality show through in enhanced factory-wide productivity thanks to optimized connections to equipment beyond the machines in the immediate assembly line. Both the ii-N1 and ii-N2 offer seamless connectivity to Europlacer's STORAGE 2000 tower and the Innovaxe automated reel storage system for optimized parts and feeder location.

In addition, both machines deploy Europlacer's latest RC5.17 operating software, which itself comprises a host of new features including the open-source Maria DB database system. Extending the operating software functionality are upgrades to Europlacer's ii-Tab mobile solution, which now allows reels to be booked and automatically assigned after picklist creation. With the Warehouse Management tool, the picklist can be sent directly to the storage tower or the mobile rack solution to enable automatic reel delivery.

Where to see these new machines. Europlacer revealed the single turret ii-N1 machine, paired with the new ii-P7 screen printer, at Productronica Shanghai last month. Visitors to the IPC APEX Expo in Anaheim from 09 to 11 April can see the ii-N2 machine on the Europlacer booth #1830.

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Not going to be at APEX? Contact us to arrange a remote demo of our ii-A1 directly from our US Center of Excellence in Phoenix, AZ.

Thailand Leading Way as Industry Alternative to China

TAIPEI – Taiwan's PCB industry continues to expand its factories in Thailand and Vietnam to strengthen the resilience of the global PCB supply chain, and representatives of the Taiwanese and Thai governments are actively negotiating for assistance to Taiwanese factories, says the Taiwan Printed Circuit Association.

According to a client survey conducted by Goldman Sachs Group in early 2024, 54% of respondents see geopolitics as the main risk to the current market and the global economy, while the threat of inflation has eased. In addition to cost-effectiveness and market operations, geopolitics has become an important consideration in international supply chain strategic planning. Against this backdrop, Southeast Asia has become a direct beneficiary of the global PCB and electronics supply chain.

In addition to the advantages of abundant labor and relatively low labor costs, the geopolitical risks in Southeast Asia are also limited. Amid the current international tensions, the region has become a popular choice for enterprises seeking an alternate production base, which is conducive to promoting the development of the local PCB industry. Among them, Thailand has a leading competitiveness in the region by virtue of its relatively mature PCB and downstream electronics industry. In 2023, Thailand's PCB local production output will account for about 3.8% of the world's total, and it is expected to grow to 4.7% in 2025 as the world's major PCB manufacturers continue to deploy locally.

Although the PCB supply chain in Southeast Asia is still in the early stages of development, and manufacturers still face many hidden costs, the implementation of the ASEAN Common Tariff Agreement will help improve the regional trade environment and make up for the supply chain shortcomings, TPCA said. It is expected that the initial challenges will be gradually overcome over time, resulting in improved overall cost-effectiveness, the trade group added.

Audio, Video, Disco

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	NOV.	DEC.[r]	JAN.[p]	YTD
Computers and electronics products	0.5	-0.4	0.3	0.4
Computers	4.9	-0.6	4.2	19.4
Storage devices	-2.4	-3.7	7.7	15.7
Other peripheral equipment	1.5	0.8	6.5	4.0
Nondefense communications equipment	0.2	-0.5	0.0	-2.8
Defense communications equipment	-2.4	-2.0	1.0	-4.1

A/V equipment	-0.6	-3.2	12.6	17.4
Components[1]	1.5	1.8	0.9	8.8
Nondefense search and navigation equipment	0.6	0.0	0.9	2.6
Defense search and navigation equipment	1.6	-1.5	0.9	5.9
Electromedical, measurement and control	-0.1	0.0	-1.5	1.4

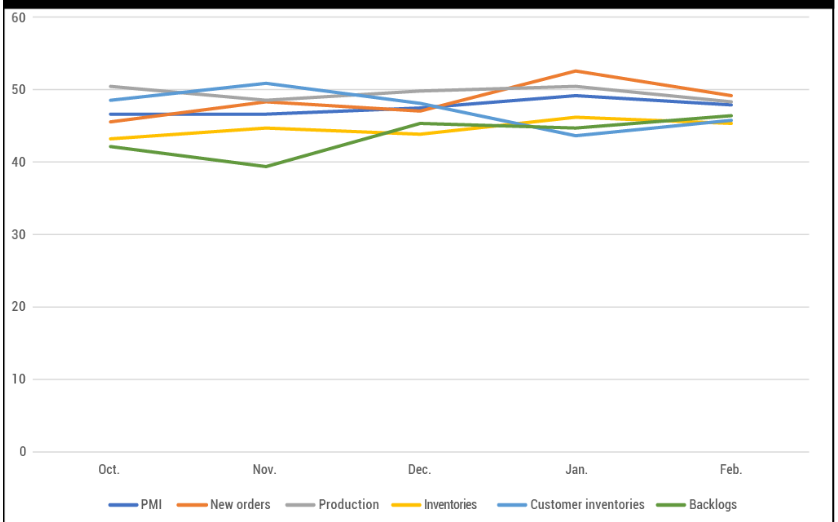
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Mar. 5, 2024

Key Components

	OCT.	NOV.	DEC.	JAN.	FEB.
EMS book-to-bill[1,3]	1.18	1.18	1.16	1.15	1.22
Semiconductors[2,3]	-0.7%	5.3%	11.6%	15.2%	TBA
PCB book-to-bill[1,3]	0.97	0.97	0.90	0.93	1.07
Component sales sentiment[4]	88.8%	82.8%	77.8%	98.0%	100.8%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA

US Manufacturing Indices



Source: Institute for Supply Management, Mar. 4, 2024

Hot Takes

Printed circuit board assembly production by EMS companies achieved record revenues of 57.3 billion euros in 2023, with EMS outsourcing representing 43% of the total available market of Europe's PCB assembly. (in4ma)

The US lacks the capacity – even with the 109 fabs planned to come into operation by 2026 – to see its **semiconductor industry** become a $1 trillion market by 2030. (SEMI)

Global PC shipments are predicted to reach 265.5 million units in 2024, up 2% from the prior year. (IDC)

Total **North American EMS shipments** in February rose 4.1% year-over-year and fell 0.8% sequentially. Bookings increased 26.4% year-over-year and increased 16.5% from January. (IPC)

The pace of **Bay Area tech layoffs** so far in 2024 remains below the cutbacks in the industry over the same time frame in 2023 – even as a widening number of technology companies continue to chop employees. (GovTech)

The value of **exports from Taiwan** grew 1.3% in February, year on year – weaker than the prior three months. (ING)

The global market for **AR/VR headsets** grew 130% year-over-year during the fourth quarter. (IDC)

The **Taiwanese PCB industry** is actively expanding its operations into ASEAN countries, such as Thailand and Vietnam, to enhance the resilience of the global PCB supply chain. (DigiTimes)

Global shipments for **gaming PCs** declined 13% year-over-year to 44 million units in 2023, yet gaming monitors bucked the trend, growing 20% as lower pricing helped drive volume. (IDC)

Global **semiconductor sales** totaled $47.6 billion in January, an increase of 15.2% compared to the January 2023 total of $41.3 billion. (SIA)

North American PCB shipments fell 11.6% in February versus a year ago but rose 7.1% sequentially. Bookings were up 25.6% and 47.5%, respectfully, compared to the previous year and month. (IPC)

Shipments of artificial intelligence PCs – personal computers with specific system-on-a-chip (SoC) capabilities designed to run generative AI tasks locally – will grow from nearly 50 million units in 2024 to more than 167 million in 2027. (IDC)

Semiconductor revenue growth of 12% is expected in 2024, followed by 21% growth in 2025. Moderated growth is anticipated in 2026 as the market enters a downcycle later that year. (Techcet)

India's technology sector is expected to grow 3.8% to $253.9 billion in 2024, compared with the previous fiscal year's 8.4% as clients hold back spending and delay decision-making. (National Association of Software and Service Companies)

Taiwan-based notebook ODMs, several of which experienced sequential shipment decreases in January, are expected to witness a pickup in March shipments. (DigiTimes)

The global **semiconductor materials market** is set to grow nearly 7% as conditions turn favorable in 2024. (Techcet)

Q4 foundry revenues rose 7.9% to $30.49 billion, primarily driven by **demand for smartphone components,** such as mid and low-end smartphone APs and peripheral PMICs. (TrendForce)

The Point of Pride

Returning to a focus on soft skills will help industry find responsible employees.

FOR WELL OVER a decade, the number one question, complaint and concern I hear from businesspersons, regardless of industry or company size is: "Where is industry – any and every industry – going to find all the people necessary to actually build stuff?" And yet despite this serious workforce void, businesses continue to plan on a combination of reshoring product from distant lands or growing organically – which requires expanding their workforce. But how can you expand your manufacturing when the most critical ingredient – employees – is nowhere to be found?

Academia, from the earliest contact in elementary school to high school and right through university, has become misaligned with the real-world skills and education needed for a balanced and thriving economy. Yes, society needs doctors, lawyers, engineers and other more academically focused professions, but society also needs people with the interest and skill to touch and build product. In addition, there are real skills, education and training that together enable a worker to operate the complex and simple machinery and processes that successfully produce a multitude of technologically advanced, viable and sought after products. Maybe it is time to recalibrate our focus to some of the traits and skills that lead to success regardless of profession but appear to be currently missing in the workforce.

The first is promoting, developing and rewarding something called *work ethic*. From elementary through graduate school, teachers should instill in students that while the grade is important, it's *how* you work toward getting a grade that is the arbiter of future success. Acknowledging the effort made even if by way of saying "well done" to someone who is giving a task everything they have, even when they fall short of an "A+." Being motivated promotes a strong work ethic. In my career, I have worked with many "C+" people who through hard work and dedication – work ethic – have outperformed their classroom "A+" peers. How? They simply worked harder, took the task at hand seriously, and continually strived to improve. I fear academia is often too quick to stress the grade when the more important life skill is developing and maintaining a strong work ethic.

Developing a strong work ethic, of course, requires another increasingly rare trait: *persistence*. Too often people when challenged will stop, retreat and move onto something different and easier rather than working diligently to find a way to "nail this!" Developing persistence requires a parent or teacher with much patience. Applying persistence when challenged contributes to building self-confidence as well as a strong work ethic.

Clear communication is another lost skill – despite all the advances in technology and social media developed expressly to improve communication. Being able to text is great, but in the workforce – and life – being able to verbally communicate, face to face, concisely and with mutual respect is critical. "Hey bro …" may be a fine way to open a conversation with good friends, but it is not an appropriate way to address a coworker or supervisor. Equally important are basic writing skills. Work often revolves around emails, which means creating concise, to-the-point emails that address a question, problem or thought that is being distributed or copied to a wide spectrum of people who may or may not be familiar with the topic. Clear, concise writing, along with articulate verbal skills, are critical for success in any work environment.

Getting along with different types of people – read: coworkers – who may have very different backgrounds, interests and opinions is equally critical. Respect for others and the ability to work with those whom you may not personally like – but professionally must work with – is necessary to thrive in life. Those who have not been taught how to interact with different or difficult people, including interacting professionally day in and day out, will most likely have difficulty in whatever they pursue. I have seen too many young people quit a job simply because they do not like a coworker.

Taking *personal pride* in what you do is one of the most important traits that too often is missing by people entering the workplace. Much like work ethic, it is caring that what you do is completed well, finished on time and delivered with no mistakes – the first time and every time. Pride makes people shine in comparison to those around them. Pride defines who you are, what you do, and most of all, what others think of you. Pride is also demonstrated by little things, such as showing up to work early and being the last to leave.

Which brings us to responsibility. When you combine a strong work ethic, persistence, the ability to communicate verbally and in writing, the flexibility to work with others no matter how diverse, and take pride in your work, the result is a responsible person. Every manufacturer I have ever known has "be a responsible person" at the top of their list of desired traits in employees. The sad reality is that when looking for employees, you can find people with intelligence and who have potential skill but show symptoms of lacking responsibility. Symptoms such as not showing up for work on time every day, bristling when being challenged or taught basic work tasks, copping an attitude with people they do not like, and not taking pride in the work they do is regrettably too much the norm.

Employers must stress to schools, academia and youth to recalibrate the lessons of essential personal and professional traits and skills in order to have a balanced and available workforce to meet tomorrow's challenges. The next generation needs to focus on developing a solid work ethic, persistence, interpersonal communication skills, and most of all, pride. For those who do so, abundant and lucrative career opportunities lie ahead – especially in manufacturing.

PETER BIGELOW is president of FTG Circuits Haverhill; (imipcb.com); pbigelow@imipcb.com. His column appears monthly. He is vice chair of the UHDI & Substrates: Design to Package Forum, to be held on June 5, 2024, in conjunction with PCB East in the Boston suburbs.

FOCUS ON BUSINESS

The 80/20 Rule

Don't be afraid to drop bad fit customers.

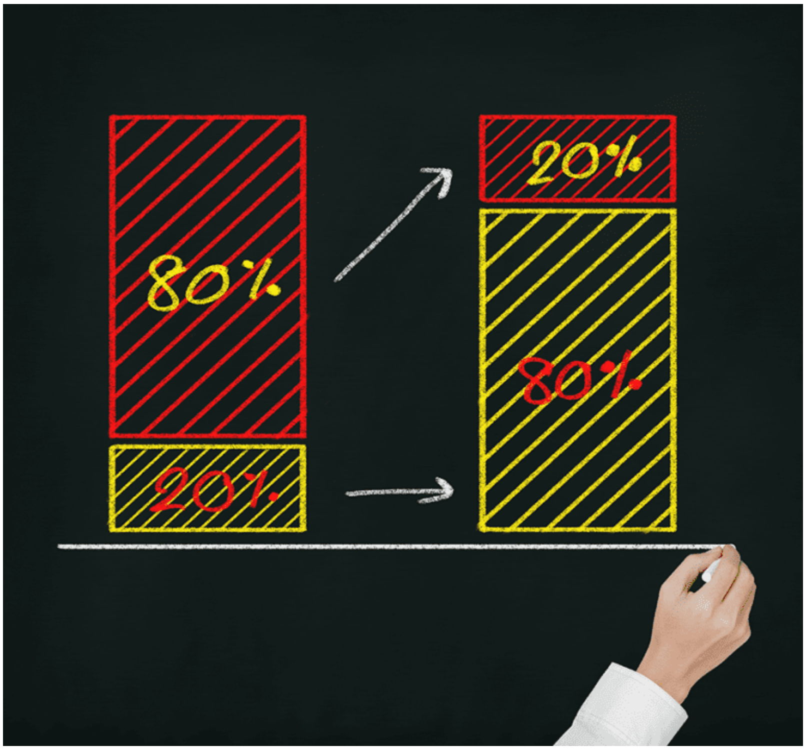
SINCE TAX SEASON is upon us, I recently had a chat with my CPA. She is co-owner of one of the largest accounting firms in my area and I've done business with her for over two decades, so we discuss business strategy in addition to going over the numbers. This year, she mentioned they were planning to rationalize their customer base, eliminating those who tended to provide incomplete records right before critical deadlines. She saw these clients as problematic to her business for two reasons: they overloaded resources and their behavior increased the probability her team would make a mistake.

There is a parallel in the electronics manufacturing services (EMS) industry. Ask any longtime industry CEO and they will say 80% of their issues come from 20% of their customer base. Why do EMS companies keep bad fit customers? There are a number of reasons:

- A long-term customer hasn't evolved as the EMS provider has grown and no one has analyzed the cost to continue to service it
- The project or division is part of a larger more attractive piece of business and taking the bad fit business is necessary to keep the good fit business
- Business is down and the EMS company doesn't want to lose any customers
- The company is expected to grow or outsource more attractive business if its initial needs are handled well, but that better business never gets awarded
- No one is analyzing whether accounts are a good or bad fit.

It isn't unusual for OEMs to outsource a basket of good fit and bad fit business so in cases where the problem project is part of a larger, more attractive project, it is better to keep the bad fit business. Similarly, there are situations where a smaller piece of business is the path to the larger piece of business.

My accountant's observations also apply in this situation, however. When an account is exceptionally problematic it consumes resources, leaving fewer for customers that are better fits. Potentially, this often-reactive resource drain may result in program teams disappointing a good account with far more growth potential. The odds of quality issues in a problematic customer are also higher, particularly if inability to forecast is forcing expedites that must be purchased through gray market sources. The cost to service problematic customers is also higher and often those costs are never captured.



How do you address this trend?

First, program managers should analyze accounts for fit with the business model at least annually. Accounts that seem to fall outside good fit business trends in terms of volumes, profitability and customer behavior should be more closely evaluated.

- What changes would make this account more attractive?
- Is there a potential for growth in value-add or growth in total business?
- Is there a way to coach the customer in better forecasting or planning practices?
- Would product lifecycle management (PLM) or design for excellence (DfX) recommendations help eliminate some of the issues?
- If the account is expected to grow over time, how long will it take?

In short, the analysis should evaluate the potential for the business relationship to improve and set action items and a target date for when those improvements would begin to happen. If no improvement is possible and losing the customer wouldn't put a larger account at risk, the next step would be determining how best to disengage.

This is an important decision. There are multiple options:

- Discuss the business fit issue with the customer and introduce them to a better fit EMS option
- Raise pricing until they leave

- Put the project at lower priority in the factory and let late deliveries incentivize them to leave
- Give them a deadline to leave.

Interestingly, the last three options are the most common ways EMS providers use to get rid of bad fit customers. The problem is that they damage your brand. Sourcing managers move among companies, and they have long memories, particularly if they felt that an EMS company treated them badly when disengaging. This is particularly true when a deadline to leave doesn't give them time to find a new source and create a transition plan. Some EMS providers even have a reputation for welcoming all types of business in market downturns and then triaging the bad fit accounts when the economy improves.

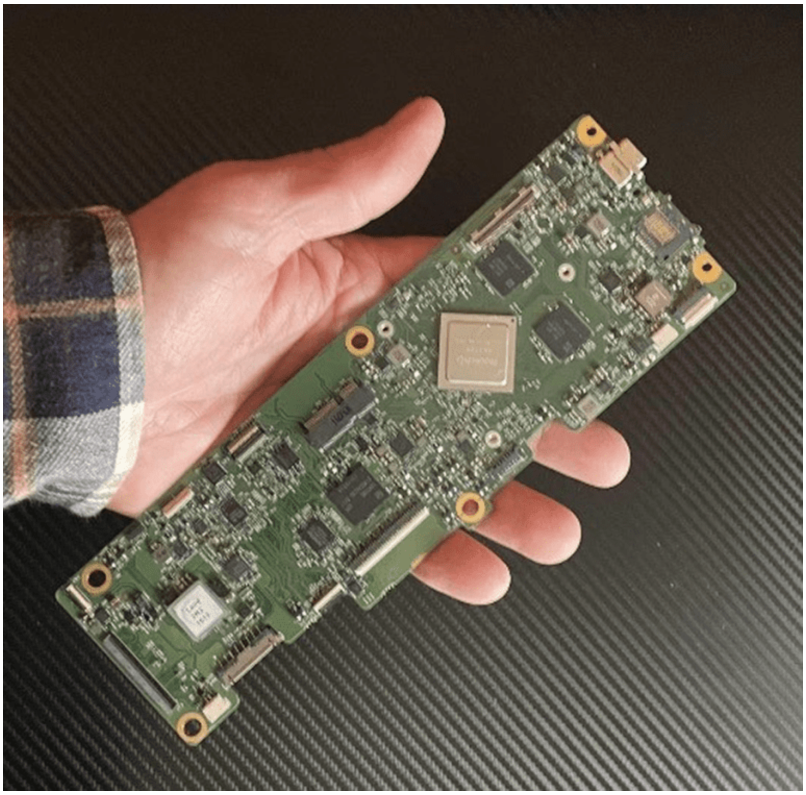
Bad fit accounts are a lose-lose situation: bad for both the EMS provider and customer. The best way to avoid them is to screen prospective customers against a definition of what a good fit account looks like, set clear expectations about the relationship during the sales and NPI processes, and work with the customer to correct problematic behavior when it first begins. If fit issues become unresolvable over time, try to initiate a disengagement process that works for the customer.

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services.* She can be reached at smucha@powell-muchaconsulting.com.

Designing for PCB Assembly

What's best for your design may not be what's best for assembly.

PRINTED CIRCUIT BOARD assemblies animate a collection of components designed to do something useful. Joining those components on a board that completes the connections with a circuit pattern is the best solution we have to create modern electronic devices. The performance and reliability of the device is largely determined by interconnections on the PCB assembly.



A six-layer board that uses the outer layers for routing as well as placement. (Image credit: Author)

The placement itself is a function of the signal connectivity on a local scale and voltage domains on a macro scale. More chips equal more voltage domains. Each IC requires dedicated support consisting of some or all of the following:

- Passive components that do the grunt work of supplying and filtering power
- External clocks for optimizing data flow

- Local power supplies
- Test points, connectors, etc.
- Wherever the I/O pins take you in terms of neighboring components.

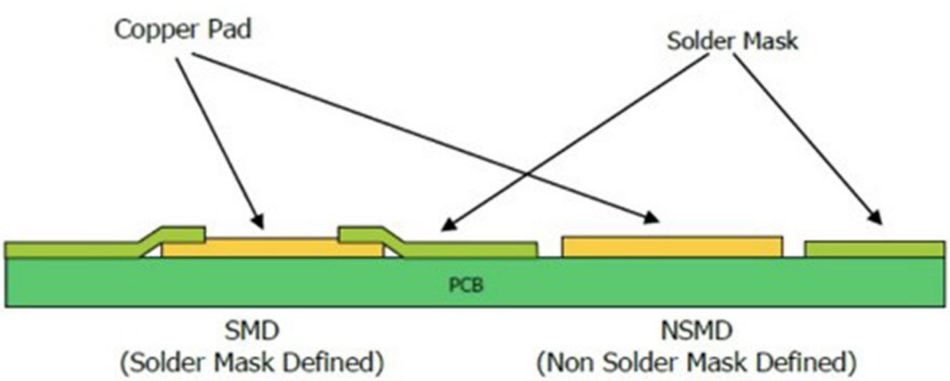
The component placement is prioritized roughly in that order with analog chains the first in line for placement consideration. Just as you did not (likely) get complete freedom of choice on the board outline or interface components, you add your personality to the mix. Seriously, doing board design rewires your brain to do board design!

BGA placement (your assembly line might not like this). Pins lucky enough to be on the outside row of a ball grid array (BGA) are special. The ball mapping session from the chip through the package to the board can be contentious. No team really wants the XO pin(s) on its doorstep. As designers, we're happy to see them on the outer edge so we know where to put the crystal. The best placement permits top-side fan-out of as many of those accessible pins as possible. We end up with an apron of little parts around the big part.

If you ask the assembler how to do the placement, there would be no parts anywhere near the BGA to permit a nozzle around it for rework. We want that crystal and those decoupling caps right next to the device. The assembly line managers don't want to have to desolder those parts to replace a chip.

That's not the only contradiction. It would be nice if all the polarized components were oriented the same way. In fact, all the components of a type should be mounted in the same rotation. Use one side of the board. Spread everything out. Use three tooling holes. No routing under the fiducials, etc. The manufacturing engineer wants to see the same opportunity for acceptable solder joints all across the board. Access for rework is second on their mind.

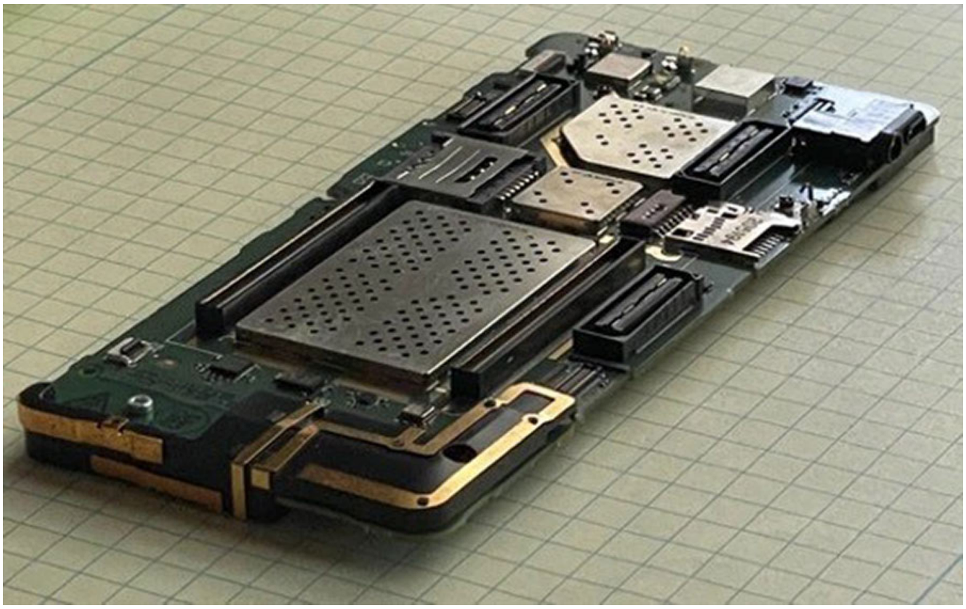
Optimum for assembly is thermal spokes that make up less than half of the perimeter of the pad. Of course, you would expand the solder mask to appease the component vendors. The SI/PI crowd needs that maximum copper pour to feel good about their simulations. Lots of copper looks better to me on those thermal plots too. The customer deserves the best we can build for them even if that means a tighter assembly process window.



The mask over the pad (SMD) is noted as having a stress point where the mask starts which could lead to the propagation of cracks across the solder joint. (Image credit: EE Stack Exchange)

The customer's requirements are first priority. With all these conflicting interests, we have to pick a winner and the winner is almost always the customer. The manufacturing engineer has to find the right solder paste granularity to go with the right stencil thickness and openings to dial in that board. The key process control from there is the preheat-reflow thermal profile as the oven gradually ramps up the temperature and then completes the soldering. The process has been shown to work better with proper thermal chokes around the pads.

What's best for the process isn't always best overall. What good is 100% yields in assembly when the product can't withstand the rigors on the job? Sometimes, we have to challenge them to compete on the leading edge. It comes down to a balancing act where everyone involved is a little nervous but not in a panic. Just be pragmatic and share the risk when one group wants something the other group cannot provide.



It's much more efficient to build it right than to rework it into submission. (Image credit: Author)

What could possibly go wrong? A gallery of solder defects also stems from missteps in the layout. For instance, a tall component could create a shadow where a nearby component would not reach reflow temperature for long enough. The edge warms up faster and ultimately hotter than in-board areas. An edge mounted part could see one pin in the hot zone. The difference could be enough to pull a ceramic cap apart. Same deal with a wirewound resistor.

This is not a theory. It was good enough (bad enough?) of a defect to make it onto the control chart where the assembly people were tracking yields. We wanted the blocking cap near the edge where it could do its thing. Well, we moved it inboard on the next revision. The point here is to take your learnings from the project filtered through all your other project learnings and give them something fit for production.

Other things that might show up on the solder defect control chart:

- **Solder balls.** This is an indication of too much solder and possibly excessive reflow temperature.
- **Solder bridges.** Happens on through-hole components when positioned along the axis of travel in the wave

or drag solder machine. Fine-pitch components are more prone to this when the solder dam is less than 100μm wide or gang relieved. Root cause once again could be too much solder.

- **Insufficient solder.** Symptom of hole-size/pin-size mismatch for through-hole components and improper stencil thickness or aperture size for SMD parts.
- **Measles.** This is local delamination. The usual suspect is the outgassing of steam. Boards are often baked to dry them prior to assembly to mitigate this defect.
- **Cold solder, pillow on head, disturbed solder, etc.** These reflow issues tend to be process related but could be caused by tall components next to small ones.

There are enough unmentioned solder defects to fill a workmanship manual. Your job, should you choose to accept it, is to intercept every one of them with a solid PCB as a foundation. Support it with good drawings and other documentation to bolster the reliability of the product.

A note about assembly drawings is to make them about what is rather than how-to. Don't get the assembly drawing entangled in the process. I got that kind of request when we had an in-house assembly group. Describing how to assemble is a whole different document. At most, you would perhaps specify SAC 305 solder or equivalent for typical boards. Even then, how do you inspect the board and decide it was put together with a specific solder? I don't like having to rely on a Certificate of Conformance with each shipment.

The more you can learn about your assembly process, the better your boards will become. It's a place where machines are taking over more and more as the precision required increases with the density of the boards. I look at those machines as a place where product flows in one direction and revenue flows in the other – back toward you. Let those machines be all they can be.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

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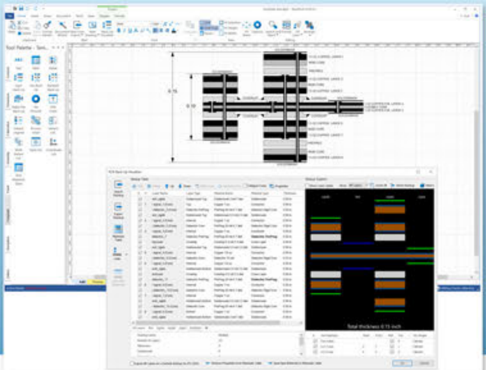

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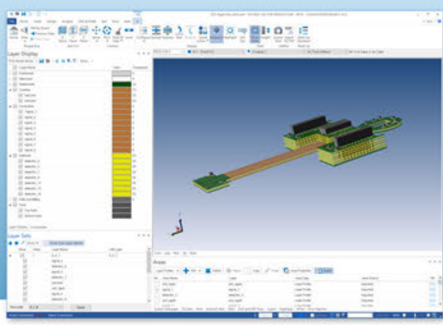
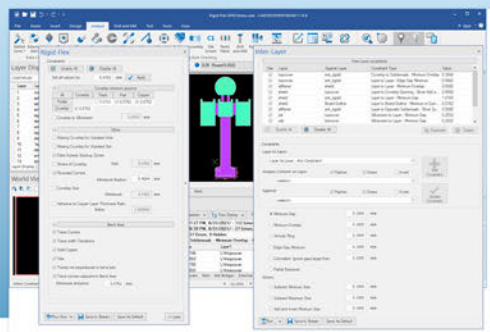


A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



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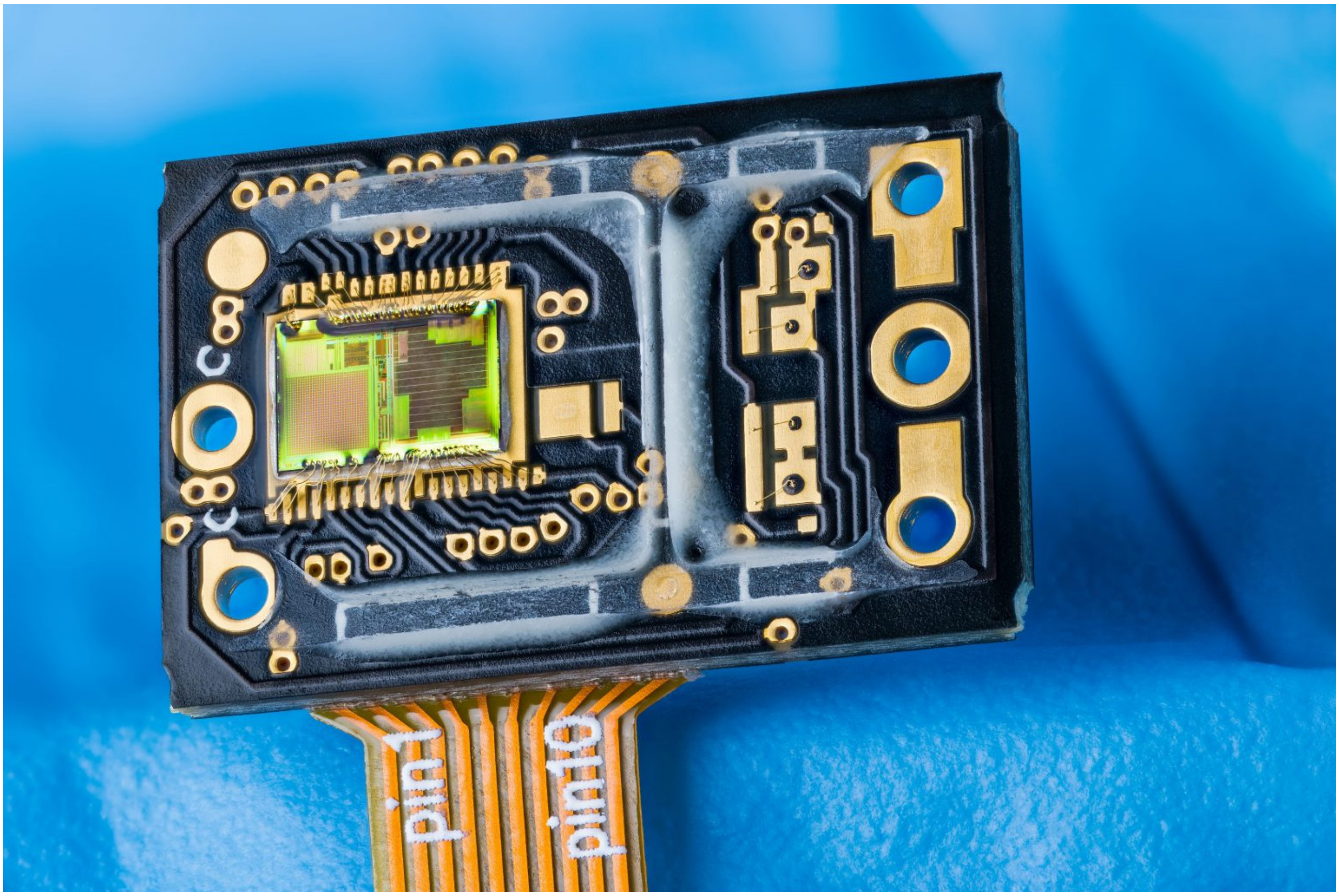
DESIGN **BEST PRACTICES**

A Journey in Rigid-Flex Design

Overcoming the challenges of rigid-flex designs can be incredibly rewarding.

AS TECHNOLOGY CONTINUES to advance, the demand for smaller, lighter and more efficient electronic devices is ever increasing. This demand has led to the emergence of rigid-flex PCBs, a revolutionary technology that combines the benefits of rigid and flexible circuits into a single solution.

As a principal PCB designer with several decades of experience in designing a wide spectrum of PCB technologies, I've had the privilege of delving deep into the world of rigid-flex PCB design. This month I'll share insights and experiences from my journey within this fascinating technology.



Once primarily seen in computers, rigid-flex is now found in every end-product, like this optoelectronic sensor board.

As I have progressed in my evolution as a PCB designer, more specifically with regards to rigid-flex PCB design, this technology has always presented a unique set of challenges and opportunities compared to traditional rigid PCBs or flexible PCBs. One of the significant advantages of rigid-flex technology is its ability to reduce space and weight in electronic devices while improving reliability and durability. Achieving these benefits, however, requires a thorough understanding of rigid and flexible circuit design principles, as well as the nuances of integrating them seamlessly.

In my early years at my first attempt with a rigid-flex PCB design, the thought alone intimidated me. Back then, rigid-flex PCB was kind of like a mystical type thing that was not widely understood. Even with several years of rigid PCB designs under my belt, I hesitated due to lack of knowledge in this realm but knew enough to get the fabricator involved at the earliest stages of design. Finding educational content on rigid-flex PCB design back then was not so easy. Not like it is today! Plus, EDA tools have come a long way and today have far superior capabilities and functionalities to address all the required details and constraints that make up a rigid-flex PCB design.

Here are some aspects to keep in mind.

Ensure mechanical reliability. Aside from collaborating with the PCB fabricator from the beginning of the project, one of the key considerations in rigid-flex PCB design is ensuring proper mechanical reliability. Unlike rigid boards, flexible circuits are susceptible to bending and twisting, which can lead to mechanical stress and fatigue over time. As a result, careful attention must be paid to factors such as material selection, bend radius and reinforcement techniques to ensure the reliability and longevity of the final product.

Manage signal integrity. Another challenge I have experienced in rigid-flex PCB design is managing signal integrity and impedance control. The flexible portions of the board introduce additional impedance variations and signal losses compared to rigid sections, which can affect the performance of high-speed and high-frequency circuits. To address this, designers must carefully analyze signal paths, use appropriate routing techniques and employ impedance matching strategies to maintain signal integrity across the entire board.

Design for manufacturability. In addition to mechanical and electrical considerations, rigid-flex PCB design also requires careful attention to manufacturability and assembly. Design for manufacturability is key. The unique construction of rigid-flex boards introduces complexities in terms of fabrication and assembly processes, which can impact yield, cost and time-to-market. Working closely with manufacturers and assemblers is essential to ensure that the design meets all requirements, performs as intended and can be efficiently produced and assembled with the highest yield and at the lowest cost.

Despite the challenges, working on rigid-flex PCB designs can be incredibly rewarding. The ability to create compact, lightweight, and highly reliable electronic products opens a world of possibilities for innovation and advancement. Whether it's designing wearable devices, medical implants or aerospace systems, rigid-flex technology offers unparalleled flexibility and versatility for a wide range of applications.

Over the years, I've had the privilege of working on numerous rigid-flex PCB projects, each presenting its own set of unique challenges and opportunities. From designing intricate multilayer circuits to optimizing layouts for maximum reliability and performance, every project has been a learning experience that has helped me grow and evolve as a designer.

Rigid-flex PCB design represents the future of electronics engineering, offering a compelling combination of performance, reliability and flexibility. Today, as a printed circuit engineer, I feel fortunate to be part of this exciting journey, pushing the boundaries of what's possible and helping to shape the future of technology. With continued innovation and collaboration, the potential of rigid-flex technology is limitless, and I look forward to seeing where it takes us next.

Ed: This column originally appeared in Siemens' Electronic Systems Design blog.

STEPHEN CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience and integrating the design-to-source Intelligence insights from Supplyframe into design for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com. He will speak at PCB East in the Boston suburbs in June.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How Do We Power 5G Networks?

5G has great potential, but brings power challenges at the infrastructure and board levels.

5G NETWORK CAPACITY is predicted to increase as much as 1000-fold by 2030. That's a stunning increase that can be attributed to effects such as our digital lifestyles and digital business transformation. Clearly, our dependence on online services that are available anytime, anywhere and at full speed shows no sign of abating. The effect on global energy demand could be even more stunning. The information & communications technology (ICT) industry currently consumes about 4% of the world's electricity, and this could increase to an amazing 20% with the growth of 5G networks. In absolute terms, that's equivalent to 150 quadrillion BTU per year.

Of course, 5G is huge, in scope as well as deployment. It covers low frequency bands, up to about 1GHz, although the main benefits of 5G are its ability to carry richer services that by their nature require faster data rates. These will push the limits of Frequency Range 1 (FR1) as defined by 5G standards, up to 6GHz in the FR1 range, and even higher in FR2 that extends into the millimeter-wave bands at 60-70GHz and even beyond. While services in the FR1 bands can support data rates of about 1-2Gbit/s, the higher bands are needed to support multi-gigabit data rates and latency of less than a few milliseconds.

At the highest frequencies, however, signaling range is considerably reduced. Each cell can only cover a small area. Weather conditions and other atmospheric effects can also affect range and the performance of the air interface. Many cells are needed to extend coverage, which will tend to restrict the fastest, most intuitive and high-value services to metropolitan areas. So, although we can expect to download at speeds of 10Gbit/s and faster – enough to allow downloading a complete high-definition movie in a few seconds – network deployment costs are high and extending coverage to reach rural areas is challenging.

There is great potential for delivering 5G services through satellites in low-earth orbits (LEO). After Starlink and similar satellite delivery platforms for Internet services have already shown the way, direct satellite delivery of 5G services is a logical step. Because access to space is now more affordable than ever, it is not difficult to foresee service providers extending their infrastructures into the sky as 5G continues to develop toward reaching its full potential.

Companies are already looking at the prospects for delivering services to connected vehicles, such as streaming entertainments, location-based services and telematics, as well as autonomous driving. Satellites could also hold the key to bringing 5G to rural and remote areas. 5G handsets with satellite transceivers are on the market now. It's fascinating to contemplate the opportunities for satellite-based 5G to cover inevitable shortcomings in ground-based delivery.

Ground-based infrastructure will be needed for the fastest 5G services, considering the natural physical limitations on range at high frequencies. Many small cells are needed, in conjunction with larger base stations. While the efficiency of 5G systems is unquestionably greater than earlier networks, our insatiable demand for richer services, instant responses and easy access for a growing number of subscribers is continuing to drive up demands for energy and power. 5G infrastructure is reckoned to need as much as four or five times as much power as 4G. Here's another startling statistic; a 5G base station is reckoned to consume more power than 70 households. Although we are more energy conscious than ever, engineering new ways to use this precious commodity more carefully, we are also using more than ever as our nature drives us to experience more richly and intensely accomplish more tasks in less time.

While there are obvious difficulties associated with generating the power to run 5G infrastructures in an environmentally acceptable way, managing power at the board level also brings many challenges. In particular, thermal management begins to demand careful attention at higher operating frequencies. This is calling for innovative design and new technologies throughout the hardware, all the way to the PCBs at the heart of each system. Ventec and other material suppliers are working hard in this area to create substrate materials that blend properties such as minimal signal-strength losses with high thermal conductivity. New ceramic-filled hydrocarbon materials are emerging that combine extremely low losses with about six times the thermal conductivity of ordinary FR-4 materials.

Performance improvements made possible by forthcoming advanced substrate materials show how our industry is once again surpassing perceived barriers through a dual strategy of reducing the magnitude of the challenge while at the same increasing our ability to combat its effects. In this case, low-loss materials are reducing the thermal demands on the substrate, while their increased thermal conductivity promotes extraction of the heat present to preserve the electronics at the heart of the system. We can hope to avoid the prospect of expensive and even more power-hungry active cooling systems for 5G base station electronics and – even less acceptable – more bulky and power-hungry 5G handsets and edge computing systems.

ALUN MORGAN is technology ambassador at Ventec International Group (ventec-group.com); alun.morgan@ventec-europe.com. Learn more about thermal management of hybrid PCBs in this special PCEA webinar presented by Ventec and available on the PCEA YouTube channel (youtube.com/@pcea-official).

Tear Resistance in Flexible Circuits

Proper design and handling can minimize the risk of rips.

I HAVE A potential new application for a flexible circuit for use in an inspection device. The flexible circuit will see some light pulling and tugging forces when extracted. Should I be concerned the circuit may be prone to tearing? If so, are there different materials that can be used that will not tear?

The short answer is yes; flex circuits can tear if not properly designed or handled. You did not mention the number of layers or the thickness, so I will assume that your application is only one or two layers and is on the thin side. As the layer count goes up, so does the thickness, and therefore the strength and tear resistance. Once a flex is four-plus layers with standard thickness materials, it should be very durable, and tearing should not be a concern if the extraction does not generate extreme shearing forces.

Virtually all flex circuits use polyimide film as the primary insulator. Polyimide film has lots of great electrical and mechanical qualities, but tear resistance is not one of them. In static applications there is seldom an issue, but if there are multiple flexing cycles during service, preemptive steps mut be taken in the design to guard against tears. The key is ensuring that a tear does not start, because once it does, it tends to propagate.

How do you accomplish this?

- Inside corners on the circuit outline are the most common areas for a tear to start. Inside corners should *always* be radiused, period. The larger the radius, the better! If a large radius is not possible, look at adding a laminated patch of flexible tear-resistant material that will cover the sharp radius. This patch is applied before the parts are punched out of the panel, so the patch would follow the exact contour of the circuit edge and would then extend inward ~0.125″ or more. Some examples of flexible, tear-resistant materials are PTFE or similar film that stretch rather than tear. Tyvek (the stuff they use to make full body biohazard suits) is also a good choice because it is inexpensive, flexible and virtually impossible to tear. The downside is it must be applied after any SMT operations; I don't believe it would hold up in a reflow oven.

  FYI, etched copper "tear stops" are *not* an effective way to keep a tear from propagating unless the copper is *really* thick (2oz+). Since most flex circuits are made with 1oz copper or less, a tear in the polyimide will run through the copper "tear stop" as if it weren't even there **(Figure 1)**.

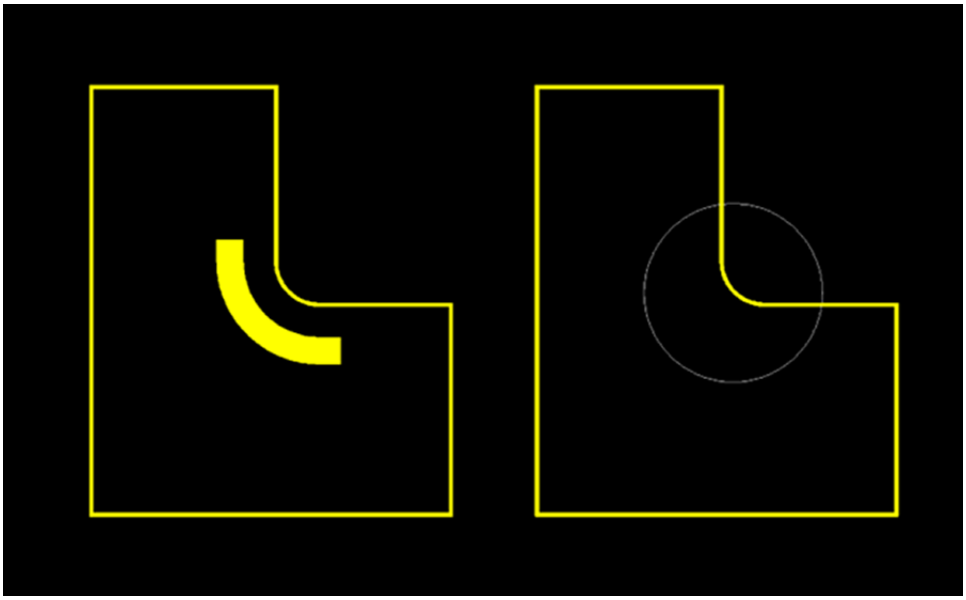


Figure 1. Copper “tear stops” (left pic) provide very little tear protection. The picture on the right shows a tear resistance material (such as PTFE film) laminated to an area that could be prone to tearing.

- Slits that go into the flex to separate different flex legs require a relief hole at the end of the slit. A slit is, after all, a partial tear. The relief hole at the end of the slit should be as large as possible (within reason). If flexibility beyond the end of the slit is not required, try laminate stiffeners to get the slit from propagating further into the circuit that you intended.
- Sharp edges along a stiffener can be an issue if there will be shearing forces in the application. This is typically an issue only in instances of one or two layers of flex. The standard “fix” is to apply a bead of semirigid epoxy along the stiffener edge. This is effective only if the stiffener is thick enough (over ~0.020″) for the applied bead to have a roughly triangular cross-section. If the stiffener is very thin, the cross-sectional shape will be more like a half-moon and will have limited effectiveness.
- Ensure the flex supplier uses a final punching tool that will leave a smooth profile without any nicks or cuts that could start to run through the rest of the circuit.
- Ensure operators use caution when installing the circuits so that they do not cause damage to the circuit profile.
- When the circuit is installed, it should be relaxed and not under any tension that could cause a tear to start and propagate.
- Using thicker layers of polyimide for the base laminate and outer cover material can make the circuit more robust, but the downside is that the circuit will be stiffer due to the added thickness, which may or may not be acceptable in the application.

I always recommend to contact the flex circuit supplier if the application has any special features that could cause undue stress on the circuit materials. Examples of this are a sharp twist in the flex when installed, odd profiles like serpentine patterns, or as in the application described at the start of this column, the need to pull on the flex to uninstall. Every application is unique and flex suppliers have probably seen it before and can steer you in the right direction.

MARK FINSTAD is director of engineering at Flexible Circuit Technologies (flexiblecircuit.com); mark.finstad@flexiblecircuit.com. He and co-"Flexpert" **NICK KOOP** (nick.koop@ttmtech.com) welcome your suggestions. They will speak at PCB West at the Santa Clara Convention Center in October.

RECOGNITION

CIRCUITS ASSEMBLY Announces 2024 NPI Award Winners

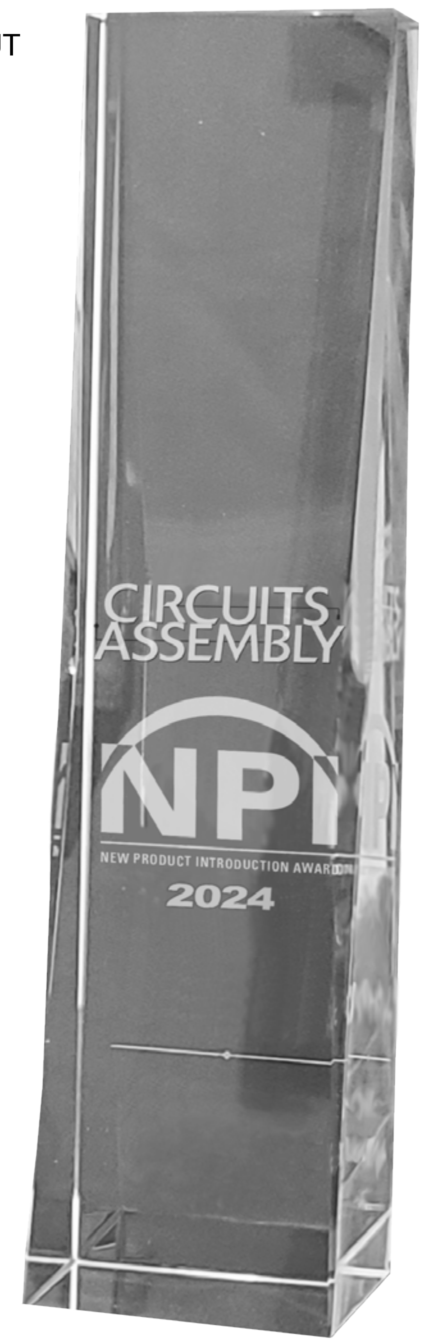
PEACHTREE CITY, GA – CIRCUITS ASSEMBLY in March announced the 2024 New Product Introduction Award winners for electronics assembly equipment, materials and software.

The 17th annual NPI Awards recognized leading new products during the past 12 months. An independent panel of practicing industry engineers selected the recipients.

The winners are:

Anda Technologies Automation Tools – ADA Series Smart Manufacturing Platform
Kyzen Cleaning Materials – AQUANOX A4618 KYZDS
Henkel Coatings/Encapsulants – Loctite Stycast CC 8555
Hanwha Techwin Automation Americas Component Placement – XM520 High-Speed Dual Lane Chip Mounter
Juki Automation Systems/Essegi Automation Component Storage – ISM 3600 FA, FAMR System
PVA Dispensing Equipment – Direct Series with new PathMaster X Programming Software
Tagarno First Article Inspection – Tagarno 4K Microscope
Indium Flux – Indium8.9FRV
ViTrox Process Control Tools – V9i XL ARV
ASYS Group Screen and Stencil Printing – SERIO 6000 with "Sphere" Intelligent Print Head
StenTech Screen/Stencil Printing Peripherals/Consumables – BluPrint CVD Surface Treatment

Cetec ERP & CalcuQuote Software – Management – Supply Chain Connected ERP
Vayo Software – Process Control – Vayo-Stencil Designer
Arch Software – Production – ArchFX GLO
Weller Tools Soldering – Hand Tools – Zero Smog Shield Pro
BTU International Soldering – Reaow – Aurora
Kurtz Ersa Soldering – Selective – VERSAFLOW ONE X-Series
ITW EAE Soldering – Wave – Deep Wave Option
AIM Solder Solder – Materials – NC259FPA
ViTrox Test and Inspection – AOI – V510i 3D AOI
Brooks Automation Test and Inspection – Functional Test – PreciseFlex 3400 Cobot
ViTrox Test and Inspection – AXI –V810i Advanced X-Ray Inspection (AXI) System – Series 3 Dual-Lane
Pemtron Test and Inspection – SPI – D-2
Henkel Thermal Interface Materials – Berquist Hi Flow THF 5000UT



"The judges this year noted the current trend for speed without losing accuracy," said Mike Buetow, president of the Printed Circuit Engineering Association. "But they also pointed out the interoperability requirements of systems and software, and stressed the importance of full functionality regardless of the logo."

For more information on the CIRCUITS ASSEMBLY NPI Awards, click here.

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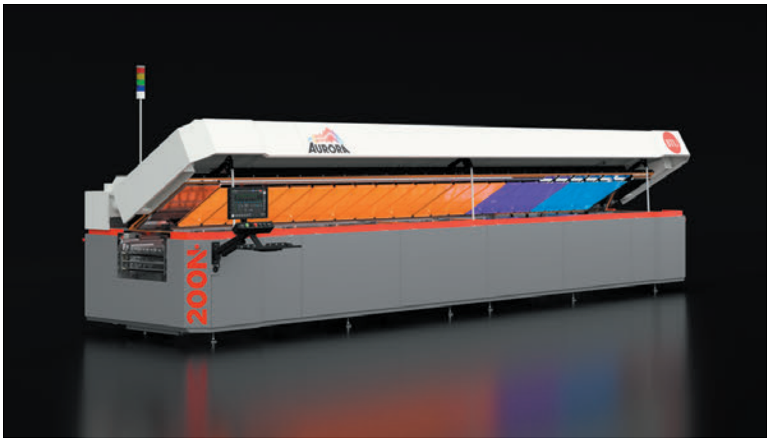

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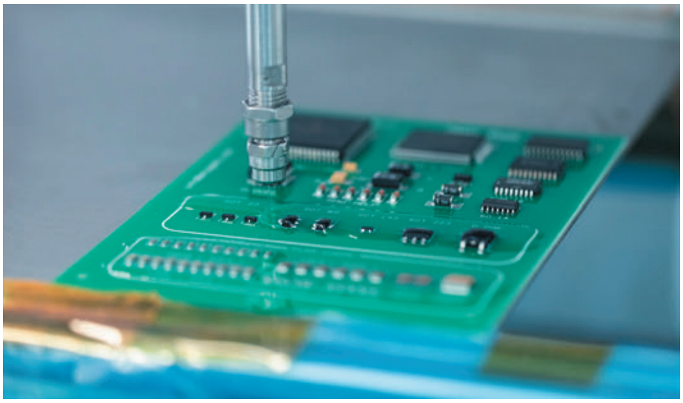

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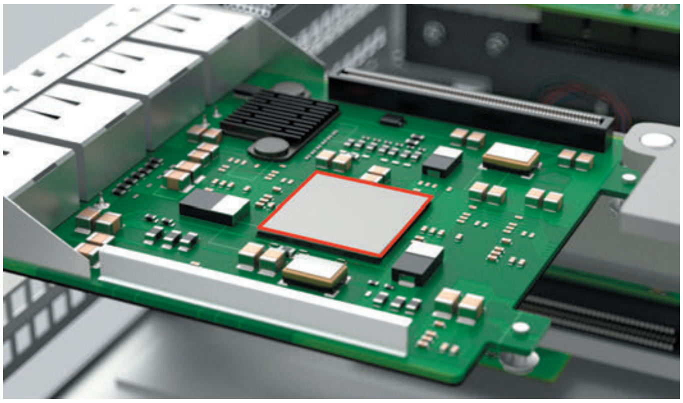

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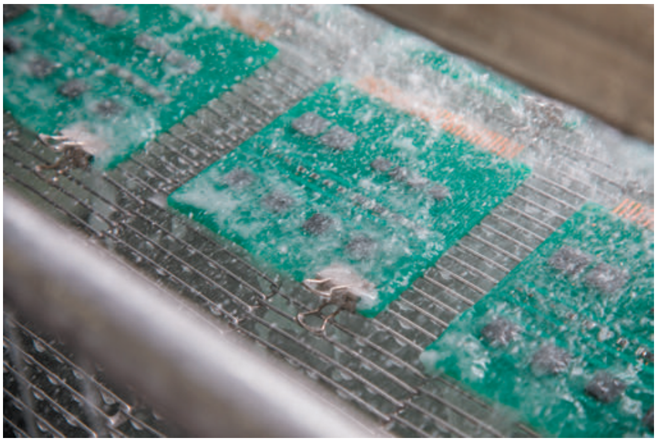

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V510i 3D AOI

TEST & INSPECTION – AXI

V810i Advanced X-Ray Inspection (AXI) System – Series 3 Dual-Lane

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THERMAL MANAGEMENT

Thermal Vias are Ineffective. Here's Why.

Adding thermal vias can take up valuable board space with little benefit.

by DOUGLAS G. BROOKS, PH.D. and DR. JOHANNES ADAM

We have developed several articles and publications in the past questioning the value of thermal vias.[1] Here is our definitive conclusion, and why.

Thermal vias are non-current-carrying vias between two layers provided for the purpose of permitting heat to conduct from one layer in a PCB to another. The idea is to lower the temperature of the heated surface compared to another, lower temperature surface. In a typical application, the heated surface might be a pad underneath a heated component. The opposite surface might be another pad or plane further down in the PCB structure. Someone untrained in heat transfer might suggest using thermal vias without an opposite copper surface, but we will show that such an approach is totally ineffective.

Simulation Model

We used the simulation tool TRM[2] to simulate several different combinations of thermal vias and configurations. The simulations consisted of:

1. A printed circuit board 150 x 150mm square by 2.4mm thick (not counting two 33µm top and bottom layers for creating pads and planes).
2. A copper pad 25 x 25mm square on the top layer heated with a continuous 2W of power.
3. Either a 90 x 90mm square plane, a 25 x 25mm square pad, or nothing on the bottom layer.
4. Several combinations of thermal vias, to be described below.
5. Lab conditions in still air, 20°C.

Our three standard configurations consisted of bare thermal vias with no terminations on their opposite end, or vias terminated on either a 25 x 25mm square pad or a 90 x 90mm square plane on the opposite side of the board. The standard via used had a conducting cross-sectional area of 0.16 mm^2. That is approximately equivalent to a 25-mil diameter, 4-mil plated via. We used either no vias, or 6, 12, or 18 vias placed on the pad in no particular pattern.

Model Extensions

Before we discuss the results in detail, we added a couple more twists to the analysis. Almost any article on thermal vias concludes that you need a *lot* of vias. Individual vias contribute very little by themselves. Our data show the same. So we also tested a model with an *infinite* number of vias to determine the absolute limit. We simulated that with a solid core of copper, 25 x 25mm square, extending from the top pad to the bottom layer or plane. That is not actually equivalent to an *infinite* number of vias, but on a simple equivalent cross-sectional area basis it is equivalent to just under 4,000 thermal vias.[3] We also simulated 96 and 1,164 thermal vias in a similar manner – by using six copper columns sized such that their collective cross-sectional areas were the equivalent of that many vias.

These last simulations are admittedly not perfect. The physical arrangement of the vias around the board affects the results. Nevertheless, we believe it is an acceptable way to approximate an otherwise impractical simulation. The results do not suggest that these approximations are unreasonable.

What Does *Effective* Mean?

Another question to be considered is, what does it mean that a thermal via is more or less "effective?" One interpretation is that, as additional thermal vias are added, the temperature drop across the thermal vias lessens, meaning more heat is conducted away from the heated surface. We think this misses the point. The fundamental problem is that the heated pad is too hot (relative to the surrounding environment, or ambient). We judge the effectiveness of thermal vias by the reduction of the absolute temperature on the pad, relative to the surrounding environment (or ambient temperature).

But even that poses a problem. As we have emphasized as often as possible, temperature is a "point" concept. That is, the temperature varies from point-to-point on a pad or along a trace because all the factors that impact temperature are also point concepts.[4] **Figure 1** is a thermal image of the top layer of our simulation of 18 vias connected to a plane. **Figure 2** is an enlarged portion of the heated pad itself (with a tighter thermal scale). What is the appropriate temperature reading? If we look at the top of one of the thermal vias it is 50.32°C. A via nearby has a temperature of 46.99°C. At the approximate center of the pad the temperature is 50.57°C. Just a few mm away the temperature is 48.91°C. We believe the appropriate temperature is the maximum temperature of the pad and that is what we report in **Table 1**.

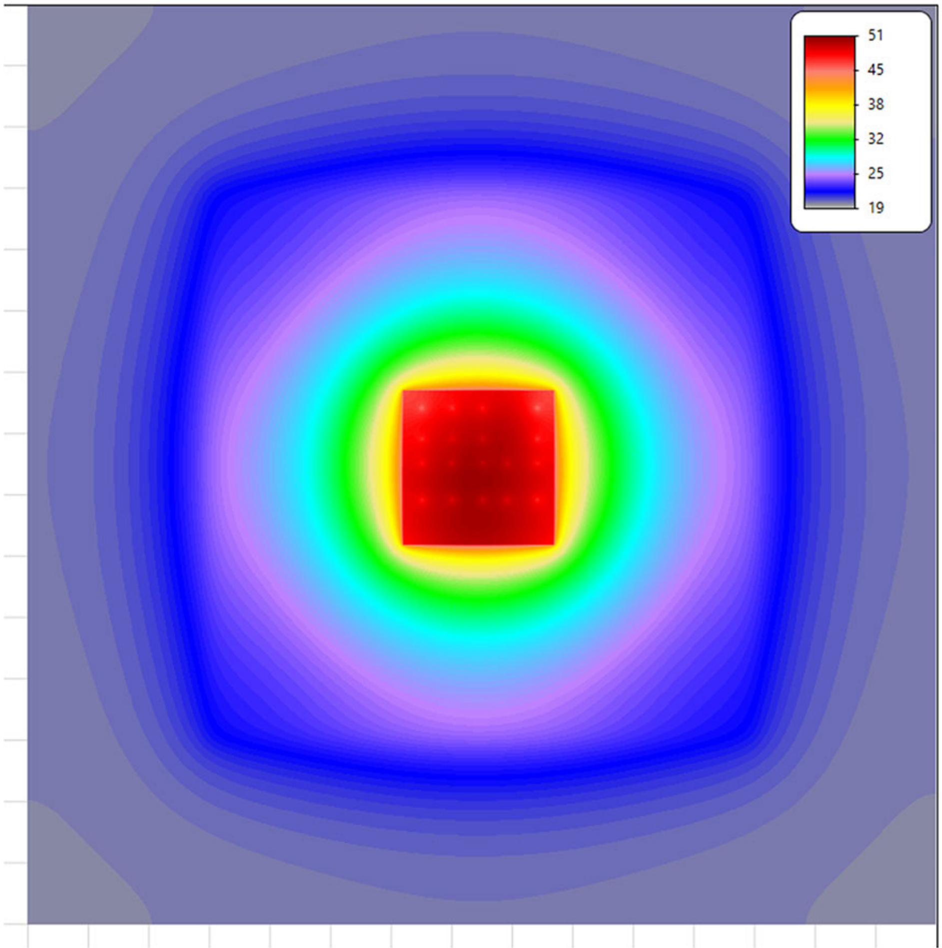


Figure 1. Thermal image of top layer of 18 vias connected to a bottom plane.

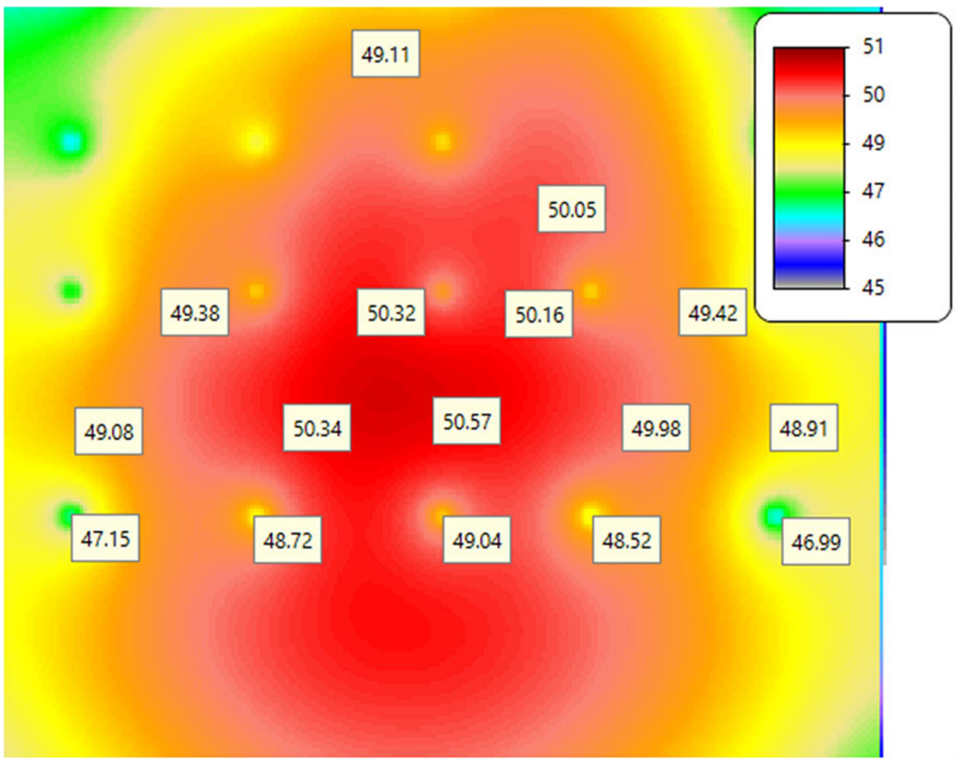


Figure 2. An enlarged image of the pad in Figure 1. (Note that the thermal scale is different.)

Table 1. Temperature of Surface of Pad, Via or Plane

Config.	Temp. (°C)	Number of Vias						
		None	6	12	18	96	1164	Inf.
No Pad	Top	83.1	83.2	83.2	83.3	83.3		
	Bottom Dielectric	79.2	79.4	80.1	78	79.9		
	Bottom Via		81.9	82.8	82.1	81.9		
Pad	Top	80.4	79.3	78.6	78.3	78.2	74.1	70.8
	Bottom Dielectric	73.2	74.6	75.4	75.2	75.7	74.1	70.8
	Bottom Via		75.7	75.2	76.1	76.6		
Plane	Top	54.6	52.6	51.3	50.5	50.7	47.8	41
	Bottom Dielectric	45.8	47.1	47.1	47.2	47.9	47.8	41
	Bottom Via		48.3	48.3	48.2	48.9		

Simulation Results

Now, with that background, we can look at the results (all temperatures are in degrees C). The raw data are tabulated in Table 1 and graphed in **Figure 3** (note that the horizontal axis in Figure 3 is logarithmic). Look first at the column labeled "none." This, in effect, illustrates the temperature of the pad or plane alone. With no pad or plane, the heated pad on the top layer has a temperature of 83.1° (a 63.1° increase above the ambient). The dielectric on the bottom layer has a temperature of 79.2°, about 4° lower than the top layer.

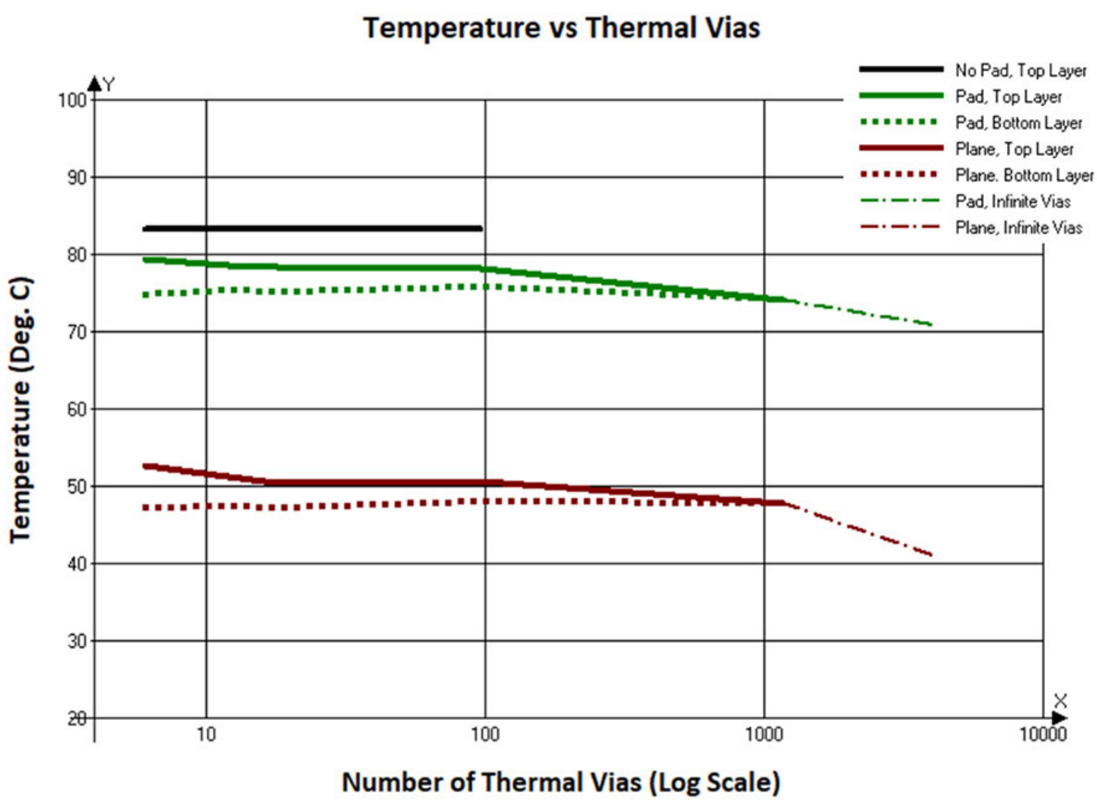


Figure 3. A visualization of Table 1's data.

This result is almost universally true; PCBs are so thin that the thermal image of the bottom layer looks very similar to, and only slightly cooler than, the top layer if there are no intervening planes. If a pad is on the bottom layer (of size equal to the heated pad), the top layer and bottom layer temperatures change slightly (here by about 3° and 6°.) But if we add a plane on the bottom layer,[5] the temperature on the heated pad drops considerably. In this case, the temperature drops by 28.5°. Our assumed ambient temperature is 20°, so if we look at *relative* temperature *changes*, we have (83.1-54.6)/(83.1-20) = 28.5/63.1 or by about 45%. This is not untypical of the effect any plane has in any thermal study, whether it involves heated pads or heated traces.

This impact should not be lost on the engineer or PCB designer. Simply adding an underlying plane lowers the temperature of a heated pad by 40-50%, far lower than any number of thermal vias possibly can. And it also should not be lost on the reader that the vast majority of boards today *already have* internal or bottom layer planes.

Next, look at the horizontal lines in the table grouped along the label ("no pad"). These are the columns for the number of thermal vias from the heated pad to the bottom layer. In these cases, if no lower pad or plane is present, the thermal vias have almost zero effect. The temperature of the heated pad does not change no matter how many thermal vias are added. This can also be seen by the black line in Figure 3. There is no slope to that line at all. The purpose of a thermal via is to conduct heat away from the heated pad *to* somewhere else. But in this case, there is no place to conduct the heat.

The other two cases are more interesting. Thermal vias (if we use lots of them!) appear to have some impact. The first six thermal vias lower the pad temperature from 80.4° to 79.3° in the case of a lower pad and from 54.6° to 52.6° in the case of a lower plane. The next six thermal vias lower the temperatures by another 0.7° and 1.3° respectively. And the next six thermal vias by 0.8° in each case. As more vias are added, the temperature of the lower pad or plane increases slightly. The cost of this improvement is the loss of a significant number of routing channels internal to the board. We don't consider this to be an effective use of board area.

It should be noted that each thermal via contributes a little less than the previous one, at least after a few thermal vias. That is, the marginal contribution of each additional thermal via decreases. We can see why this must be true by looking at the heat transfer formula, Equation 1.

$$Q/t = kA(\Delta T)/d$$

Eq. 1

Where:
Q/t = rate of heat transfer (watts, or joule/sec)
k = thermal conductivity coefficient (W/m·K)
    About 0.6 for FR4
    About 385 for copper
ΔT = change in temperature (°C = °K)
A = Overlapping area
d = distance between pad and plane

If a thermal via is effective, it lowers the temperature of the heated pad. If the temperature lowers, then the ΔT term in the equation goes down, so the heat transfer must go down. Therefore, if one thermal via is effective, the next one, by definition, must be less effective. That is why the slopes for the pad and plane sections in Table 1 decline exponentially.

At some point, the temperature on the heated pad and the underlying pad or plane must be approximately equal. In this simulation that appears to be in the range of 800 to 900 thermal vias. At that point there can be, by definition, nothing further to be gained by adding more thermal vias. Why, then, does our simulation show that in both models the temperature continues to decline? The answer may surprise you. Everyone (it seems) looks at thermal vias from the standpoint of the conductive cross-sectional area of the via, the part at the bottom. But the via also has a cylindrical wall made of copper that is in contact with the board dielectric. In this model the surface area of that wall is approximately 28 times greater than the conductive cross-sectional area! For any individual thermal via that is inconsequential, because the wall is in contact with the dielectric (whose thermal conductivity coefficient is equal to or less than 1.0) while the cross-sectional area is in contact with a material whose thermal conductivity coefficient is equal to about 385. But if a large number of additional thermal vias (in this case approximately 3,000 more!) are added, then the wall contribution finally begins to show an effect.[6]

Lower Heat Sink

What if we had a lower pad that was a heat sink? Then might thermal vias be more effective? We simulated the condition of a lower pad with a constant temperature of 20°, equal to the ambient temperature. This lowered the heated pad temperature to 33.4°, significantly lower than any other case. Interestingly, the bottom pad held at 20° everywhere, but just off the pad the temperature rose slightly. This is a direct result of the fact that the top pad heated the area around and away from the pad itself, and that heat flowed vertically down to the lower pad, just off the heat sink.

One might argue that in this case thermal vias would be more effective since their lower end would be connected to the sink itself. But why would you consider thermal vias (and their costs) in a situation where the heat sink itself has already lowered the heated pad temperature so dramatically? We think you would have to hypothesize a very unusual case where the addition of thermal vias would be required and effective.

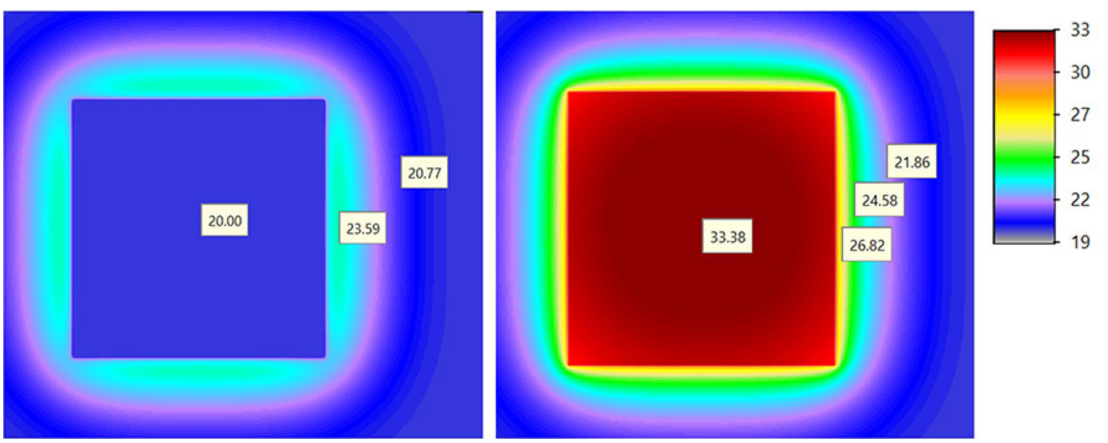


Figure 4. A heat sink drops the pad temperature dramatically.

Conclusion

Every board design is different. So, every application of thermal vias to a heated pad might be different. Nevertheless, we believe the *relative* trends in this simulation have very wide application across almost all heated pad situations. In general, thermal vias provide very little benefit, and do so at the cost of reduced routing channels on several layers. Much more benefit is to be obtained from the addition of a plane somewhere below the heated pad, and a great majority of current designs already have such planes. One might argue that if we could develop board materials with much higher thermal conductivity coefficients, then thermal vias would be much more efficient. But if we had such materials, the conductivity from the heated pad to a plane through that board material would also be much better, making the contributions from any thermal vias still only marginally beneficial.

Our advice: Stop wasting time and board area on thermal vias.

NOTES

1. See, for example, Brooks and Adam, *PCB Design Guide to Via and Trace Currents and Temperatures,* Artech House, 2021, Section 8.7, "Thermal Vias"; Brooks and Adam, "Thermal Vias: Maximize Effectiveness in PCB Design," *EDN,* Aug. 13, 2021; and PCB Via and Trace Currents and Temperature: Biggest Myths.
2. We used a simulation program called TRM (Thermal Risk Management), which was originally conceived and designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation. TRM is available here.
3. On an equivalent (round) via basis, the maximum number of vias that could be placed on this board is approximately 1,736. But that would not completely cover the surface. There would still be some nonconducting areas between the circular vias.
4. Our book, referenced in Note 1, covers this in numerous places.
5. Results would be similar if we added the plane on an innerlayer.
6. One revolutionary result of IPC-2152 is that current carrying internal traces are actually cooler than current carrying external traces with the same current. That is because the heat spreading in the board material creates a larger heated area for subsequent external convection or radiation. It should be noted that if we had a board material with a significantly higher thermal conductivity coefficient, all these results might be quite different.

DOUGLAS BROOKS, PH.D. has bachelor's and master's degrees in electrical engineering from Stanford and a Ph.D. from the University of Washington. He owned an engineering service firm and has published multiple books, including Physics of Electronics for PCB Designers and PCB Design Guide to Via and Trace Currents and Temperatures; doug@ultracad.com. **DR. JOHANNES ADAM, CID,** is founder of ADAM Research, a technical consultant for electronics companies, a software developer, and author of the Thermal Risk Management simulation program. View their recent video on Thermal Via and Trace Currents and Temperatures on the PCEA YouTube channel or at Printed Circuit University.

CONSORTIA

Connecting the Industry, from Boards to Assemblies

HDP is embarking on new rounds of evaluations of laminates and lead-free solders.

by MIKE BUETOW

The High-Density Packaging User Group, the nonprofit consortium of electronics manufacturers and suppliers that collaborate on various technical problems in order to reduce cost and time to market, has nearly 25 projects underway, several of which are due to be completed this year.

We spoke in March with Madan Jagernauth, marketing director and project facilitator of HDP, about its current research on lead-free solder alloys, its recent conference Best Papers, and whether the consortium members are ready to tackle artificial intelligence.

The following has been lightly edited for grammar and clarity.

Mike Buetow: It seems like 2024 is something of a transition year for HDP. You had your 30-year anniversary last year. You completed eight projects and you have 18 more now in the implementation phase. Let's start with the year just ended. As part of your anniversary HDP prepared four special retrospective reports. Can you summarize them and explain why HDP felt it was important to look backward as well as forward?

Madan Jagernauth says HDP's four technical retrospectives show the foundational research its members have produced over 30 years.

Madan Jagernauth: Well, Mike, 30 years is a long time for a consortium like this to be operating, so it was important for us to look back to see where we've come from and where we're going. There are lots of challenges in industry. A couple years ago we took a good look at the technical direction in the industry and the kinds of things that HDP should be working on and our members should be paying attention to as the industry evolves.

Looking back was us trying to get a sense of where we've come from. In the first decade HDP was a small group, about 15 members on average, so there were a small number of things that could be done. About 20 years ago, with the transition to more environmentally friendly materials, HDP became more important to members and grew to where we are now – about 50 members – and did some really good work starting about 20 years ago in lead-free alloys, some very seminal work on SAC 305 and SAC 405 in the early days, writing implementation guides and those kinds of things. The first thing I looked at was what we did on lead-free solder assessments over the years, and there were some very important sets of projects, reports written and used by our members.

At the time that lead-free solders came on the scene, no materials for lead-free printed circuit boards were really reliable, so the evaluation of laminate materials became very important, to [be able to] say which of these would actually work with higher temperature solders because the reflow temperatures for those lead-free solders were much higher than the reflow temperature for eutectic tin.

Starting about 2006, HDP has been running material evaluations for laminates and we're on our seventh phase now. That's the second part of looking back at what material testing we did over time.

And then, of course, there's all the other associated technologies that evolve over time for printed circuit boards themselves, with microvias, higher density vias and stacked vias, and the assembly technologies of how you actually put components on boards. Those are the four legs that I looked at as I was taking a retrospective and then relating that to how we go forward with our technical direction on the next generation of high-speed materials and evaluating those, the next generation of solders and evaluating those, the higher copper densities and what's coming with those. With all of this change, what changes are needed to the reliability assessment methodology as you get to things like higher voltages on printed circuit boards for electric vehicles or other types of applications? It all relates back to where we've come from, where we are today and where we're going.

MB: I know that HDP keeps its reports generally in house. They are done by the members for the benefit of the members. Was there any thought given to making the retrospective reports available to a wider audience?

MJ: Yes, those are available on our website. I published a couple of them through LinkedIn. They basically say what we have done. They don't cover the results of what we've achieved.

MB: Let's talk about the recently completed projects. What highlights can you share about those?

MJ: There's a lot of work on things like microvia reliability, the way boards stack up and the flatness reports, new technologies like photonic soldering, so a variety of projects were completed last year. We completed eight projects last year. We have 18 in implementation right now. When you look at it, there are six projects related to materials, primarily high-speed materials. There are four projects related to solders, two are related to the reliability of solders themselves and two are to the application of these solders: reflow reliability and rework reliability. There are four projects related to higher copper densities for backdrill, one of them with microvias and two with innerlayer copper balancing, and then there are two or three projects related to different test methodology like next-generation surface insulation resistance testing, one on copper roughness. When I look at the four or five legs of our technical direction, and the fit of the projects to the technical direction, about two-thirds of our projects are in line with where we see the technical direction of the industry pointing. There are of course some projects for which members have very specific near-term issues they're trying to address and they have commonality with other members, so those get into the mix as well.

MB: HDP has 23 projects underway, and as you noted, 18 in the implementation phase. These projects are approved by the HDP board of directors and going forward are restricted to HDP members and select others that have signed the R&D participation agreements. So implementation really is where the rubber hits the road, so to speak. You mentioned a couple that were recently completed, but you have a few in areas that are constantly evolving, like high-speed materials and next-generation solder alloys. What can you tell us about those?

MJ: We're in the seventh phase of our materials evaluations right now, which started in 2006. Through Phase 6 we completed evaluations of 85 different laminate materials. Phase 7 is testing of 11 more materials, and this tends to be a two-year project. The completion date is set for 2025 because those running this know that to do a complete set of testing on this set of materials takes a long time. These are major projects that require a lot of member participation and lots of very detailed testing. What was done for that as well is that the test vehicle that was used previously was updated to include new test coupons. That's very important for our laminate materials suppliers or fabricators. Everybody in the chain is very interested in that project and usually that project gets the highest participation among members because it creates such foundational knowledge for our membership.

Two others I'll mention [involve] the solder evaluation. We have been evaluating third-generation solders for about eight years; I think the evaluation for third generation started in 2016 and was completed around 2019 or 2020. And this is a collaboration we're doing with iNEMI. In first phase of this evaluation the thermal cycling was done for 10 minutes dwell times of the two extremes. There were three different thermocycles. There was also some vibration testing done to see if that kind of a test would actually affect the reliability of the solder. That was done three or four years ago.

The second phase started then, and the focus was some of these solders which have to operate for extended durations at high temperature, so there was a desire to test for a longer dwell time. Instead of 10 minutes of the extremes, it was increased to 60 minutes at the extremes, adding essentially 100 minutes per thermal cycling to this process. These are very reliable solders. You had 100 minutes to cycle. It takes it to a much longer cycle. It's more boring than watching a pot boil. It's like watching grass grow. But the good news is solders are very reliable. We're in the middle of that right now.

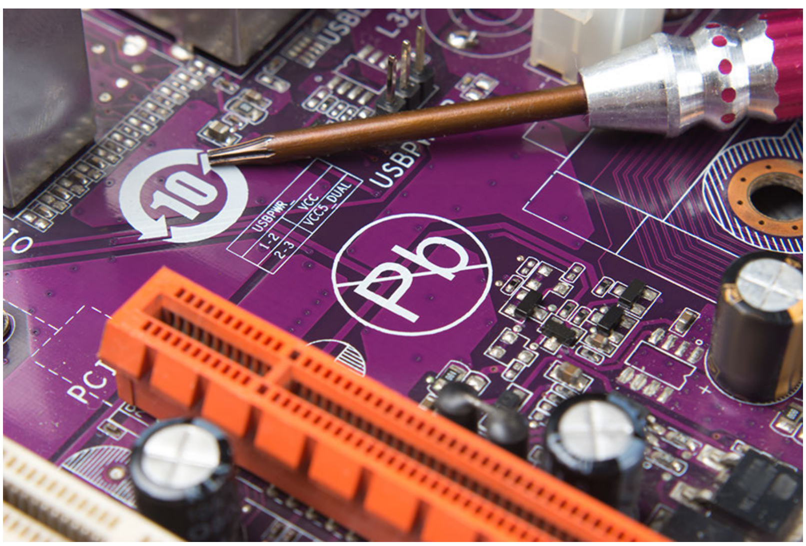
Then there is a third phase that's running in parallel that is looking at saying well, there's a traditional way of thermal cycling that limits the rise time of the cycle. If we did a shock test, would that change the reliability of the material? Would you have the same failure mechanisms and could we substitute a faster rise time to complete this kind of evaluation faster? This is a big part of providing information to our members on the third generation of solders. Some people are still specifying tin-lead. What we're seeing is this current-generation solders are very reliable but when the testing is done – which I'm sure we will get done to some point – we will see what the results really are that can be published. The intent of course with something as big as this is to publish as much as we can.

MB: How is it decided which materials are included? Does it require participation by the material supplier?

MJ: When we launch a project we will notify all our members and invite them to participate in a project. The ones who want their materials to be part of it, in terms of solders, will say “yeah,” and they will provide materials and which one of their solder compounds they want to evaluate. In the case of Evaluation 3, there was a desire to run a smaller set so that we didn’t have this big matrix. There was a subset of the ones from the second phase of evaluation that went into the third phase of evaluation. Then of course it’s a question of which of our laminate suppliers would participate in providing materials for the test vehicle, [and] which one of our fabricators would fabricate. In this case, the project is led by Richard Coyle from Nokia. Panasonic provided the laminate materials and Sanmina built the test vehicles. And then there’s the usual set of members – Shenju, Nihon Superior, Indium and MacDermid – providing the solders. I may be forgetting one or two.

MB: HDP has received a couple best paper awards of late, one in the area of fabrication and one in assembly. I think nothing better shows the breadth of HDP’s research.

MJ: Our members are doing really good work, Mike. I talked just now about the solder projects and the Evaluation Phase 2. The paper that was presented by [Coyle] at SMTAI last October, titled “A Collaborative Consortia Project to Assess the Effect of Thermal Cycling Dwell Time on the Reliability of High-Performance Solder Alloys,” is the one that we’re doing the 60-minute dwell time on. This is a collaboration between HDP and iNEMI. Testing is being done by Nokia, Collins and CALCE for this particular phase of the project. It’s a big effort across a large number of industry participants who are very interested in the results of this type of testing. And all [Coyle] presented was a status update on where this project is. I came into HDP about three years ago and took over this project and have been working as a facilitator for that period. And we are still in the middle of testing. Not all of the testing is done. The test vehicle is very interesting. It’s got two components on it, a 192-pin BGA, and an 84-pin BGA and as you’d expect the 192-BGA that’s larger fails first and the 84-BGA device sometimes takes forever, especially with the 0° to 100°C cycle, it takes forever to fail.



Despite its roots in PCB technology, HDP has been a force in evaluating Pb-free alloys.

MB: I really think that this underscores the importance of HDP as a collaborative organization. There is no other organization I can think of that is doing this type of broad-based research with this many members, and consistently producing results. If I go back 30 years, I think most people thought of HDP as a board interconnect organization. As I look over what your research has been over the past several years, nothing could be further from the truth. It really is very broad-based and you're filling a gap that is badly needed.

MJ: I think what members see is that they can run projects through HDP that they are not able to run themselves efficiently inside of their companies, either because it will take too long or they don't have the right set of resources all within the four walls. When you look at a project like that one from the material suppliers all the way to the fabricators and the test houses and then you look at the next ones, the ones that will be presented at IPC Apex [in April 2024], those papers are basically another reflection of what we're doing. The HDP paper that won Best of Conference includes device sizes from 26 sq. mm to 100 sq. mm. Eight different laminate materials, eight fabricators that made these test vehicles looked at the surface topology variations as you look at packet size changes, the way copper is distributed on the various layers, the resin field rates because if you have a high flow versus a low flow resin, it'll change what happens in ground planes versus via fields.

And then, how do you get to a point of designing something like this where you can actually balance the copper to get the flatness you need to assemble large BGA devices? This is of high interest to many people as they look at larger integrated circuits being put on printed circuit boards and the boards are getting thicker because you're going to higher-speed devices, more I/Os in the boards … all of this is interrelated. You've got what I would say is a highly stochastic system that you're trying to control. There are many variables in there that I don't know you can control all of them at any given time. There's always going to be some variability. But how do you manage it as you gain more knowledge about what you can do in the design to get the results you want? This [paper] is one that was written by Gary Brist and Neil Hubble; Gary is with Intel, Neil is with Akrometrix. This is where the interest is right now.

MB: Have your members asked about starting a project in artificial intelligence?

MJ: No, but I mean, what's artificial intelligence? Seriously. There are three elements in networks. There's a compute part, there's the storage part and there's a transmission part; networking. Networks are getting faster. The next generation of wireless and optical networks are running at very high speeds. The 1.6 terabit per second network is going to require baud rates of 112Gb. The next-generation wireless networks, they're talking about sub-terahertz spectrum, from 90 to 300GHz. Try doing that on printed circuit boards. This is where the interest is, so one of the projects we are running now is looking at the effect surface treatments have on high frequency and that will be tested up to 120GHz, I believe, because as you get to those speeds, you're talking about some major skin effects and when you've got an immersion gold or whatever else on top of the copper, where does current actually run? Does this layer of surface treatment affect the performance of that circuit? Things like that are being done right now.

MB: Most of your biannual meetings take place in the US, if memory serves. Your spring meeting this year, which takes place in May, is in Taiwan. Is that unusual?

MJ: Before Covid HDP was doing one [meeting] in North America, one in Asia and when we had a lot of members in Europe, one in Europe. Now we're doing the annual meeting in February in North America, the spring meeting in May/June in Asia, and then a virtual meeting in the fall.

Ed: HDP's next meeting takes place May 21-23 in Taipei.

MIKE BUETOW is president of the PCEA (pcea.net); mike@pcea.net.

Exploring the Impact of AI

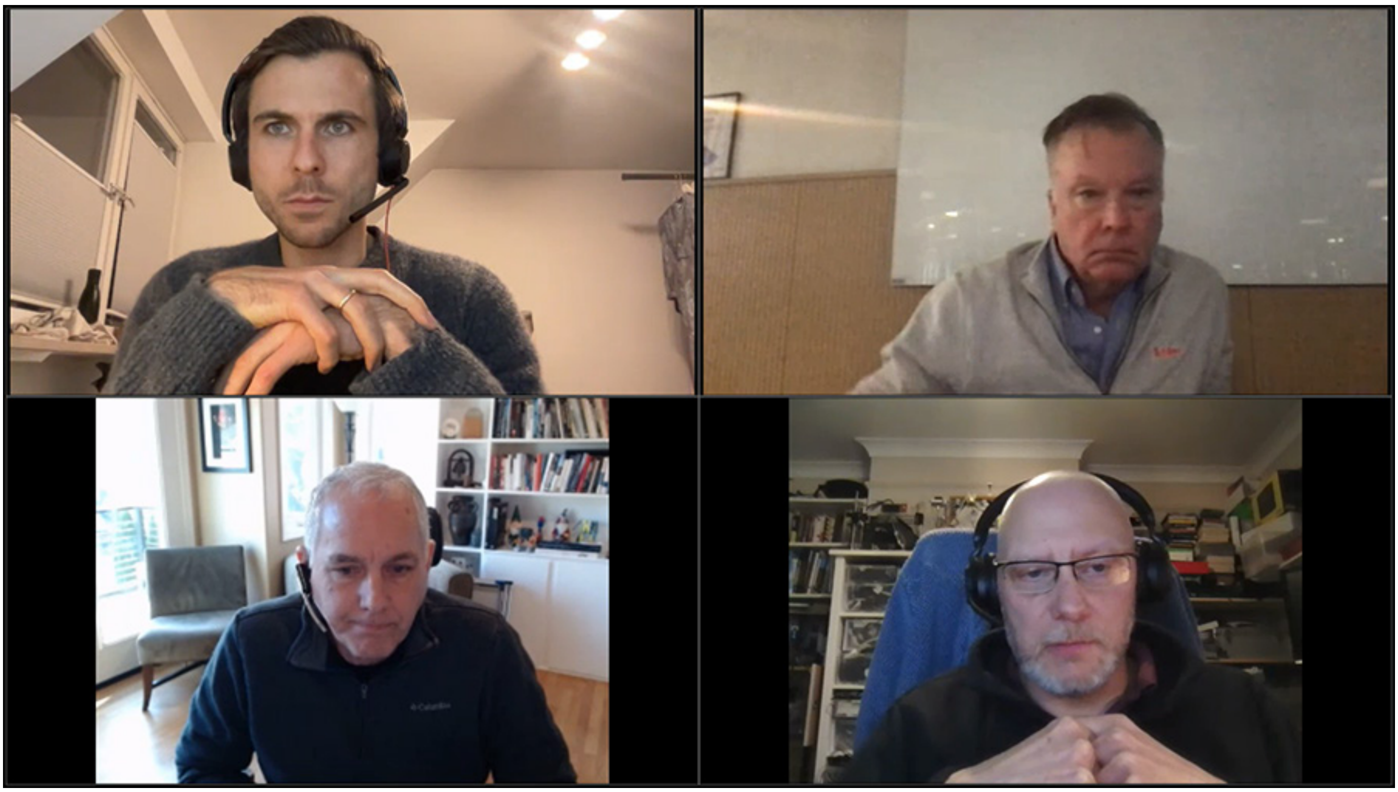
A special panel discusses the growth of AI tools and its possible effects on the industry.

by TYLER HANES

"Will AI take my job?"

That's the question on the mind of many around the world today – including electronics engineers and PCB design engineers – and was one of several questions considered during an online panel hosted by PCEA in March.

A group of panelists with notable AI experience – Circuit Mind's Tomide Adesanmi, Cadence Design Systems' Taylor Hogan, Zuken's Kyle Miller, Luminovo's Sebastian Schaal and Siemens Digital Industries' David Wiens – gathered to share predictions for the future of AI in the electronics supply chain and answer questions from an audience of industry professionals.



Panelists Sebastian Schaal, clockwise from top left, Taylor Hogan, Kyle Miller and David Wiens discuss the impact AI could have on the electronics industry during a PCEA-hosted webinar.

The 90-minute panel discussion was moderated by Phil Marcoux, who is credited with installing the first surface mount line in the US and is a subject matter expert in artificial intelligence process control and management for electronics assembly.

The panelists opened the discussion by addressing "the elephant in the room" as Marcoux described: Will AI take engineers' jobs?

Adesanmi gave a definitive answer to the question based on his own work at Circuit Mind, a developer of automated schematic tools.

"My first answer to this is if you think that AI is going to take the job of an electronics engineer in the next decade or so, you don't really know what an electronics engineer does on a daily basis," he said.

Adesanmi said he has mainly seen customers using AI tools to get answers and insights faster, such as choosing between Wi-Fi or Bluetooth in a design to stay under a power budget, and then taking those answers into account for their design.

"Engineers are using this sort of AI tool to get a full idea of what they can accomplish very, very quickly," he said.

Schaal, cofounder of Luminovo, a developer of an AI-driven component sourcing and BoM platform, sees the potential for AI to resolve communication bidirectionally between design and manufacturing.

"If you have a business relationship where an OEM, an EMS and the PCB manufacturer are working together, and they are willing to open their notes, then those profiles can be shifted left into an earlier process … where designers can then upload their design tool files, and you can see that 360-degree view on the supply chain. That's something we can provide to the whole design intelligence ecosystem."

But while AI tools can look at a list of components and requirements to make a list of possible combinations on a board, it still comes down to the engineer to use their own creativity and experience to ensure the design works, Adesanmi said.

"The engineer remains the architect," he said. "They remain the experts that make this more reliable in our use case, and they remain the verifier of the design in the end."

Miller, the architect behind Zuken's new AI-powered ECAD router, echoed Adesanmi's prediction of at least 10 years before AI has a real impact on design jobs, and he said engineering fields are more likely to be under threat before electronics or design engineers.

"Software, for example, is probably going to be one of the first ones to go," he said. "And it purely comes down to available data."

Because there are plenty of examples of code around the internet, AI will have a much easier time training itself, but the PCB design industry's lack of shared data may prove to be a saving grace for designers, Miller said.

Another factor to consider is that designers' roles continue to change, said Siemens' Wiens, who leads a product marketing team and has more than 30 years' experience in EDA.

The work they are responsible for has continued to increase throughout the years, so engineers will likely be viewing AI as less of a threat to their jobs and more as another helpful tool to help them do their jobs, he said.

Experts say AI will accent, not replace, humans' roles in electronics design and engineering.

With the demand for electronics increasing and the industry workforce at best staying stable and maybe even decreasing, taking advantage of AI as a toolset may be the only way to keep up with that demand, Schaal said.

"One of our largest customers basically said 'Look, we see that the electronics manufacturing industry continues to grow, but we just can't find the people to sustain that growth. The only way we can sustain it is by radically focusing on automation,' " he said.

Marcoux also asked the panelists what they would consider to be the "gold ring" of using an AI tool within the industry.

Taylor, a distinguished engineer and product architect at Cadence, said he believes that software is the determining factor in producing better PCBs.

"If the software was better, we could generate more designs quicker for evaluation," he said. "So my goal in life is to bring the automation of PCB design up to the point where I see design is today."

He said he doesn't believe that will reduce the number of designers or engineers, but it will change how they do their jobs.

When looking at a design that a human made, the rules don't always correlate with the board, he said, and sometimes there is a tribal knowledge about which rules are truly important and which ones work well. Because AI doesn't have the leeway to make those kinds of decisions, designers will need to do their jobs differently – but that will afford much more productivity.

"I don't think it's going to begin with the click of a button and the magic happens," he said. "I think it's more like a co-pilot."

Opening Up to AI

The panel also received questions from the audience, including one that asked what skills could be important for designers to learn to keep up with AI.

Wiens said the easiest way to prepare for the future is to come to it with an open mind.

He said anyone who has been involved in the industry long enough has been a part of a newly-introduced product that has had low adoption – particularly when automation is involved.

"A lot of times it's because teams have their established processes and, frankly, are too busy to consider new ones. So as a result, opportunity goes by." he said. "I think having an open mind, thinking about AI as an opportunity, not as a threat, is the biggest thing that designers and engineers can consider as they move forward."

Adesanmi said he sees two different ends of the spectrum with AI, either as a generalist or as a specialist, and for the best success, engineers should gravitate toward one end or the other rather than stay in the middle.

Being a generalist who has experience in several different fields should allow an engineer to become a supervisor of AI tools who manages processes throughout the production line, but on the other side of the spectrum, there will also be a need for specialists who can handle processes that AI can't, he said.

"The way I think about it is that if you can put yourself on one end of the spectrum and not dilly-dally in the middle of it, you will probably find a path to the future," he said.

For many disciplines, the key to lasting in the industry is being willing to change your tool stack, Luminovo's Schaal said, and while electronics engineers haven't always had to change their tools as often as others, that looks to be changing.

"I think adaptability is something you desperately need," he said. "Being able to work with different tools and rethink how you've done processes, I think that's key."

Cadence's Hogan also stressed patience as AI grows and develops, and said working with EDA companies that are asking how and why certain designs work will help improve the process and provide a valuable tool.

"This is only going to make you more productive, but you're going to have to give up the notion that just because it doesn't look like something you did, it's not good," he said.

Ed: The entire panel discussion is available here. To keep up to date with PCEA's free webinars, sign up for a free membership at pcea.net/pcea-membership-info/.

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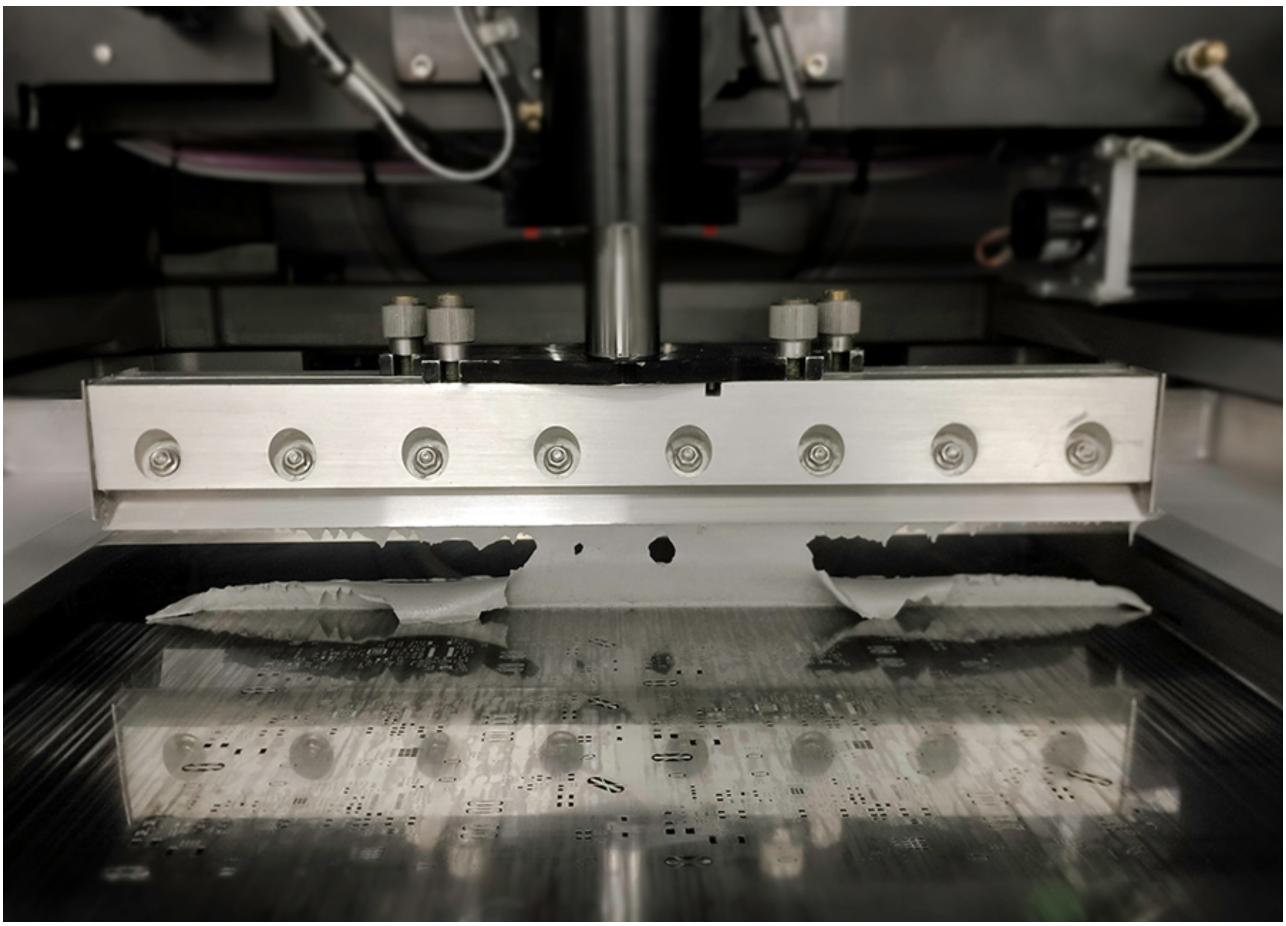
Preserving Solder Paste Integrity

A closer look at mixing methods and automated mixers.

by GAYLE TOWELL

While automation in manufacturing brings efficiency and consistency, the use of automated solder paste mixers is a topic of debate, with significant concerns over their impact on the paste's properties. This comprehensive analysis delves into why many industry experts advise caution.

Solder paste is not just a blend of materials; it's a finely tuned compound where each element plays a specific role. The balance between solder powder and flux is crucial, as it determines the paste's behavior during the printing process and affects the quality and reliability of solder joints. Certain properties of the paste – its viscosity, rheology and thixotropy – fundamentally determine how well it will perform and can be significantly affected by how the paste is handled.



The mixing approach can be tied to changes in solder paste properties and, ultimately, performance on the line.

In solder printing, the right viscosity ensures the paste can be deposited accurately without spreading. Rheology involves the study of the flow and deformation of the paste and is essential for understanding how the paste behaves under stress during the printing process.

Thixotropy, a specific rheological behavior, refers to the property of certain fluids to become less viscous under applied stress. In the context of solder paste, this means it becomes fluid enough to be printed through stencils but then thickens to hold its shape once the stress (like the squeegee's movement) is removed.

Overmixing or mixing under high shear conditions, as seen in some automated mixers, can permanently alter the paste's viscosity and thixotropy. This can lead to issues such as slumping or spreading of the paste on the board, which can cause defects in the solder joints.

Pitfalls of Automated Mixers

Because of the complexity and balance in most solder paste formulations, it's important to understand how mixing methods impact its properties. Automated mixers, often perceived as efficient solutions, can pose significant risks to the integrity of solder paste due to their operational mechanisms and effects.

High shear stress. Unlike manual methods, automated mixers apply high shear stress to the solder paste. This stress can lead to a phenomenon known as shear thinning. In this state, the paste becomes excessively fluid, negatively impacting its ability to retain shape and form reliable joints.

Temperature changes. The operation of automated mixers can generate a considerable amount of heat, leading to an increase in the temperature of the solder paste. Note that some sources suggest this heat generation is a benefit in that it permits cold paste to reach room temperature faster, but this heat is generated by friction as opposed to natural conduction heating of paste set out at room temperature. Frictional heating can cause rises in temperature that can prematurely activate the flux or accelerate the aging of the paste, both of which are detrimental to its performance.

Inconsistent mixing across formulations. Automated mixers might not achieve uniform mixing across all solder paste formulations, particularly those with varied particle sizes or compositions. This lack of uniformity can result in unpredictable solder paste performance, with some areas of the paste potentially having different properties than others.

Perceived benefits are often illusory. Many automated mixer manufacturers emphasize the speed of preparation along with the uniformity of the paste after mixing. It's important to note, however, that the state of the paste after mixing is not the same as the state of the paste after being idle for a while or during a print pause. This is because the forces involved in mixing cause a combination of changes to the paste's rheological properties. Some of these changes are temporary and sustained only in the immediate aftermath of those extreme forces. (Other changes are permanent, but not in a good way – such as partial flux activation or solder sphere deformation.)

The Evidence: Real-World Implications of Automated Mixing

While empirical studies directly linking the use of automated mixers to solder paste performance issues are limited, a wealth of anecdotal evidence and professional experiences paints a clearer picture of their potential impact.

Many process engineers and technicians have reported challenges with solder paste performance that correlate with the use of automated mixers. In contrast to automated mixing, manual or proprietary mixing methods, which prioritize precision and control, have consistently demonstrated their ability to maintain the quality of solder paste.

Furthermore, there are instances where reverting from automated to manual mixing methods has resulted in observable improvements in solder paste performance. The consensus among many experts is that while automated mixers offer convenience and uniformity in preparation, they lack the nuanced control necessary to preserve the delicate balance of solder paste properties.

Mixers Used During Solder Paste Manufacturing

It's important to note that manufacturers of solder paste do not use simple hand mixing techniques. Instead, they utilize proprietary blending processes that cannot be considered analogous to any blending done by automated mixers to prepare paste for use in an electronics production setting.

In contrast, these mixers are calibrated to ensure stable temperatures and consistent mixing, factors that automated mixers often lack. Every part of the process is carefully measured and refined and kept consistent from one batch to another, ensuring the paste produced is uniform and meets all the required specifications. The paste made in this way is also thoroughly tested after blending to further ensure it maintains its intended properties.

Best Practices for Solder Paste Preparation

The best practices for solder paste preparation involve a careful and controlled approach, with a strong emphasis on manual techniques and strict adherence to manufacturer guidelines. By following these practices, electronics manufacturers can ensure the solder paste retains its intended properties, leading to better quality and reliability in the final electronic assemblies.

Manual mixing: A preferred approach. One of the key best practices in solder paste preparation is the use of gentle, manual mixing methods. Techniques such as lightly stirring the paste with a plastic spatula for a minute or more can be highly effective. Permitting the paste to reach ambient temperature before mixing is also essential, as it ensures the paste's properties are not altered by sudden temperature changes.

Avoiding mixers for paste warming. Using mixers to warm solder paste directly from refrigerated storage is not recommended. This practice can cause uneven heating and potentially damage the paste's properties. Instead, the paste should be allowed to gradually come to room temperature in a controlled environment.

Adherence to manufacturer guidelines. Manufacturer guidelines are often based on extensive research and understanding of each formulation's tolerance to different mixing methods. Look for each manufacturer's specific instructions on the amount of time and type of mixing tool to use, ensuring the best possible performance of their product.

Automated mixers are often marketed for their ability to provide consistency in preparation and save time. Manufacturers of these mixers tout benefits such as airtight containers to reduce oxidation and humidity concerns, automated operation for even and gentle softening of the paste, and the capability to prepare paste for printing in significantly less time. These features can be particularly attractive in high-volume production environments where time efficiency is a critical factor.

What mixer manufacturers tout and what happens on the production line can be significantly different, however. While embracing innovation is key in the electronics manufacturing industry, it's crucial to balance it with traditional practices that have proven effective, particularly in the context of solder paste preparation. While some formulations might tolerate automated mixing, others may demand the gentle and controlled environment of manual mixing. It's essential to recognize these differences and choose the mixing method that aligns best with the specific requirements of the paste in use.

For those who choose to use automated mixers, conduct thorough testing to understand the impact of the mixer settings on the solder paste and its overall performance. Testing should include assessing changes in the paste's viscosity, rheology and thixotropy after mixing, as well as evaluating the solder joints produced for quality and reliability.

In conclusion, while the innovation represented by automated mixers offers certain advantages, it is essential to weigh these against the proven effectiveness of traditional mixing methods. Balancing these two approaches, while staying informed about the specific needs of different solder paste formulations, is key to achieving high-quality and reliable results in electronics assembly.

GAYLE TOWELL is content specialist at AIM Solder (aimsolder.com); gtowell@aimsolder.com.

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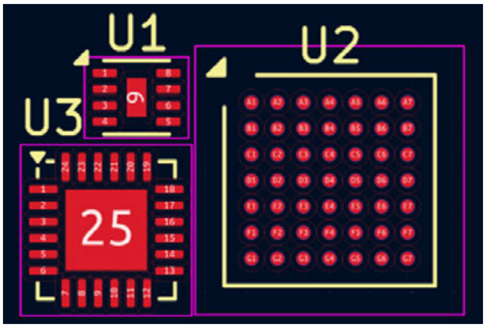

KICAD 8.0 ECAD

KiCad 8.0 features hundreds of bug fixes, performance improvements and other smaller changes since KiCad 7. Includes improvements to the official KiCad libraries, expanded support for importing data from other tools, new possibilities for data export, improvements to the command-line interface, improvements to documentation and other smaller changes. Also features numerous improvements to schematics and symbols, including new UI panels for properties, net navigation and search, as well as a new BOM exporter. Simulation improvements include a simulator UI overhaul and new features, and PCB and footprints improvements include multiple footprint dragging, interactive length tuning patterns, a 3-D viewer UI overhaul and other smaller changes.

KiCad

kicad.org

KYOCERA AVX 9159-600 SERIES CONNECTORS

9159-600 dual-row inverted through-board card edge connectors feature staggered contacts that enable four to 12 positions. Features a BeCu contact system that provides full 2.5A per contact current rating and low-profile (2.85mm above-board) through-board design supports applications with minimal height constraints on the mating side of PCB and doesn't interfere with LEDs. Staggered contact configuration prevents shorting and contact damage when inserting and removing mating PCBs, and is approved to UL1977 safety standards. Is for 1.6mm-thick mating PCBs with gold-plated pads and rated for 2.5A per contact, 300VAC, 10 mating cycles, and operating temperatures extending from -40° to +125°C. Features white, glass-filled, high-temperature, UL94 V-0 nylon insulators equipped with 4, 6, 8, 10, or 12 contacts, gold plating on the nose, and lead-free matte tin plating on the tails.

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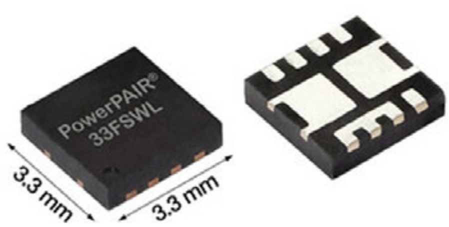

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SiZF4800LDT 80V symmetric dual n-channel power Mosfet combines high and low side TrenchFET Gen IV Mosfets in a single 3.3 x 3.3mm PowerPAIR 3x3FS package. Can be used in place of two discrete devices typically specified in the PowerPAK 1212 package, saving 50% board space, and provides space-saving solution for synchronous buck converters, point of load (POL) converters, and half- and full-bridge power stages for DC/DC converters in radio base stations, industrial motor drives, welding equipment and power tools. Offers on-resistance down to 18.5mΩ typical at 4.5V and 54% lower thermal resistance compared to competing Mosfets. Features continuous drain current of 36A, 38% higher than competing devices. Unique pin configuration simplifies PCB layout and supports shortened switching loops to minimize parasitic inductance. Is 100% Rg- and UIS-tested, RoHS-compliant and halogen-free.

Vishay Intertechnology

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Delo Industrial Adhesives

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GÖPEL MULTIEYES PLUS AOI

MultiEyeS Plus AOI now features an intelligent assistance function for THT placement. Features a 47MP image acquisition unit equipped with a flexible LED lighting system to provide very high image quality and detail resolution with an inspection area of up to 650 x 550mm. Verifies presence, position and color of THT components, reads labeled or laser-edged 2-D codes and barcodes, and recognizes text. Integrates a powerful laser projection into the AOI module for the assistance function, which makes it possible to intuitively support manual placement by displaying placement information directly in operator's field of vision, and displays faults detected during placement directly on the PCB.

Göpel Electronic

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HITACHI HIGH-TECH LS9300AD WAFER INSPECTION

LS9300AD inspects the front and backside of non-patterned wafer surfaces for particles and defects. In addition to the conventional dark-field laser scattering detection of foreign material and defects, is equipped with a new DIC (differential interference contrast) inspection function that enables detection of irregular defects, even shallow, low aspect microscopic defects. Has wafer edge grip method and rotating stage currently used in conventional products to enable front and backside wafer inspection. Is said to reduce inspection costs and improve yield for semiconductor wafers and semiconductor device manufacturers by providing high-sensitivity and high-throughput detection of low-aspect microscopic defects.

Hitachi High-Tech

hitachi-hightech.com

KITOV V. 2.7 INSPECTION SOFTWARE

Kitov's inspection platform version 2.7 includes upgrades for an enhanced user experience and expanded functionality. Features multiple components designed to enable smart inspection processes, including improved AI Trainer that permits operators without specialized expertise to rapidly gather and label defect data. Also features improvements to Planner Tool, including a more accessible interface, equipped with intuitive icons, tool tips, contextual menus and versatile features like an undo function for reversing unintended actions. Also includes improvements to CAD2SCAN functionality, including an expanded range of quality tests that can be applied to a CAD model, enhancing its ability to detect missing components; mark part edges, patterns and surfaces, and more. Workcell Configurator has also been updated to permit 70% quicker configuration and validation of robotic workcell hardware through a straightforward and intuitive user interface.

Kitov.ai

kitov.ai

MASTER BOND UV15RCL EPOXY

UV15RCL epoxy is a low-viscosity, cationic type UV curing system with a special color changing feature. Features a red material that changes to clear once exposed to UV light, indicating that there is UV light access across the adhesive material. Cures under UV light in around 30-60 sec. with a broad-spectrum UV lamp emitting light with a wavelength range between 320-365nm and a minimum required energy of 20-40mW per cm^2. Features a glass transition temperature (Tg) of 90°-95°C and when post-cured for 1-2 hr. at 125°C, Tg can increase to 125°-130°C. Has a service temperature range from -80° to +350°F, cures tack free and has a very low viscosity of 115-350cps, making it ideal for spin coating. Is not oxygen inhibited and provides light transmission properties and good optical clarity, with a refractive index of 1.517. Is also said to be an excellent electrical insulator with a volume resistivity exceeding 10^{14}ohm-cm.

Master Bond

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SNAPCHIP AI COPILOT

AI Copilot for electronic component sourcing uses advanced AI algorithms to streamline the sourcing process. Is said to speed improvements in component sourcing tasks: researching parts is now 50 times faster, finding the best quotes is 10 times faster, and identifying alternates is 100 times faster than traditional methods. Combines real time data from OctoPart with parametric data on +1 billion components from Silicon Expert, and uses GPT4 from OpenAI to deliver access to information retrieval and analytics.

SnapChip

snapchip.ai

SYENSQO SWYFT-PLY COMPOSITES

Swyft-Ply composite materials are designed to enhance design options for the electronic and smart devices market. Are said to leverage the benefits of composites such as weight reduction and strength to enable new form factors that are thinner and provide more design flexibility and freedom. Offers the ability to select important material features such as dielectric performance, thermal characteristics as well as UL94 flammability requirements. Are based on multiple polymer resin types and reinforcements, available in various material formats, and have been formulated to maximize processing efficiencies through fast curing, controlled flow and extended storage conditions.

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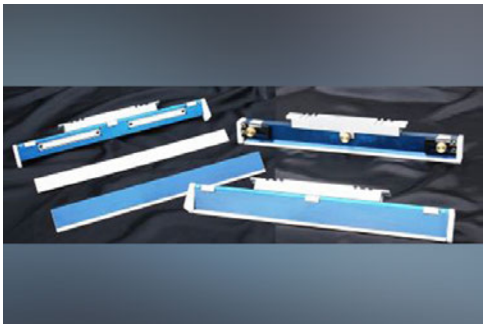

TRANSITION AUTOMATION SLIM-LINE 38 SQUEEGEE HOLDER

Slim-Line 38 squeegee holder now incorporates a magnetic locking system that replaces circular magnets with rectangular magnets, and a flux spreader shim has been added to help distribute the magnetic locking forces more evenly across the blade body and improves the blade change process by providing a smooth polished corrosion-free surface that easily receives and guides the blade to its reference pins.

Transition Automation

metalsqueegees.com

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400.1 series of air extractors is a set of energy efficient, modular and extremely low-noise extraction and filtration solutions. Includes various extraction systems for the removal of laser fume (LAS 400.1), soldering fume (LRA 400.1), odors, gases, and vapors (ACD 400.1), as well as dust and smoke (ASD 400.1), with at least two specialized filter configurations available for each area of application. Can be used mobile and stationary in a variety of manufacturing and machining processes. Features a unique filter inflow concept said to achieve a very high absorption capacity of the filter, plus an EC double blower (electronically commutated motor) with which volume flows of up to 600m³/h can be achieved while simultaneously maintaining a high negative pressure of up to a maximum of 9,800Pa. Also features sound insulation that enables a low noise level.

ULT

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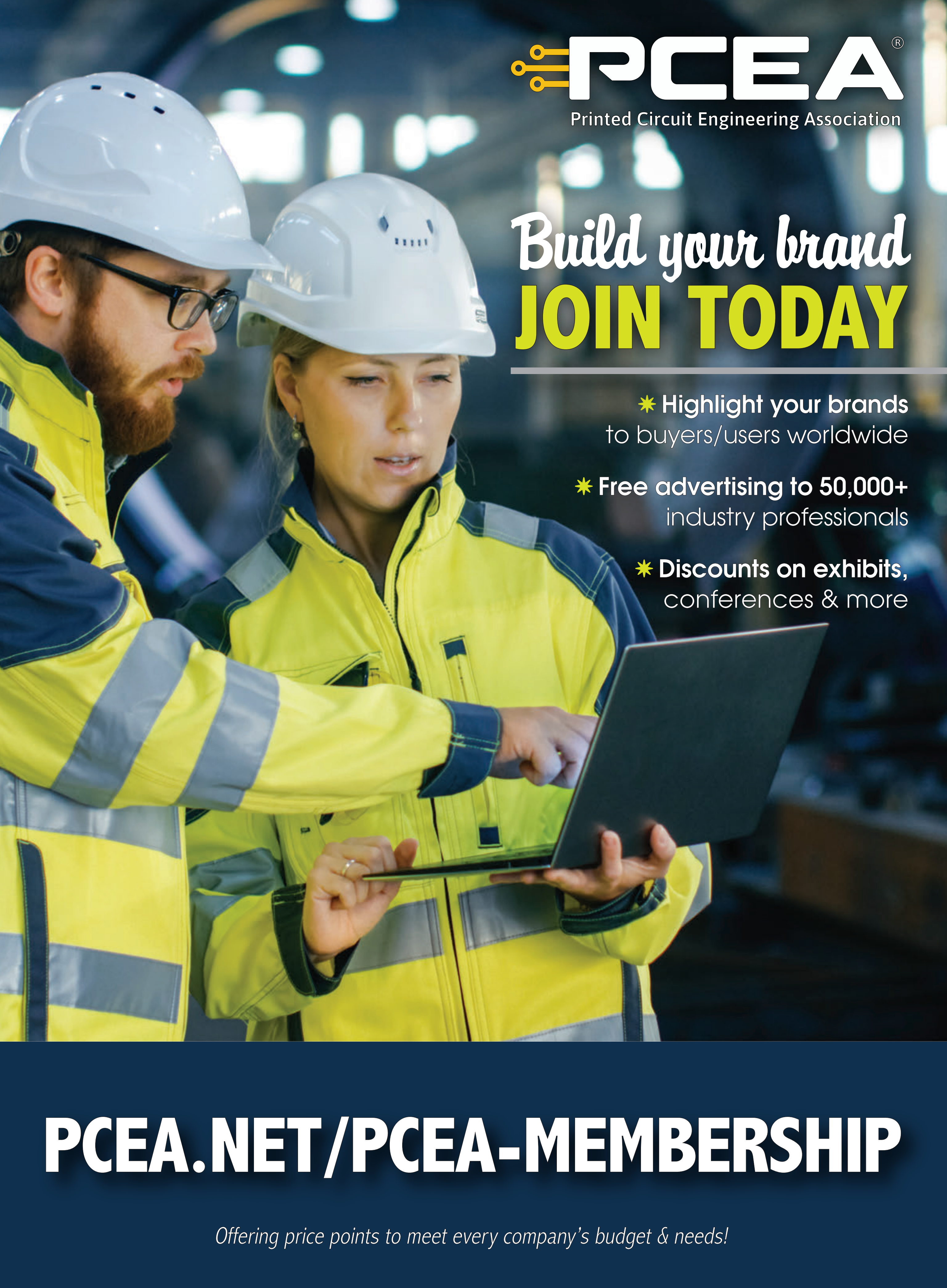
YAMAHA YRI-V AOI

YRi-V 3-D AOI now features faster board handling, multicomponent alignment checking and enhanced LED coplanarity measurement. Includes stopperless transfer system to brake and stabilize each board electronically after entering the machine, cutting the time to position the assembly ready for inspection. Also includes new multicomponent alignment check that simplifies programming to measure the distances between arrayed parts such as LED emitters in automotive or general lighting, and upgraded height measurement system uses a blue laser to ensure accurate and repeatable height assessment for components that are difficult to capture with standard equipment, such as transparent LED packages. Can now be equipped with 25MP top-camera system, which significantly expands the inspection area that can be imaged at one time.

Yamaha Robotics SMT Section

yamaha-motor-robotics.de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In Case You Missed It

Electromagnetic Compatibility

"High-Frequency Modelling of Electrical Machines for EMC Analysis"

Authors: Yerai Moreno, *et. al.*

Abstract: The trend toward electrification in mobility has led to increased use of silicon carbide (SiC) semiconductors. These semiconductors are more efficient but also present challenges related to electromagnetic interference (EMI) due to their higher voltage derivatives. This paper introduces a new high-frequency impedance model for electrical machines. The proposed model distinguishes itself from existing approaches by being entirely derived from finite element method (FEM) simulations, which include capacitances in the magnetic simulation. This approach achieves a balance between computational efficiency and high accuracy across the entire frequency spectrum, ranging from 100Hz to 50MHz. The model provides valuable insights during the design phase and was rigorously validated using data from 28 samples of an industrial machine. (*Electronics*, February 2024, https://doi.org/10.3390/electronics13040787)

Package Warpage Analysis

"Warpage Study by Employing an Advanced Simulation Methodology for Assessing Chip Package Interaction Effects"

Authors: Jun-Ho Choy, *et. al.*

Abstract: A physics-based multi-scale simulation methodology that analyzes die stress variations generated by package fabrication is employed for warpage study. The methodology combines coordinate-dependent anisotropic effective properties extractor with finite element analysis (FEA) engine, and computes mechanical stress globally on a package-scale, as well as locally on a feature-scale. For the purpose of mechanical failure analysis in the early stage of a package design, the warpage measurements were used for the tool's calibration. Warpage measurements on printed circuit board (PCB), interposer and chiplet samples, during heating and subsequent cooling, were employed for calibrating the model parameters. Warpage simulation results on full package represented by PCB-interposer-chiplets stack demonstrate the overall good agreement with measurement profile. The performed study demonstrates that the developed electronic design automation (EDA) tool and methodology can be used for accurate warpage prediction in different types of IC stacks at early stage of package design. (ISPD '24: *Proceedings of the 2024 International Symposium on Physical Design,* March 2024, https://dl.acm.org/doi/abs/10.1145/3626184.3635284)

Solder Fatigue

"Numerical Investigation of Thermal Fatigue Crack Growth Behavior in SAC 305 BGA Solder Joints"

Authors: Rilwan Kayode Apalowo, *et. al.*

Abstract: This study aims to investigate the reliability issues of microvoid cracks in solder joint packages exposed to thermal cycling fatigue. The specimens are subjected to JEDEC preconditioning level 1 (85°C/85%RH/168 hr.) with five times reflow at 270°C. This is followed by thermal cycling from 0° to 100°C, per IPC-7351B standards. The specimens' cross-sections are inspected for crack growth and propagation under backscattered scanning electronic microscopy. The decoupled thermomechanical simulation technique is applied to investigate the thermal fatigue behavior. The impacts of crack length on the stress and fatigue behavior of the package are investigated. Cracks are initiated from the ball grid array corner of the solder joint, propagating through the transverse section of the solder ball. The crack growth increases continuously up to 0.25mm crack length, then slows down afterward. The J-integral and stress intensity factor (SIF) values at the crack tip decrease with increased crack length. Before 0.15mm crack length, J-integral and SIF reduce slightly with crack length and are comparatively higher, resulting in a rapid increase in crack mouth opening displacement (CMOD). Beyond 0.25mm crack length, the values significantly decline, that there is not much possibility of crack growth, resulting in a negligible change in CMOD value. This explains the crack growth arrest obtained after 0.25mm crack length. (*Soldering & Surface Mount Technology*, February 2024, https://doi.org/10.1108/SSMT-08-2023-0049)

Substrate Characteristics

"Investigating the Influence of Substrate Orientation and Temperature on Cu Cluster Deposition"

Authors: Yiwen He, *et. al.*

Abstract: The crystal orientation and temperature of the substrate are crucial factors that influence clusters deposition and, consequently, the properties of thin films. In this study, the molecular dynamics simulation method was employed to investigate the deposition of Cu_{55} clusters on Fe(001), Fe(011), and Fe(111) substrates with varying crystal orientations. The incident energies used ranged from 0.1 to 20.0eV/atom, and the substrates were maintained at temperatures of 300, 500 and 800K. Analysis of cluster and substrate atom snapshots, along with the physical properties of clusters, revealed how the crystal orientation of Fe substrates affects the morphology and structure of the cluster at different temperatures. Additionally, specific microscopic mechanisms responsible for these effects were identified. The simulation results demonstrate that the crystal orientation of Fe substrate significantly influences the deposition of Cu_{55} clusters. The structures of the clusters on the three crystal substrates undergo similar changes as the substrate temperature increases, with the Cu_{55} clusters on the Fe(111) substrate exhibiting the most significant changes in response to the temperature rise. (*Journal of Applied Physics*, March 2024, https://doi.org/10.1063/5.0193758)