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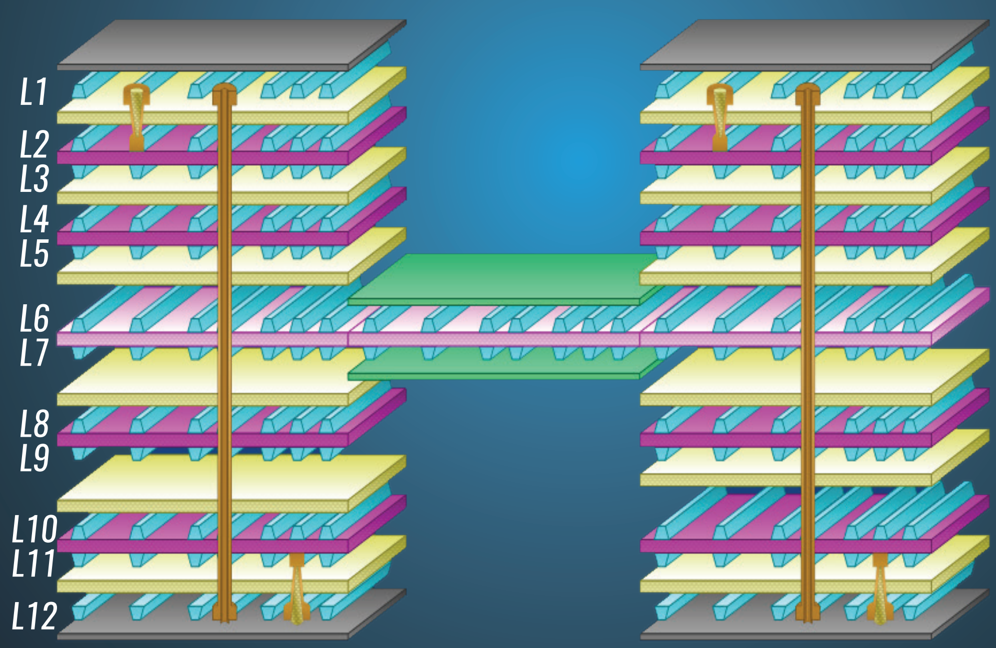

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ON PCB CHAT (PCBCHAT.COM)

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VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

PCD&F/CIRCUITS ASSEMBLY EDITORIAL

MANAGING EDITOR
Tyler Hanes 205-258-0067 | tyler@pcea.net

COLUMNISTS AND ADVISORS

Peter Bigelow, Robert Boguski, John D. Borneman, John Burkhert, Jr., Stephen Chavez, Geoffrey Hazelett, Mark Finstad, Jake Kulp, Nick Koop, Alun Morgan, Susan Mucha, Greg Papandrew, Chrys Shea, Jan Vardaman, Gene Weiner

PRODUCTION

ART DIRECTOR & PRODUCTION
blueprint4MARKETING, Inc. | production@pcea.net
Nathan Hoeller | nathan@pcea.net

SALES

VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

SENIOR SALES EXECUTIVE
Will Bruwer 404-313-1539 | will@pcea.net

REPRINTS

sales@pcea.net

EVENTS/TRADE SHOWS

EXHIBIT SALES
Frances Stewart 770-361-7826 | frances@pcea.net

TECHNICAL CONFERENCE
Mike Buetow 617-327-4702 | mike@pcea.net

EVENTS MANAGEMENT
Jacqueline Bress 404-955-7675 | jacqueline@pcea.net

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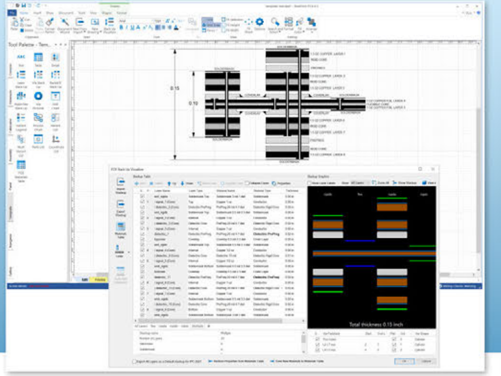

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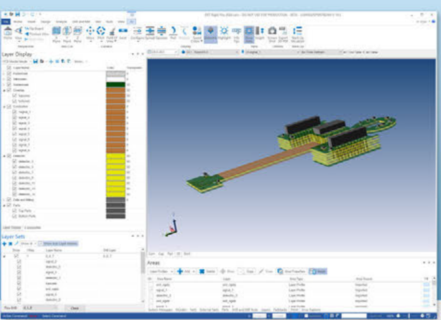
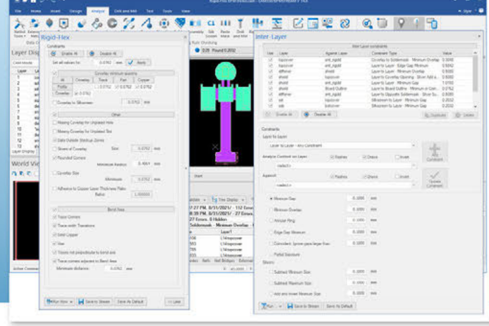


A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



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College Campuses are Aflame. Are Worker Protests Inevitable Too?

SEVERAL NOTABLE COLLEGES are undergoing crises on their campus as students, faculties and administrations wrestle with how – or even whether – to respond to events taking place far from home, in particular in the Middle East.

The ongoing protests on college campuses have brought to light many conflicting points of view, and generated tremendous reaction well outside the sphere of the student bubble. It's not necessary to recap all the outrage and countermeasures here. But there are obvious business implications that, in my opinion, merit some consideration.

Near the end of April, we welcomed Audrey McGuckin back to the PCB Chat podcast. McGuckin spent 22 years with Jabil in a variety of roles culminating as vice president and chief talent officer, and has experience living and working all over the world: Singapore, China, Taiwan, Japan, Germany, France, and Spain as well as the US, where she has called home for the past 25 years. Her eponymously named consulting group offers advice on strategy, operations, and human resources to executives across a variety of industries, including many in companies in the electronics supply chain.

A proponent of strategic solutions to workforce development, training and issues, McGuckin is not afraid of tackling the more complex personnel issues head-on.

To wit, McGuckin not long ago addressed in her blog another complexity that many businesses had to understand and develop ways to address. Specifically, she looked at why DEI (diversity, equity and inclusion) programs are failing in many organizations, an outcome she asserts can result when the program goals don't fit the business context, or that they are the proverbial solution in search of a problem.

So it was only natural, then, to ask McGuckin about possible parallels between what's happening today at US schools and the DEI programs in business environments in terms of the strategies business leaders *could* use to address them and the perhaps lack of a playbook for doing so.

These are not unreal scenarios to businesses. Over the past few years, we have seen numerous instances of workers pushing even their blue-chip employers for changes well beyond their day-to-day responsibilities.

No Tech for Apartheid, an activist group that has singled out Amazon and Google as war profiteers, occupied Google offices in multiple states last month to protest a $1.2 billion cloud computing contract the company was awarded by

the Israeli government. (After nearly 30 workers staged a sit-in protest, Google's response was to fire them.)

But that's just the most recent of myriad instances where workers in the electronics supply chain have used demonstrations to make their voices heard. Around six years ago, literally thousands of Google employees and contractors staged a brief walk-out to protest the company's handling of sexual harassment claims and other workplace issues, and to push for changes in pay structures.

Just a year ago, in what now feels like eminently simpler times, tech workers formed human roadblocks in Tel Aviv in protest of what they called unjust changes to Israel's judicial system.

The so-called Facebook Papers, leaked in the wake of Covid in part to protest the social media giant's policies on sharing of anti-vaccine misinformation, led to collective activism by workers at all levels of the tech titan.

That reaction in particular prompted Catherine Bracy, founder and chief executive of TechEquity Collaborative, to observe, "We are experiencing a major shift in work norms. Executives and upper management often come from a tradition that expects workers to check their personal lives and opinions at the door. Rank-and-file workers, especially millennials and Gen Z-ers, aren't willing to make those kinds of compromises."

None of this is lost on McGuckin. In the context of DEI, she responded, the part the McGuckin Group likes to focus on is "inclusion." "The reason we like to focus there," McGuckin told me, "is because we think that's directly correlated to leadership and the next connection point is, as a leader, how do you create an environment where everybody feels included? How do you create an environment where everybody feels like they can contribute?

"We think that the No. 1 way to do that is empathy. Empathy is walking in the shoes of others. How as leaders do we do that? It is not easy, but one of the ways is to create platforms for storytelling, to create platforms that allow leaders to tell their stories."

McGuckin uses a process she calls "sharing your story in six images." In contrast to one's professional résumé on their LinkedIn page, these are stories that shaped one's life. In her experience, when colleagues connect on a personal level, through stories, they can summit barriers that others can break through.

Not everyone has a made-for-TV life story to share, of course, but that doesn't mean they don't have a meaningful one. McGuckin's rule seems ever-so-simple on its face, but implementation is always the hardest part. Google has 180,000 workers. It can afford to take a hard line. That might not work for everyone, though. What's your company's plan?

Respects to a friend. I've spent my entire career in this industry, and the best part of it has been the many friendships developed along the way. When you are surrounded by friends every day, how can you not have fun? The saddest part is saying goodbye, especially too early. I will truly miss Regina Lathrop, my favorite San Francisco Giants fan (sorry Rob), who sweetness and humor lit up every conversation we had over the years.

mike@pcea.net
@mikebuetow

P.S. See you in June at PCB East and the UHDI Forum in the Boston suburbs! More than 65 leading companies will exhibit on June 5, and the tech conference features more than 75 hours of original content.

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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JEDEC Updates DDR5 SDRAM Standard

ARLINGTON, VA – JEDEC in April published the JESD79-5C DDR5 SDRAM standard, which includes features designed to improve reliability and security and enhance performance in applications from high-performance servers to emerging technologies such as AI and machine learning.

JESD79-5C introduces a method to improve DRAM data integrity called Per-Row Activation Counting (PRAC). PRAC precisely counts DRAM activations on a wordline granularity. When PRAC-enabled DRAM detects an excessive number of activations, it alerts the system to pause traffic and to designate time for mitigative measures. These interrelated actions underpin PRAC's ability to provide a fundamentally accurate and predictable approach for addressing data integrity challenges through close coordination between the DRAM and system.

JESD79-5C DDR5 also:

- Expands timing parameters definition from 6800Mbps to 8800Mbps
- Includes DRAM core timings and Tx/Rx AC timings extended up to 8800Mbps, compared to the previous version which supported only up to 6400 timing parameters and partial pieces up to 7200 DRAM core timings
- Introduces self-refresh exit clock sync for I/O training optimization
- Incorporates DDP (dual-die package) timings
- Deprecates PASR (partial array self-refresh) to address security concerns.

"I'm delighted to highlight the collaborative efforts of JEDEC's JC-42 Committee for Solid State Memory to advance the DDR5 standard," said Mian Quddus, chairman of JEDEC's board of directors. "Groundbreaking new features in JESD79-5C are intended to support ever-evolving industry demands for security, reliability and performance in a wide range of applications."

"The JC-42 Committee is pleased to unveil PRAC, a comprehensive solution to help ensure DRAM data integrity, as an integral component of the DDR5 update. Work is underway to incorporate this feature into other DRAM product families within JEDEC," said Christopher Cox, JC-42 committee chair.

TTM Opens PCB Fabrication Plant in Penang

PENANG – TTM Technologies officially opened a $200 million, state-of-the-art printed circuit board manufacturing plant here, its first in Penang. TTM anticipates that the new plant will generate annual revenue of about $180 million (approximately RM855 million) by 2025.

Built on 27 acres in Penang Science Park, the printed circuit board fabricator's state-of-the-art automated facility is customized to support mass production for various commercial end-markets, including networking, data center computing, medical, industrial, and instrumentation.

The new facility is configured to minimize energy and water consumption and will reduce the carbon footprint by 60% compared to a traditional PCB plant while still meeting rigorous environmental operational standards.

TTM expects to employ up to 1,000 workers at the site over time. A Phase 2 expansion could increase estimated revenues by 25%.

In a statement, TTM called the plant the result of "close collaboration" with its customers to address demand for geographical manufacturing diversity and PCB supply chain resilience.

"The opening of our flagship plant in Penang marks a significant milestone for TTM," said Thomas Edman, president and chief executive, TTM. "We are thrilled to embark on this expansion plan, with a state-of-the-art facility that underscores our commitment to providing our customers with differentiated advanced technology PCB solutions on a global scale. Today, we are proud to celebrate the grand opening of TTM's first large-scale, highly advanced technology-equipped facility in Southeast Asia.

"Penang's robust industrial ecosystem, position as the electrical and electronics hub, strong talent pool, and conducive business environment have made Penang a preferred location for TTM. Due to the outstanding support of the government and the efforts of our employees, TTM is now entering our production ramp only two years after our initial ground-breaking. As TTM builds our presence in Penang, we eagerly anticipate a longstanding relationship and mutually rewarding partnership with the Malaysian government, our customers, and our critical vendors," said Edman.

The inauguration of TTM's Penang plant was marked by the official opening ceremony, presided over by YAB Tuan Chow Kon Yeow, chief minister of Penang, accompanied by various administration and company officials.

"Penang is indeed proud to be the chosen location for TTM to establish its first large-scale, highly automated, and innovative PCB manufacturing plant in Southeast Asia, which also signifies the confidence that foreign investors have placed in Penang," said Chow. "Often lauded for its well-developed industrial ecosystem, Penang has the capacities and capabilities to support the needs of industrial players in next-generation technologies and growth strategies. I am optimistic that TTM will reap a myriad of benefits from its operation in Penang, the Silicon Valley of the East."

Arlon EMD Announces CA Expansion

RANCHO CUCAMONGA, CA – Arlon EMD has announced an expansion of its factory here, which will include the addition of two prepreg treaters and a press line.

The expansion will permit a larger portfolio of products to be manufactured in North America, improving responsiveness to the regional market and mitigating risk and capacity surges, the company said.

Arlon EMD, which was acquired by Elite Materials Company in 2020, has provided high-performance thermoset substrates for mission-critical printed circuit boards manufactured for high endurance and long-life programs for 45 years.

EMC is the world's largest manufacturer of halogen-free and HDI copper-clad laminates, with plants in Taiwan and China, and a factory currently being built in Penang, with a planned completion date in late 2024.

Thales Expands PCB Production Capabilities in Germany

ARNSTADT, GERMANY – Thales Group has expanded its circuit board production capabilities at its Industrial Competence Center here, citing an increased demand among Germany and Europe's rail systems.

The company said circuit boards are critical components for the railway industry to make the rail infrastructure in Germany and Europe fit for the future, and global supply bottlenecks can threaten that goal.

To prevent supply issues, Thales said it has made its circuit board production more efficient.

"This means we can increase our production speed and have significantly more planning and delivery security," the company said. "Our customers such as Deutsche Bahn and all rail travelers benefit from this through better planning of upcoming modernization projects."

Orbic to Reshore PC Manufacturing in NY

HAUPPAUGE, NY – Orbic Electronics has purchased a 27,000 sq. ft. building and three acres of land here for $6.6 million as part of its plan to move manufacturing from China to the US.

Orbic, which manufactures phones, laptops and other electronic devices, announced its Project Patriot plan in January, which will see it bring as many 1,000 jobs to Long Island in the next five years. The company previously received an incentive from the Suffolk County Industrial Development Agency to lease and renovate a 70,000 sq. ft. building in Hauppauge as part of a $30.8 million investment.

"This initiative is a stride forward in our vision of a sustainable, job-creating future," said Mike Narula, president and CEO, Orbic. "Project Patriot is set to be a very exciting time in our company's history, and Suffolk County is the perfect location for the bulk of our work to advance the production of American-Made products and grow American manufacturing jobs. Having our products read 'Made in America' is a tremendous point of pride for us, and it will also allow our company to bolster the local economy, helping other vendors in Suffolk County succeed alongside us."

IPC Releases 'J' Revisions to 2 Electronic

Assembly Standards

BANNOCKBURN, IL – IPC has announced the release of "J" revisions for two standards often used together for the manufacture of electronic assemblies.

IPC J-STD-001J, *Requirements for Soldered Electrical and Electronic Assemblies,* is the industry-consensus standard for soldering processes and materials and IPC-A-610J, *Acceptability of Electronic Assemblies,* is a post-assembly acceptance visual standard.

Revisions to these standards are completed every three years, with significant changes made to each one. Committee leaders addressed more than 1,350 comments for revision "J."

Some of the significant changes found in the standards are as follows:

- Global changes implemented in both documents:
    - Removed redundant minimum electrical clearance references – covered in Chapter 1 of documents
    - Clarified the use and definition of wire, lead and conductor
- Changes to IPC J-STD-001J:
    - Added hardware installation requirements
    - Added graphics to address bubbles in x-ray images
- Changes to IPC-A-610J:
    - Chapter 10 has new images
    - Conformal coating – clarified voiding/bubbles

In addition to the revisions for IPC J-STD-001J and IPC-A-610J, redline documents are available.

Ibase Breaks Ground on Vietnam Manufacturing Facility

VINH PHUC, VIETNAM – Ibase Technology has broken ground on a new manufacturing facility here, with plans to begin operations in early 2025.

The new factory will include six assembly lines for SMT and DIP, along with 10 system assembly lines, and will increase Ibase's monthly PCBA capacity by 60,000 and its monthly system assembly capacity by 30,000 for board and

system-level embedded and networking products, the company said.

"We have achieved a significant milestone in our company's endeavor to expand our manufacturing capabilities in Vietnam. This marks our first plant outside Taiwan and is an integral part of our long-term manufacturing roadmap aimed at providing our customers with the capacity they need for years to come and to meet their demands for greater flexibility, efficiency and quality," said C. S. Lin, chairman, Ibase Technology. "The AI revolution is underway, with the adoption of AIoT devices and the power of edge computing coming together to unlock the potential of edge AI. With over 20 years of experience in the IPC field, Ibase has the expertise to design and manufacture edge AI computing platforms essential for today's AI era. The new plant in Vietnam will be instrumental in the success of our edge AI initiatives."

Once completed, the Vietnam plant will provide 194,106 sq. ft. of manufacturing space, and when combined with the company's three manufacturing sites in Taiwan, its total manufacturing space will reach 491,997 sq. ft.

NCAB Group Acquires Belgian PCB Supplier

STOCKHOLM – NCAB Group has expanded into Belgium with the acquisition of PCB supplier Cumatrix BV.

Cumatrix's net sales amounted to SEK7 million ($652,000) in 2023 with an EBITA margin of about 7%. The company has two employees, and the majority of its sales are for the industrial sector with sourcing from manufacturing partners in China.

NCAB said the acquisition is expected to be earnings accretive in 2024, and synergies are expected in the areas of suppliers, payment terms and logistics.

"This acquisition is small but all the same it presents a strategic opportunity for NCAB Group to establish a local presence in the Belgian market," said Benjamin Klingenberg, VP, NCAB Europe. "With this action, we also gain highly skilled and experienced personnel from the PCB industry, who will complement our existing capabilities and play a pivotal role in unlocking new growth opportunities and expanding our network in Benelux."

"We are happy to be able to enhance our business in the NCAB context," said Cumatrix owner Gert Peeters. "This will mean a positive development for our customers, us personally and not the least give us new possibilities to grow in Belgium with the support of the entire NCAB Group."

Colorado EMS to Expand, Add 100 Jobs

COLORADO SPRINGS, CO – Spectrum Advanced Manufacturing Technologies has received $1.3 million in tax credits from the Colorado Economic Development Commission to expand its operations here and add up to 101 new jobs.

The planned expansion will include two new building at its existing campus, including a 12,500 sq. ft. manufacturing

center which will house ISO 8 Class cleanrooms for the production of AR/XR headsets and 3-D monitors, plus a 3,000 sq. ft. segregated cleanroom facility reserved for wiring and harnessing.

"This expansion signifies a strategic response to the growing demand for Spectrum AMT's expertise in high-reliability electronics manufacturing and assembly," said Jeff Gilbert, COO, Spectrum AMT. "We are deeply appreciative of our partnership with 5Star Bank and remain firmly committed to not only supporting critical industries like aerospace and defense but also contributing meaningfully to the advancement of technologies that shape the future, from space exploration and scientific discovery to addressing global medical challenges. We are proud to be part of a Colorado ecosystem that fosters innovation and economic growth, and we are excited to continue playing a vital role in Colorado Springs. This community has been instrumental in our beginning and continued success."

Zetwerk Plans Expansion of EMS Capacity

NEW DELHI – Zetwerk has announced a Rs1,000 crore ($119.6 million) investment to ramp up its electronics manufacturing capacity.

The company currently produces one device per second from its Noida factory in India's Uttar Pradesh, and plans to expand to 60 assembly lines from its current 16 lines across six manufacturing facilities. The expansion will enable Zetwerk to cater to major multinational corporations and OEMs in the computer devices segment through its Bangalore facility, the company said.

The company will manufacture motherboards, desktop PC power supplies and other electronic components, and said it aims to become a leading original design manufacturer and electronics manufacturing services provider.

"Zetwerk views India's electronics manufacturing sector as experiencing a transformative shift, akin to a Y2K moment, that will propel the nation toward a flourishing 'Viksit Bharat' (developed India)," said Josh Foulger, president of Zetwerk Electronics.

Fineline Acquires German PCB Maker

HAZOREA, ISRAEL – Fineline Global has announced the acquisition of German PCB supplier IBR Leiterplatten.

IBR will continue to operate independently and will now strengthen its position in the market, benefiting from additional production capacities, resources and infrastructure from the strong Fineline network, Fineline said in a release announcing the acquisition.

Existing projects and day-to-day operations will remain unchanged for IBR customers, the company said.

With the acquisition, Fineline said it will continue to expand its position as a leading value-added reseller of printed circuit boards in Germany and the DACH region.

"We are pleased to be able to offer IBR customers even more opportunities and benefits for stronger cooperation," said IBR managing director Christian Ringler.

"The Fineline team and I are very excited to see what IBR's recipe for success has been so far, and at the same time how we will continue to successfully develop both business models in the future," said Dirk Wolter, managing director, Fineline Germany.

KLA to Exit FPD Business

MILPITAS, CA – KLA announced in April that it is exiting the flat panel display (FPD) business by the end of the year, but will continue to provide services to the customer base for its discontinued products.

The company said the decision is based on multiple factors, including the cancellation of a new technology product by a major customer – reportedly Apple's recent scrapping of its microLED watch project – and it is investigating alternatives to the FPD business. FPD revenues accounted for 1.4% of the company's total revenue in 2023.

Apple's decision to cancel the microLED watch has affected other companies, as Ams-Osram also announced that it is considering its options after a canceled project and estimates its loss at $650 million to $900 million, while Kulicke & Soffa said it will also see losses of $110 million to $130 million after it had an Apple project canceled.

iNEMI Publishes First Wave of Online Roadmaps

MORRISVILLE, NC – The International Electronics Manufacturing Initiative (iNEMI) has published the first roadmap topics in its new format, with printed circuit boards, sustainable electronics, smart manufacturing and mmWave materials and test now available online.

"The in-depth content on these topics is intended to help companies align technology progress with their respective commercial interests and to support high-volume manufacturing," said Francis Mullany, iNEMI director of roadmapping. "The new format provides a more structured, accessible view of the roadmap that is easily updated based on market movements and technology innovations. And, of course, the roadmap continues to chart the future evolution of electronics manufacturing in terms of application drivers, technical needs, gaps, and technical solutions over a 10-year horizon to help guide R&D investment decisions by industry as well as public research programs and government agencies."

The initial wave of roadmap topics focuses on key technologies and cross-cutting topics critical to complex integrated systems (CIS), as discussed in a recent iNEMI/IPC whitepaper "Complex Integrated Systems: The Future of Electronics Manufacturing." The scope of each topic area now available is described below:

Printed circuit boards. Printed circuit boards (PCBs) are a fundamental element of a vast range of electronic

products. The PCB manufacturing ecosystem must continuously evolve and react to "technology blurring" with respect to substrates. The initial iNEMI Roadmap discussion of this topic covers a broad spectrum: high-speed PCBs and substrates; test, inspection and measurement; and environmental issues. Other topics currently under preparation include microwave and mmWave PCBs, laminate-based semiconductor packaging and PCB design.

Sustainable electronics. Sustainability in the design, manufacture, use and end-of-life handling of electronics systems is increasing as a consideration across the entire electronics manufacturing ecosystem. The iNEMI Roadmap currently focuses on the full scope of circularity and on key materials used. A new reporting format gathers information on sustainability hot-spot issues and roadmaps mitigating technologies on a per-substance basis.

Smart manufacturing. The term "smart manufacturing" encompasses the adoption of informed, intelligent, automated manufacturing processes at factory, enterprise, and ecosystem levels for increased flexibility, resiliency and efficiency. The initial release of roadmap content looks at the central topic of data flow architecture and at the issue of security of smart manufacturing systems and data.

mmWave materials and test. As part of the 5G/6G MAESTRO project, work on this topic was supported by the National Institute of Standards and Technology's (NIST's) Office of Advanced Manufacturing. It considers challenges posed by the operation of electronics at mmWave frequencies and higher. The focus is on the materials and their characterization and electrical test, primarily for PCBs and packaging substrates.

Publication schedule. In the coming months, the iNEMI Roadmap will:

- Provide qualitative market driver assessments and quantitative requirements for multiple application areas
- Map technology gaps and potential solution approaches for other critical technology topics such as board assembly, complex integrated systems, modeling and design
- Build a dynamic online presence for the iNEMI Roadmap, collaborating closely with other industry roadmaps.

See the current working view of the 2024 topic schedule.

New Kaga Factory to Receive METI Subsidy

SAN LUIS POTOSÍ, MEXICO – Kaga Electronics' factory construction project here will receive a 100 million yen ($660,000) boost from Japan's Ministry of Economy, Trade and Industry as part of its Indo-Pacific and Central-South America Regional Supply Chain Involvement Support Project.

The Indo-Pacific and Central-South America Regional Supply Chain Involvement Support Project is a subsidy scheme implemented by METI to encourage business initiatives that contribute to increasing the resilience of supply chains between Japan and the Indo-Pacific and Central-South America regions.

Kaga announced the Mexico factory in August, and through its subsidiary, Taxan Mexico, aims to strengthen and expand its production base to meet the increasing demand for EMS in Mexico. In addition to meeting an increase in orders from existing customers, the new factory is also designed to attract new customers through the assembly of

circuit boards used in air-conditioning equipment for the US market, the company said.

Kaga said it is also planning for a future expansion of its integrated production capability encompassing component molding, sheet metal processing and finished product assembly functions, in addition to current unit assembly and circuit board assembly.

By promoting local and localized production, beginning with the new factory in Mexico, the company said it will reduce transportation times and control logistics costs, as well as contribute to the construction of resilient supply chains for the stable provision of products to the market in collaboration with its customers and suppliers.

PCD&F

Alfa Laval launched a production line for printed circuit heat exchangers at its plant in Le Fontanil, France.

American Standard Circuits opened a 12,000 sq. ft. warehouse in West Chicago.

Calumet Electronics announced an expansion of its PCB manufacturing facility to more than 200,000 sq. ft.

Toppan will build a semiconductor packaging substrate factory in Singapore, with plans to put it into operation by the end of 2026.

CA

Ark Electronics announced the expansion of its EMS capabilities in Mexico and Europe.

Aven named **CE3S** distributor of its optical inspection and precision hand tools.

Betamek expanded its electronics manufacturing operations via the acquisition of **Sanshin (Malaysia)** from Tokyo-listed **Outsourcing Inc.** for MYR13.4 million ($2.8 million).

Bransys purchased a **Pillarhouse** Jade MKII selective soldering system.

Desay SV opened an 80,000 sq. m. expansion at its factory in Huinan, China, featuring 50 SMT production lines.

Dixon Technologies signed an agreement to use **Dassault Systèmes'** software, and is reportedly in talks to acquire a majority stake in **Transsion Holdings'** Indian unit.

Ducommun announced two awards totaling over $50 million in revenue for circuit assemblies for **Raytheon's** SPY-6 family of radar systems.

Ellies, a JSE-listed electronics manufacturer and distributor, is being liquidated after business rescue efforts failed.

Escatec has deployed **Pudu Robotics** material handling robots at its Malaysian plants in Penang and

Johor Bahru.

Foxconn in April started a rotating chief executive system in an overhaul of its management designed to nurture successors.

Instrumental announced it has joined **Nvidia Metropolis,** a partner program focused on bringing to market a new generation of vision AI applications.

International Finance Corporation is weighing a potential $150 million investment into **Salcomp's** India subsidiary.

ITW EAE named **Foster Innovative Technology** representative in Colorado, Idaho, Oregon, Montana, Utah, Washington and Wyoming.

Nordson Electronics Solutions expanded its partnership with **smartTec Nordic A/S** for distribution in Sweden, Finland and the Baltics.

Padget Electronics signed an agreement with Chinese ODM **Longcheer** to manufacture and sell smartphones for global brands using Longcheer's design and technology.

Phononic announced the launch of a wholly owned subsidiary in Thailand as its APAC headquarters.

Remtec completed a new, 55,000 sq. ft. facility in Canton, MA.

Signal Houshmand Kasra, an Iranian knowledge-based company, has set up a complete electronics assembly line near Tehran.

SMTXtra named **Kurt Whitlock Associates** representative in Florida and **MaRC Technologies** representative for the Pacific Northwest.

Sono-Tek named **SMarTsol Technologies** representative in Mexico.

VT Mechatronics completed an expansion of its factory in Győr, Hungary that doubled its assembly capacity.

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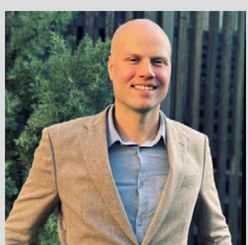
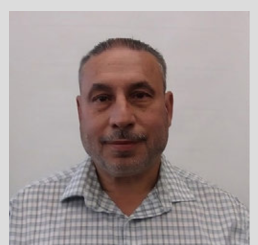
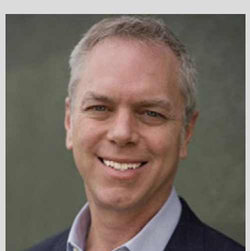


Daniel Sigtryggsson

Klaus Fiedler


Carl Colangelo


Kurt Palmer

Heraeus Electronics named **Ryan Banfield** product manager, Thick Film.

Kvikna Medical named **Daniel Sigtryggsson** senior hardware design engineer.

LPKF extended the contract of its CEO, **Klaus Fiedler,** until 2028.

Schmid Systems named **Carl Colangelo** manager of after sales engineering and sales support.

Schmoll America named **Kurt Palmer** president and CEO.

Amitron named **Lance Riley** head of sales and operations.

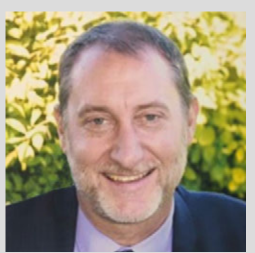
FreedomCAD promoted **Patrick White** to chief operating officer.

CA

David Prunier

Katherine Blake

Sergio Rodrigues

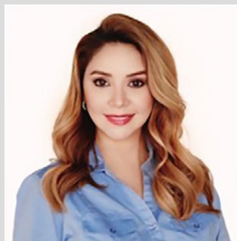

Ron Reed

Adam Osmancevic

Nino Hardin

Frank Hart

Jim Vaccaro


Angela Marquez

Accutronics named **David Prunier** COO.

AIM Solder appointed **Katherine Blake** business development manager – automotive and **Sergio Paulo Rodrigues** regional sales consultant in São Paulo, Brazil.

Avnet's **Ron Reed** and Arrow Electronics' **Adam Osmancevic** joined ECIA's Global Industry Practices Committee.

Cofactr welcomed **Nino Hardin** as director of sales.

Heller Industries named **Frank Hart** senior vice president, global sales and marketing.

South-Tek Systems appointed **Jim Vaccaro** industrial sales manager.

Zestron appointed **Angela Marquez** head of the business unit for Latin America.

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Reliable PCBs.
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'Early Bird' Discount for PCB East Technical Conference Ends May 3

PEACHTREE CITY, GA – The discounted price for the PCB East 2024 technical conference ends May 3, conference organizers said. From May 4 through June 4, registrants will pay the advanced conference price, which is $100 more than the "early bird" rate.

The technical program for PCB East 2024 features more than 75 hours of in-depth electronics engineering training from leading experts such as Rick Hartley, Dan Beeker, Tomas Chester, Zach Peterson and Susy Webb.

The conference will be held June 4 to 7 at the Boxboro Regency Hotel and Conference Center in Boxborough, MA. It features classes for every level of experience, from novice to expert.

The scope of classes ranges from basics on design engineering and circuit grounding, to DDR5 routing, impedance characterization, controlling noise and EMI, thermal management, board stackups and design for assembly.

More than half the presentations are new to PCB East, including ones on SMT equipment validation, medical wearable device compliance, flex design, AI in electronics, and signal integrity/power integrity. A special all-day session on UHDI design and manufacturing rounds out the technical conference.

"Registration for this year's technical conference is looking strong, and we look forward to an event that meets the needs of the entire electronics supply chain," said Mike Buetow, president, PCEA.

Registration for the technical conference and the exhibition is open at pcbeast.com.

An exhibition featuring more than 65 leading suppliers to the electronics design, manufacturing and assembly industry will be held June 5.

Boston Chapter to Present Talks on Supply Chain-Driven Circuit Design and Embedded Inductors

BOSTON – The PCEA Boston chapter plans a kickoff meeting on May 2. The speakers are Gopu Achath and Sanjay Keswani of EMA Design Automation on supply chain-driven circuit design and Paul Yang of Jove PCB on embedded

inductor technology.

Attendance is free, and you do not have to be a member to attend. Please RSVP to mike@pcea.net.

Meeting details. The meeting time is 10 a.m. to 12 p.m., at the University of Massachusetts – Lowell North Campus Alumni Hall room 102, 54 University Ave., Lowell, MA.

There is limited parking in the Cumnock Lot (31 University Ave.) near Alumni Hall. Additional parking is available in the North Parking Garage (293 Riverside St.). A map of the campus is here.

The speakers and topics are:

- Gopu Achath, vice president of technology, and Sanjay Keswani, lead, value engineering and services, EMA Design Automation: "Supply Chain-Driven Circuit Design." Traditionally ECAD users weren't integrated or involved in the supply chain. With the rising challenges in semiconductor industry around chip shortages, however, customers have realized the need for integrating ECAD with supply chains. Last-time buy and purchasing decisions have moved upstream to ECAD designers. Learn how to validate design components and select components for your designs based on part availability, lifecycle status, and – most importantly – lead time, all from within the design tool. We will demonstrate how to make supply chain resilience an essential part of the design process.
- Paul Yang, senior FAE manager, JOVE PCB: "Embedded Inductor Technology." With the rapid development of artificial intelligence and autonomous driving technology, miniaturization, integration, and modularization are the general trend of electronic product design, especially in chip power supply. Designers are looking for higher efficiency, higher power density, better reliability, and smaller package sizes. The inductors of tertiary power modules that power CPUs and GPUs usually occupy a large surface area, making it challenging to deploy more chips and small-sized resistor and capacitors. Thanks to the development of copper-iron cofiring integrated inductor technology, inductors can be embedded into the PCB and copper plating makes connections and fanout.

PCEA CURRENT EVENTS | CHAPTER NEWS

San Diego. Feedback for our April meeting during the Del Mar Electronics Show was awesome. Thanks to our speakers, Tom Hausherr of PCB Libraries and Stephen Chavez of Siemens. It was a great turnout, with about 70 attendees for our sessions, and great fuel to keep our chapter going! We have many new members who want to sign up for PCEA. We're planning another event in July to keep the momentum going.

Tom Hausherr (left) of PCB Libraries, with PCEA Chairman Stephen Chavez, at the San Diego Chapter meeting during the Del Mar Electronics Show in April.

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MARKET **WATCH**

Flex, IC Substrates Demand Give Cheer to Japan PCB Market

TOKYO – Printed circuit board production in Japan in February fell 9.3% from a year ago, falling to 757,000 sq. m. It was the 25th straight month of decline.

Sales fell 11.4% to 44.3 billion yen ($286 million), down the 16th month in a row. The year-over-year drop has reached double digits in 12 straight months.

The data include production of rigid and multilayer boards, flexible circuits and IC substrates, and are tabulated by the Japan Electronics Packaging Circuits Association (JPCA).

Rigid PCB production fell 13.9% from a year ago to 594,000 sq. m., the 24th consecutive month of decline, and revenue dropped 3.9% to 28.6 billion yen ($182.6 million), down for the 18th straight month.

Flex circuit production, a bright spot, rose 9.1% to 118,000 sq. m., reversing nine months of declines. Sales were up for the second straight month, rising 8.8% to 2.62 billion yen ($16.7 million).

IC substrate fabrication jumped 23% to 45,000 sq. m., the fifth consecutive rise. Sales were down for the 11th straight month, dropping 26.6% to 13.1 billion yen ($83.6 million).

Through February, PCB production in Japan was down 13% to 1.4 million sq. m., and sales were off 15.4%, at 83.7 billion yen ($534.4 million).

Rigid board production was down 17%, offset in part by a 4.2% increase in flexible demand and an 18% jump in IC substrates.

Computing Comeback

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	DEC.	JAN.[r]	FEB.[p]	YTD
Computers and electronics products	-0.4	0.3	0.2	2.3
Computers	-0.6	4.5	2.4	26.0
Storage devices	-3.7	9.4	1.6	21.1
Other peripheral equipment	0.8	7.1	2.1	9.5
Nondefense communications equipment	-0.5	0.1	0.6	-0.3
Defense communications equipment	-2.0	1.0	-2.5	-5.1
A/V equipment	-3.2	12.8	-4.6	26.3
Components[1]	1.8	0.6	0.8	9.8
Nondefense search and navigation equipment	0.0	0.4	-2.4	2.5
Defense search and navigation equipment	-1.5	1.0	0.6	8.9
Electromedical, measurement and control	0.0	-2.0	-0.9	0.4

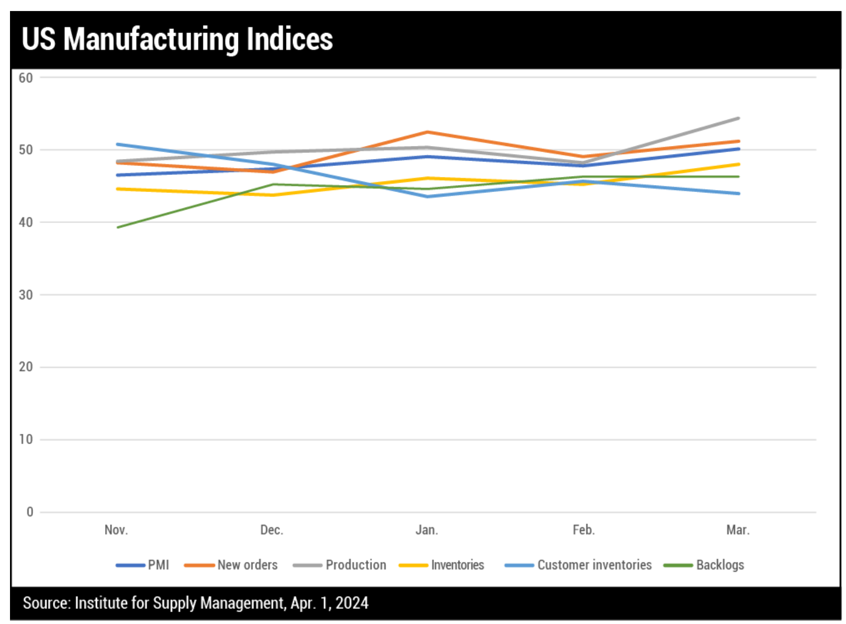
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Apr. 2, 2024

Key Components

	NOV	DEC	JAN	FEB	MAR
EMS book-to-bill[1,3]	1.18	1.16	1.15	1.22	TBA
Semiconductors[2,3]	5.3%	11.6%	15.2%	16.3%	TBA
PCB book-to-bill[1,3]	0.97	0.90	0.93	1.07	TBA
Component sales sentiment[4]	82.8%	77.8%	98.0%	100.8%	106.9%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA

US Manufacturing Indices



Source: Institute for Supply Management, Apr. 1, 2024

Hot Takes

PCB and MCM design software sales rose to $410.8 million in the fourth quarter, a 21% year-over-year increase. The four-quarter moving average, which compares the most recent four quarters to the prior four, rose 18.9%.

(ESD Alliance)

Revenues among the **top 50 EMS companies** declined 5.7% year-over-year in 2023, primarily due to drops at Foxconn and Pegatron. (MMI)

Taiwan's PCB industry should see revenues grow 6.3% this year, driven by robust demand for advanced PCBs used in AI applications and electric vehicles. (Taiwan Printed Circuit Association)

India's electronics manufacturing industry is projected to grow 41% annually until fiscal 2026, reaching Rs 5,980 billion ($71.7 billion). (Equiris Securities)

Global **smartphone shipments** increased 7.8% year-over-year to 289.4 million units in the first quarter. (IDC)

The worldwide **copper foil** market is expected to rise to $14.85 billion by 2033 from $7.41 billion in 2023. (Spherical Insights & Consulting)

Worldwide sales of **semiconductor manufacturing equipment** edged down 1.3% to $106.3 billion in 2023 from a record $107.6 billion in 2022. (SEMI)

Global **semiconductor sales** totaled $46.2 billion in February, a year-over-year increase of 16.3%. (Semiconductor Industry Association)

After two years of decline, the worldwide **traditional PC market** returned to growth during the first quarter with 59.8 million shipments, growing 1.5% year-over-year. (IDC)

Sentiment among electronics manufacturers remains positive, with demand reaching the highest level in a year. Firms that rely on borrowed capital indicated they are seeing an impact on material costs, inventories and orders as a result of higher interest rates, which then filters down to reduced capex spend and ability to grow and invest in other areas of the business. The new orders index rose to the highest level since July 2022. (IPC)

Global **300mm fab equipment spending** for front-end facilities is forecast to reach a record $137 billion in 2027 after topping $100 billion for the first time by 2025. (SEMI)

Production of **electronic components,** mainly semiconductors and displays, jumped 11.1% annually last quarter, thanks to strong demand for chips used in AI and HPC devices. Production of computers and optical components increased 17.7% from a year ago, bolstered by higher demand for AI and cloud-based data centers. (Taiwan Ministry of Economic Affairs)

US companies borrowed 7% less to **finance equipment investments** in March compared to a year ago. (Equipment Leasing and Finance Association)

Hiring in **India's electronics industry** increased 154% year-over-year in March, with telecom topping the hiring demand. (Quess)

The **AR microdisplay market** will grow at a faster pace than VR over the next five years, with AR seen as the ultimate consumer market and VR serving as a pathway for credibility and app development. (Yole)

Vietnam's electronics exports in the first quarter rose 35.7% to $16.33 billion. (Vietnam Customs Department)

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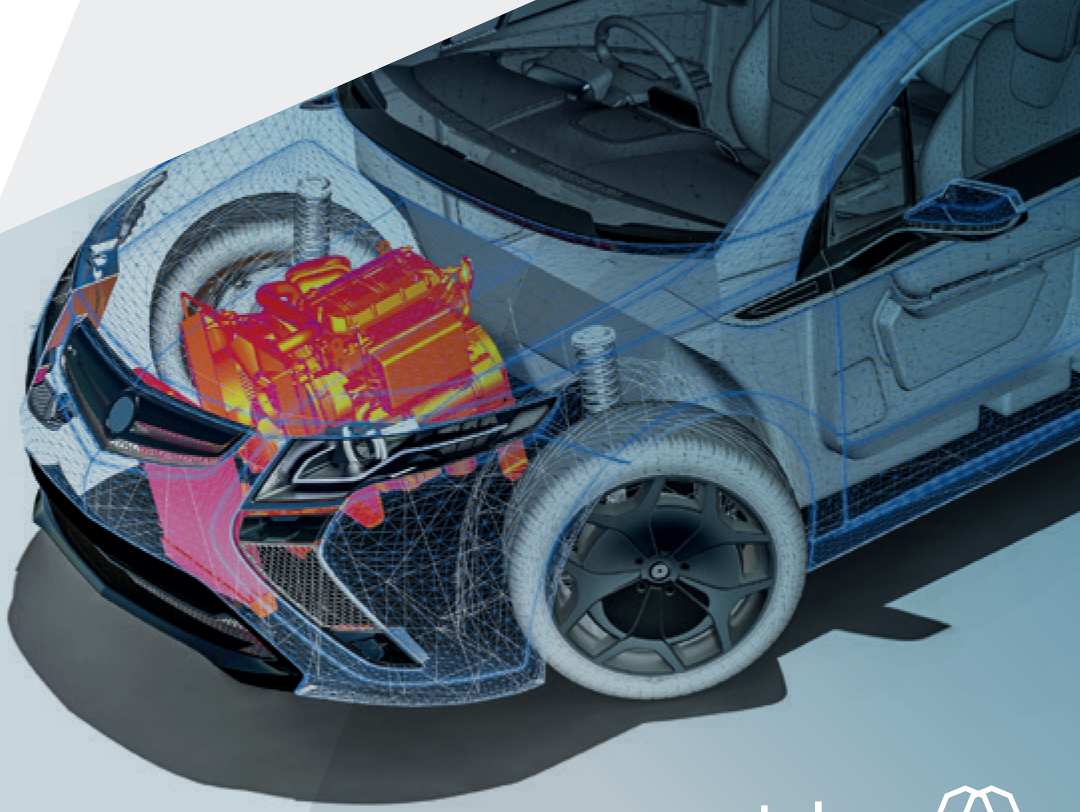

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Thinking, Big and Small

UHDI may be the next step, but what are the true limits of miniaturization?

HOW BIG IS big? How small is small?

Some things sound simple but in reality are very hard, if not impossible, to fathom. Consider space. In its most simplistic form, space is simply "up there." Look to the sky and that is space. Of course, scientists will then expand upon that to incorporate other planets, and again expand to include the solar system that encompasses those planets that circle the sun.

Within the past 100 years, humans have traversed and viewed increasingly farther into space thanks to ever-improving technology. This exploration has identified and in some cases, made contact with, phenomena such as asteroids, comets and black holes, to name just a few. Mind-boggling as these phenomena may seem, however, it is nothing compared to the infinite vastness of space! Voyager, a spacecraft launched to explore and transmit photos to Earth from deep space, has traveled over 14.8 billion miles and has only scratched the surface of the enormity of space.

Space is so big, one cannot fully comprehend its vastness.

The technologies that have been developed and harnessed to successfully explore, document and communicate back to Earth, on the other hand, are a testimony to the importance of manufacturing small devices. From the beginning of the development and deployment of the original electromechanical devices utilized to explore space, shrinking the size of devices has been the catalyst to advancing the technology.

From electromechanical to electronics, from "cards" to "chips," advances in miniaturization are the hallmark of industry, none more than our own printed circuit board industry. From discrete wire-to-wire interconnections to large circuits, spacing and thickness, the desire to get more functionality into smaller envelopes has evolved to today's fine lines and microvia technology. The number of circuits per square inch has exponentially increased while the actual size of the circuit board has correspondingly grown smaller.

If something such as space can be so big that its size is no longer fathomable, can the converse be true? Can something become so small that it also is no longer fathomable?

True to Moore's law, I must believe it unthinkable to an engineer in the early days of our industry that a circuit board or chip could possibly evolve to be as small and powerful as they are today.

Just as with space exploration, however, where the imagination may not be able to fully fathom its size, imagination can embrace the challenge of seeing how far it could go. The next wave of small is just ahead of us in ultra high-density interconnects (UHDI). This technology, still in its infancy, promises to increase circuit capacity, capability and density at least twofold. This means what is now considered small will become that much tinier in the relatively near future. As with any technology in its infancy, the relative size will become more extreme as advancements in design and manufacturing take full advantage of what can be accomplished and further shrink the package.

Which begs the question, how small can electronics technologies, and specifically printed circuit boards or interconnects, go? We don't yet know the true limit. Creative minds have imagined designs that could only be efficient if more could be done in less space. Equally determined minds have found ways to either refine manufacturing processes or develop new processes and equipment to effectively produce more capability in smaller envelopes. Looking forward, it is easy to see that advances will be made to make circuit boards significantly smaller with the capacity and capability to do more on less real estate. Going significantly smaller appears doable and is still very intellectually and emotionally digestible.

So how small does an electronic circuit need to be before its sheer size is unfathomable? A size that, as much as you look and explore, its existence is not recognizable. We already have chip packages that can barely be seen with the naked eye. Where this ends, we are a long, long way from knowing. The paradox is that when "small" is so small that it cannot be viewed by humans, like in the exploration of space, a device is invented to bring it into focus.

As with the cosmos, no matter how big and unfathomable it can appear, creative minds will continue to explore and seek answers. Ditto, inspired engineers will continue to get more functionality from ever-smaller footprints of technology. The mantra of "what if" will propel the next idea that in turn inspires the "can do" mentality to accomplish the unthinkable. How big is big? How small is small? The answer is the same: Whatever your mind can imagine!

PETER BIGELOW is president of FTG Circuits Haverhill; (imipcb.com); pbigelow@imipcb.com. His column appears monthly. He is vice chair of the UHDI & Substrates: Design to Package Forum, to be held June 5, 2024, in conjunction with PCB East in the Boston suburbs.

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WHAT ARE YOU doing differently this year?

Is your topline growing? Is your slow-moving inventory number shrinking? Are you attracting new clients while defending good existing ones? Is your cash position improving? Or are you stuck in an EMS/OEM mud pit?

Will 2024 be business as usual? Where will you get your inspiration to improve your business, from the inside team you've assembled or from an outside third party?

Sometimes inspiration comes from the most unexpected sources. I lack an engineering degree, but am part of a patent. Years ago, I solved a design issue as our time to prove a concept entered the final hours of our quest. The inspiration came from simply looking at my wife's tiny rock jewelry box and how the lid interfaced with the body of the box. Our engineers were blown away that the head of sales and marketing helped solve this difficult engineering design problem. (For what it's worth, so was I.)

Many companies I have spoken with want to grow organically but have no sales or marketing presence. How can a poor market awareness of your company and zero investment in those disciplines result in doubling your company? News flash: it can't.

You want to sell your company or buy an add-on business. How do you do that without a plan and experienced help? How do you assess your prospective buy without having done this before, especially if you represent a private equity firm with no real manufacturing services knowledge?

Can you improve the inventory/cash situation if you have numerous poor-paying customers that impose unreasonable demands on you just because they think they can. Do you wait too long to send a show cause letter out of fear it may send a "bad message" to your other clients? Do you fail to take legal action once that letter is ignored? It is my experience that poor-paying OEMs do this out of necessity (read: survival) or a crappy culture that hops from one manufacturer to another. It is rare you can "fix" these situations by buying them dinner, continued pleading, and resending undeniable proof of payments that are due.

Every turnaround I've been a part of started out by me following the cash. Make sure top leadership assumes responsibility for receiving undisputed payments. Don't just leave it to the A/R clerk and program manager. Make

calls and visits to the OEM leadership and set a mutually agreeable payment plan, or you can decide this won't change.

JAKE KULP is founder of JHK Technical Solutions, where he assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc. He can be reached at jkulp@cox.net.

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Century Circuits

Which PCB technologies are best suited to survive 100 years?

THE GOAL: BUILD an electronic device that will outlast everyone currently living on Earth. Looking back 100 years, few of us were here and the same will be said in the year 2124. Just reflecting on the brevity of life but we will take a century as forever.

One hundred years ago – 1924 – was the year that the Computer-Tabulating-Recording Company rebranded itself as IBM. Electric blenders, vacuum cleaners, traffic signals and television are among the inventions of the period. Two inventors of the era were leading us toward printed circuit boards though their patents were not commercially successful. Time would prove them to be quite insightful.

Figure 1. Created by Paul Eisler, the first printed wiring board used for a radio is about 80 years old. (Source: History-Computer.com)

Looking back to move forward. PCBs finally took hold around the middle of the century while integrated circuits followed another 25 years later. My "forever" board is going to make use of these early transistor-to-transistor logic (TTL) components that predated complementary metal-oxide-semiconductor (CMOS) technology. The physically larger transistor gates and the 5V logic are a concern. Both types were used on the Voyager space probes to build the

guidance and other systems. There was also a fully discrete version of the computer as a backup to the backup. I have confidence in those old Texas Instrument parts.

The dual-inline-package (DIP) comes in two flavors. One family's device designation starts with 74 and the other one starts with 54. The numbers indicate the type of package, with 74 being for plastic and 54 representing the same circuit in a ceramic package. Of course, the ceramic parts are what's exciting here. What we know of many lost cultures comes down to their pottery shards and burial sites.

The solid-state technology from the 1990s, while vintage, can still be found. The ceramic leadless chip carrier (CLCC) devices of the day would have a little more integration and could be accommodated on a robust through-hole printed circuit board. If we're not concerned about size, lead time or price, custom devices can be created from more modern chips. Instead of ultra high-density interconnect, we would have single-core processors in packages with a pitch of perhaps 1.27mm.

Finding things that are designed to last. High reliability doesn't have to mean antique technology. The stuff going on in the silicon photonics area includes hermetically sealed modules and devices. Enclosures with SMA connector feedthroughs and laser-welded seals are designed to keep working in almost any condition.

The automotive industry in particular specifies the most resilient connectors. It has made over a century's worth of improvements to the wiring of critical systems. The medical and aerospace industries have ruggedized devices that deserve a look as well. We want to keep our options open.

Metallization for the ages. The lesser-known Copper Age slots between the Stone Age and the Bronze Age. That makes the conductor of choice pretty easy. I'm going to want three to four ounces of copper per square foot on each layer. Yes, that will force wide air gaps on my four-layer board, which will guard against metal creepage. This mission requires flex circuit technology. The softer annealed copper they use for flexibility comes from working the metal under rollers. On a granular level, the structure of rolled annealed copper is smoother than electrodeposited copper typically found on stiff boards.

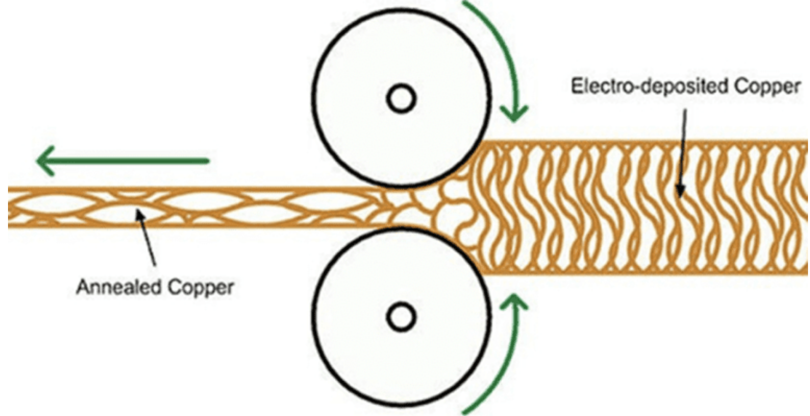

Figure 2. A diagram of how annealed copper is made. (Source: Sierra Circuits)

Since it's never going to be thrown into a landfill, we can get a RoHS exemption to use lead as a plating material. It will be a good old Sn63 eutectic solder. It's the best thing we have for soldering. Ask anyone in the aerospace business. The low-temperature solder process doesn't age the components like the lead-free options could.

Conformal coating or even encapsulating the whole thing in a resin would mitigate the coefficient of thermal expansion differences in the various materials that make up the printed circuit board. I'd like to see the potting material cure and end up like a brick of amber reminiscent of the kind archeologists find with mosquitoes that pestered the dinosaurs.

Exploring capacitor options for the long haul. Meanwhile, those pottery shards stood the test of time, thus the dielectric will go that way as well. Nice thick ceramic to go along with the metal content. It seems like the right material for the capacitors as well, but I worry about cracking. The MLC (multilayer ceramic) caps ought to survive. I'm not sure I even care about size at this point.

Electrolytic capacitors have a good reputation while tantalum caps are overcoming a not-so-good reputation for long-term reliability. Perhaps the mica "jellybean" caps have something to offer. In any case, derating them and distributing the capacitance as much as possible should help.

Resistors are tricky. On a long enough timeline, the expected tolerance increases. The most significant degradation is during bring-up and any other warming events. The immediate aftermath of getting a job is hard on a resistor but it settles in after a while. It could be hundreds of hours for some kinds of resistors though. Quarter-watt axial-leaded resistors with 1% purchased tolerance are going to have to do. We could look at printing some resistors on innerlayers.

Electronics have a habit of either dying young or dying very slowly. None of them is getting out of here without a burn-in to weed out the weakest of the lot. We're going to have to do some serious aging on these. In addition to thermal cycling, we have a salt fog chamber and a shaker table for when we want to do shock and vibe tests. Cycling from hot to cold is one of our best aging processes. Redundancy, derating and overprovisioning are our best fallback plans.

The bathtub curve for the failure rate is the instructive metric. The component engineers will have their hands full testing these things to their breaking points. Screening out early failures is the first pillar of the process. Next comes long-term test-to-failure of those survivors in torture chamber-like environments. All along, we're looking for root causes and designing experiments to single out the most resilient components. Once all the parts are vetted, the process scales up to the board assembly and, finally, the whole piece of equipment.

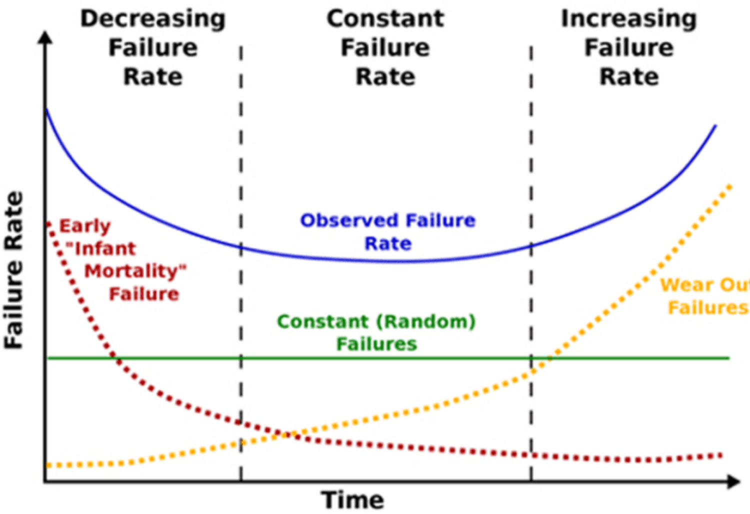

Figure 3. The blue line is a composite of the failure rates attributed to aging of a device. (Source: Wikipedia)

The easy answer to long-lasting products is that getting there must become cultural. An enterprise-wide mindset of continuous improvement is important. Tracking and eliminating defects while documenting both success and failure modes allows us to explore the leading edge while maintaining quality. It's a bad sign when a company shutters the reliability lab. Whatever advantage they may have had is going to fade away.

So, what is this forever-thing we are building? I don't really know. I'm only answering a question posed by a reader. Their name is somewhere in the avalanche of messages that fill my inbox every month. If I'm choosing, it would be something that detects and amplifies faint signals. Whether it is audio or something of a higher frequency, a good analog design stands the test of time.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

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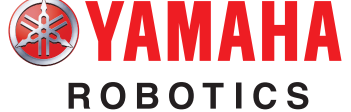

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Learning from the Past

What history can tell us about our position in high-tech.

NEW CHINESE RESTRICTIONS on the technology, including processors, permitted in equipment procured by government agencies are the latest move in the global battle for influence in the semiconductor industry; itself a part of a larger struggle for economic power.

US-based companies have more than 46% share of the $574 billion global semiconductor market (in 2022, according to a report by Citigroup), although China is the largest end-market, representing some 31% of sales. Semiconductor exports earn more for the US economy than any other products except oil, gas and aircraft. So of course, it's important.

We have all become heavily reliant on advanced semiconductors in every aspect of life and work, driving the machines we use to get things done: the IoT applications managing our homes, businesses and infrastructures; the AI powering interactions from photography and customer service to medical decision-making; even our mobility, which is increasingly electrified, automated and connected.

The Semiconductor Industry Association has noted a new upward cycle in the semiconductor market, beginning in late 2023, powered by trends such as AI and ongoing automotive electrification. It's natural that the world's largest economies want to guard their share of the action. China's move can be seen as a response to the Chips and Science Act, itself a response to global pressures threatening the US' relative strength. The European Chips Act has similar goals to its US counterpart and India also has ambitious plans to strengthen its indigenous high-tech sector. Although relatively few understand the technology, the power and influence associated with a strong semiconductor industry are clear for all to see.

I've said many times that making chips is part of an even bigger picture. That a strong high-tech sector needs more than the $40 billion in government funding allocated for building new semiconductor factories alone. All chip companies know the semiconductor business is risky. Building a new fab is a huge undertaking; a bet on the future, which can be derailed and devalued by unexpected technical developments.

There is history of investments that went awry as companies gambled on future chip geometries linked to specific technologies. When the tech changed, much of the investment became obsolete before the building was even completed. Intel's Fab 42 in Ocotillo, AZ, provides a lesson. Begun in 2011, demand for its 14nm technology had become uncertain by the time construction was completed and the plant lay unused. After receiving another few

billion dollars to re-equip the plant for 7nm manufacturing, the plant finally entered service in 2020 equipped to make 10nm chips. There are similar examples from across the world, including the UK, where plans to build a wafer fab in Dunfermline, Scotland, in the early 2000s ended after seismic changes in the mobile phone industry.

So, as the tech superpowers start to finance their ambitious plans, some caution is warranted. Government commitment to the health of high-tech industry is welcome and needed. On the other hand, the impressive spending pledges that express the commitment so emphatically must be directed wisely to avoid waste and, ultimately, strategic losses.

Advanced technologies such as AI and digital twins could provide some assistance here, by helping plan and build factories more quickly and cost-effectively, entering service within a shorter timeframe. I'm a great believer in the power of these technologies. although they alone cannot guarantee success.

We are seeking to solve problems brought about by the globalization trend pursued in previous decades, itself driven by commercial pressures. The pandemic and current geopolitical tensions have exposed the vulnerabilities in that model, particularly the difficulties in controlling long and fragile supply chains.

The Chips and Science Act recognizes the importance of supply chain to some extent by referencing the supply of chip-making equipment, as well as the ICs themselves. In China, too, the importance of factory equipment to chip manufacturing capacity is recognized. The US has sought to restrict China's access to advanced chip-making equipment. In response, China is looking to increase production and advance the technology of tools made and designed locally by companies such as Shanghai Micro Electronics Equipment (SMEE), China's most advanced lithography scanner manufacturer. Chinese chipmakers like SMIC have used European equipment to build 7nm smartphone processors, although threats to technology access for further process shrinks has driven collaborations with other local companies.

While countries around the world look to increase resilience in supply chains by prioritizing local production, it is intriguing to see that some geographical pinch points remain. Chip manufacture depends on a supply of high-purity quartz used to make the crucibles for growing high-quality silicon ingots. The highest purity quartz comes from just one place on earth: the Spruce Pine quartz mine in North Carolina. It's sobering to consider the potential for problems at this one facility to disrupt a global industry. There are sources of fully synthetic quartz, which could expand to replace the quartz from Spruce Pine, but this would take time to scale up and would also increase costs.

After the recent global pandemic, and its effects in so many aspects of our lives, we are all understandably motivated to Build Back Better. That spirit is at the core of our nature. We should be careful with our ambitions and our spending power, however. As we have become adept at doing with AI, we should use the experiences from previous good and bad examples to train our responses, to ensure that all in this world can have a secure future.

ALUN MORGAN is technology ambassador at Ventec International Group (ventec-group.com); alun.morgan@ventec-europe.com. His column run monthly.

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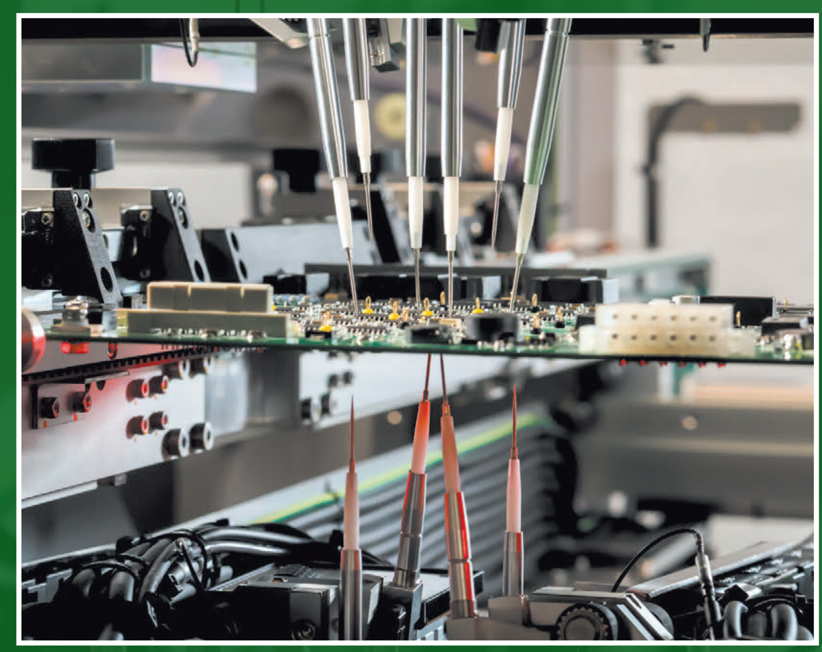

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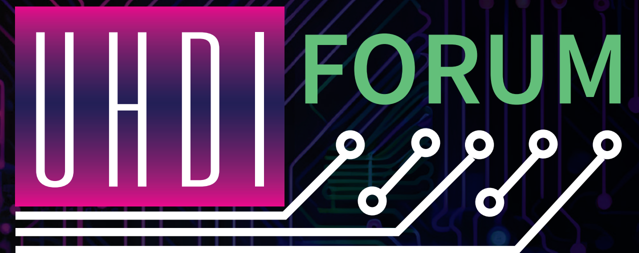

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EMC

How the PCB Stackup Helps Control EMI

Power and signal placed on outer layers minimize radiated emissions.

by AKBER ROY

The PCB stackup is like a building's foundation; a product not built on a strong base will fall apart. When electromagnetic compatibility (EMC) testing is considered, the PCB stackup is a major determinant of radiated EMI, and to some extent, conducted EMI. A PCB stackup design that enables low EMI also aids signal integrity and power integrity, as all these areas are linked and must be considered in totality.

So, to ensure a PCB design passes EMC testing, understand the stackup's role in generating emissions and determining EMI susceptibility. Simple changes in materials, layer assignments, and routing strategies can make the difference between passing and failing EMC tests. All these decisions originate in the PCB stackup.

Key Elements in PCB Stackup Design

For experienced designers, stackup design isn't terribly complex, even for designs that require high-speed routing or RF interconnects. From an EMC perspective, effectively managing EMI and reducing susceptibility hinges on a few key parameters:

- Strategic placement of ground within the PCB stackup
- Utilization of planes for power and ground
- Appropriate dielectric thickness between signals and ground
- Incorporation of copper pour within signal layers.

Carefully crafted PCB stackup can effectively mitigate common EMI issues that plague new designers. In addition, by solving these EMI challenges, one can simultaneously address specific signal integrity issues, particularly those related to routing and impedance control. Now let's dig into each of the above areas to see where EMC can be addressed.

Location of Planes in Multilayer PCBs

The placement of plane layers within multilayer boards significantly affects signal integrity and EMI. In high-speed designs, it also plays a major role in ensuring power integrity. In early two-layer designs, boards relied on conductively filled vias for grounding, which were then connected back to the primary power source. Today, even entry-level PCBs for most designs have at least four layers, primarily for EMI mitigation and improved signal

integrity.

A standard four-layer stackup is shown in **Figure 1**. This configuration provides two internal ground plane layers, ensuring effective shielding for all signals on the outer layers. This concept can be easily extended to six layers, eight layers, and beyond.

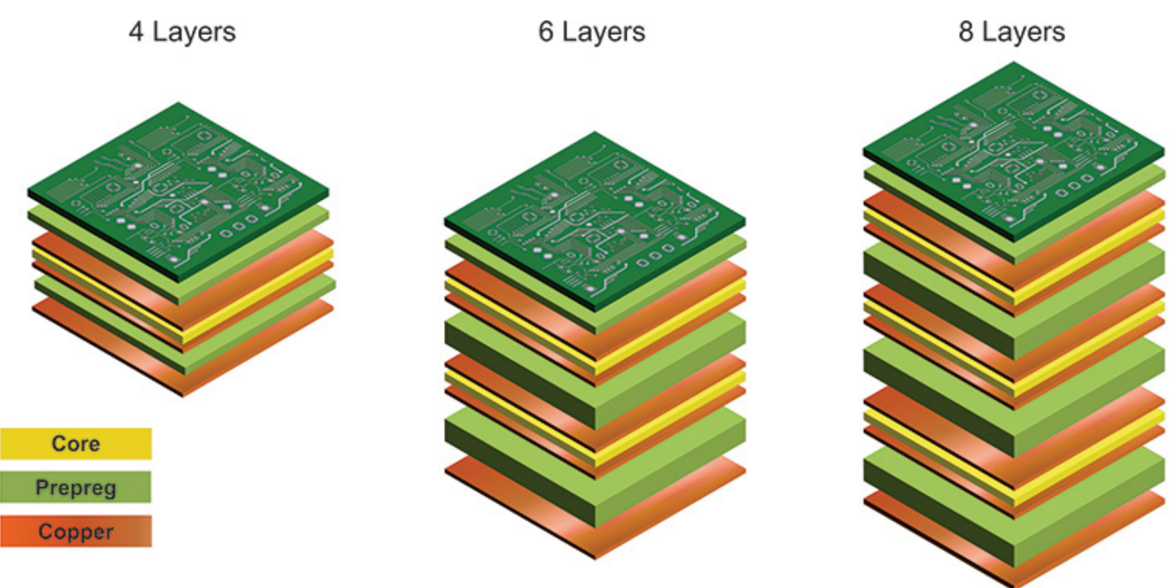

Figure 1. PCB stackups with four layers, six layers, and eight layers.

Placement of power and signal on the outer layers is preferred for minimizing radiated emissions. This configuration permits placement of an adjacent internal ground plane or image plane beneath any switching elements or signals on the top layer. This significantly reduces radiation from these elements.

Other advantages of placing a ground plane in close proximity to signals include reduced crosstalk and streamlined impedance control. With a ground plane situated in a layer adjacent to signals, the impedance of the trace and its mutual inductance/capacitance to nearby traces can be determined. This arrangement enables designers to effectively control all three factors, allowing them to easily mitigate EMI and crosstalk without sacrificing impedance control.

2-Layer PCBs and Ground Planes

What about two-layer PCBs? Can or should they have a ground plane?

In two-layer board designs for digital systems, establishing a ground plane is generally recommended. The use of two-layer boards for digital systems is acceptable under the following two broad conditions:

- When component placement and routing density is low
- When the system doesn't involve fast signals (those faster than 1ns).

The first condition is important since it dictates the feasibility of grounding by copper pour and stitching vias. As component density and the number of traces increase, there's limited space for copper pour on the top and bottom layers. Consequently, the ground becomes poorly defined near digital signals, potentially leading to increased radiation. It is also more difficult to maintain consistent impedance across the entire interconnect, especially differential impedance.

The result is a board that resembles the image in **Figure 2**, which readers may recognize as an Arduino with dense, high-speed routing near the USB connector and headers.

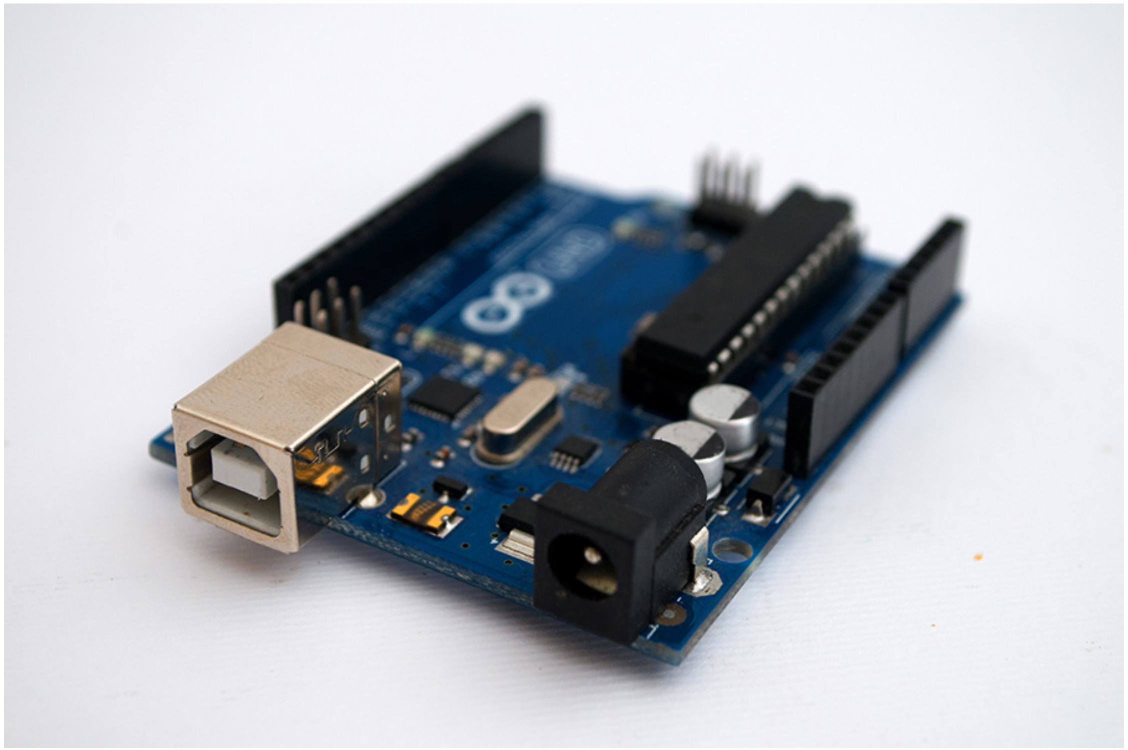

Figure 2. Arduino boards with dense, high-speed routing near the USB connector and headers typically pass EMC testing.

While Arduino boards typically pass EMC testing, it is important to note that design practices employed in Arduino boards do not universally apply to other digital systems.

The second condition is crucial since signal speed directly impacts the level of radiation emitted. Faster signals inherently emit more radiation, particularly at higher frequencies where the power spectrum concentrates more energy. This demands increased grounding to effectively suppress radiation. For this reason, it is common practice to use four-layer boards, at minimum, for PCBs designed to send and receive high-speed signals.

Layer Thickness

The thickness of the dielectric between signal and plane layers determines several parasitic effects, which are important determinants of EMI and signal integrity (SI):

- Trace self-inductance
- Trace self-capacitance
- Trace mutual-capacitance
- Spreading inductance for planes and pours.

The first two items in the list directly impact both EMI susceptibility and the level of radiated emissions expected from a PCB stackup. Furthermore, capacitance, whether self or mutual, plays a crucial role in capacitive coupling of noise originating from other conductors in the system, such as the enclosure. This coupling may lead to the undesirable occurrence of common-mode noise coupling/infiltrating an interconnect.

One fundamental parameter in PCB stackups that directly influences all the aforementioned parasitic effects is the thickness of the dielectric layer separating signal-carrying conductors and a ground plane. Similarly, the distance to a uniform power plane, acting as the reference for a trace, is vital. By bringing the reference layer closer to the signal layer – accomplished through use of a thinner dielectric – radiation and coupling, which lead to noise currents in copper traces, are reduced. This applies regardless of the circuit type (power, digital, RF, etc.).

What About Radiation from Rails and Planes?

For power integrity and radiated emissions, particularly where rails are concerned, the key consideration lies in the nature of these conductors. Large rails, such as those used for power distribution, essentially carry DC power overlaid with an AC signal (voltage ripple). In the case of digital systems, rails supply pulses of current to power-hungry processors. In both cases, the AC portion of the delivered power generates a changing magnetic field, which manifests as radiated emissions.

The spreading inductance of these large conductors dictates the amount of radiation. Essentially, what we call self-inductance for traces is equivalent to spreading inductance for a large polygon-shaped conductor. The main difference is that the spreading inductance is determined by the region in the conductor where current exists. Therefore, spreading inductance determines radiated emissions, while self-inductance in planes determines susceptibility.

The easiest way to reduce both factors in a PCB stackup is to bring the ground plane closer to the copper pour region used for power distribution. This approach reduces both spreading inductance and self-inductance, thereby confining the electromagnetic field within the stackup to reduce radiation. In terms of power integrity, this proximity increases plane capacitance, which proves beneficial for stable power delivery even at high frequencies up to gigahertz.

The Fabricator, The Stackup and You

Understanding the principles of PCB stackup design, especially with regard to EMI and EMC, is paramount for any product destined for commercial success. The most important aspect of designing a PCB stackup, however, lies in ensuring it can be built at scale. This entails consideration of material availability and processing feasibility, which must be balanced against the performance or engineering requirements of the PCB and the end-product.

So, how should a designer approach selection of a stackup to ensure minimal EMI and successful EMC testing? There isn't a singular stackup blueprint that guarantees a design will pass EMC testing – multiple designs can achieve the same goal. It's more important to understand the key parameters that can be adjusted in a stackup, rather than starting from scratch with every design iteration.

Your fabricator will inevitably have valuable input regarding the stackup, particularly regarding available materials and layer thicknesses in the stackup design. Therefore, involving the fabricator in the stackup design process is essential. Areas where a fabricator can help include:

- Determining if a standard stackup will meet project requirements
- If a custom stackup is needed, determining the optimal layer arrangement and availability of materials
- Selecting appropriate layer thicknesses from available material options
- Verifying and fine-tuning the custom stackup design, ensuring alignment with manufacturing capabilities and material availability.

Figure 3. Fabrication engineers can assist in meeting end-product requirements.

In many cases, a standard stackup with ground planes will be adequate to achieve low radiated EMI and, often, low conducted EMI. It is imperative to arrange and utilize the layers appropriately, however, lest the layer count and layer construction fall short in fully mitigating EMI issues.

AKBER ROY is chief executive of Rush PCB (rushpcb.com); roy@rushpcb.com.

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Performance Comparison of Contemporary Stencil Coatings and Underwipe Solvents on 0.4mm BGA Packages

Should chemistry formulation and drying time factor into solvent selection?

by CHRYS SHEA, DEBBIE CARBONI and JOHN HANERHOFF

The practice of periodically wiping excess solder paste off the side of the stencil that contacts the PCB during the printing process can take many different forms and frequencies. The objective of wiping is to remove unwanted solder paste from the contact side of the stencil.

How does solder paste find its way to the contact side of the stencil? By nature, solder paste sticks to both the PCB pad and the stencil. It does not fully release from the aperture upon separation, depending on the area ratio (AR) of the aperture. Very often, transfer efficiency (TE), or the amount of solder paste removed from the aperture, is less than 100%. The remaining paste often forms "strings" that snap back to the stencil's contact side **(Figure 1)**.

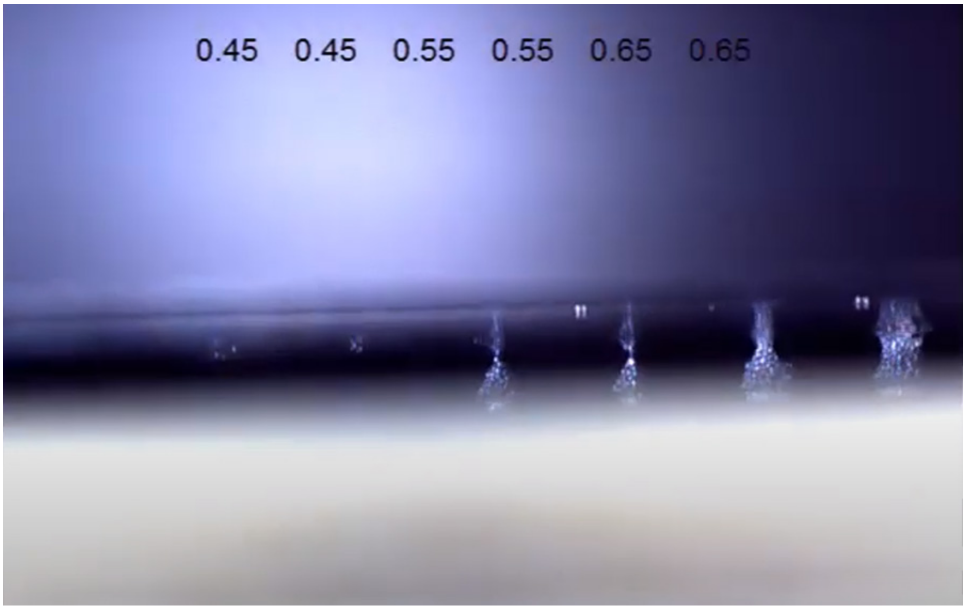

Figure 1. Solder paste release from stencil, side view.

How does errant paste on the contact side of the stencil affect print quality? The solder paste left on the bottom side of the stencil prevents it from gasketing against the PCB and is often the root cause of excessive solder deposits, solder bridges and solder balls. Therefore, it is important to remove the excess paste *before* it negatively affects the process.

The underwipe process itself has a number of variables, including printer hardware capabilities, wiper media type (paper or fabric), solvent type (if any) and number of prints per wipe cycle (prints per wipe, or PPW). These process parameters are typically adjusted based on systemic variables such as PCB layout, solder paste type, machine capability, board support, stencil coating and finest pitch components, as seen in the fishbone diagram of **Figure 2.**

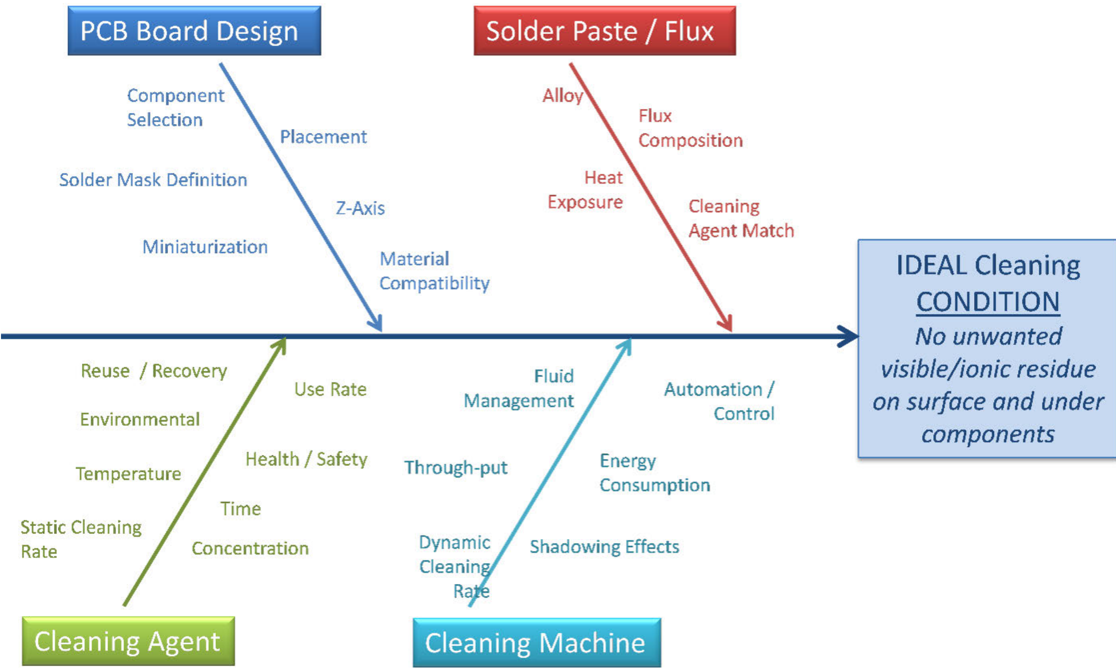

Figure 2. Factors that affect stencil cleanliness.

Previous Work

The role of underwiping on solder paste print quality was diligently studied in the mid-2010s. Research investigated the effects of print parameters, stencil types, stencil coatings, underwipe chemistries and wipe sequences.[1-5]

Findings included:

- Wet wipe was better than dry wipe.[1]
- IPA could seize up certain solder paste formulations in the stencil.[1]
- Release speed had a considerable influence (faster is better).[2]
- Solder paste “strings” upon release.[3]
- Coated stencils limit the stringing and improve release.[4]
- Ending with a vac pass is better than ending with a dry pass.[1]
- Wet wipes keep the process consistent and limit the “bounce” seen with dry wipes.[5]

Videos showing the effectiveness of wet-vac-vac over wet- vac-dry can be seen here.

Experiment

Procedure. Leveraging knowledge gained in the aforementioned studies, an experiment was designed to test components in numerous package sizes and different wipe frequencies. **Figure 3** illustrates the experimental design. The experiment was executed on production equipment that included:

- EKRA Serio 4000 printer
- Clean, new squeegee blades
- Solid board support plate
- Poly/cellulose wiper textile
- Two laser-cut stencils, one coated and one uncoated
- Two different underwipe chemistries
- Mycronic Pi solder paste inspection (SPI)
- Type 4 Tin-lead solder paste (popular, 20+ year old formulation).

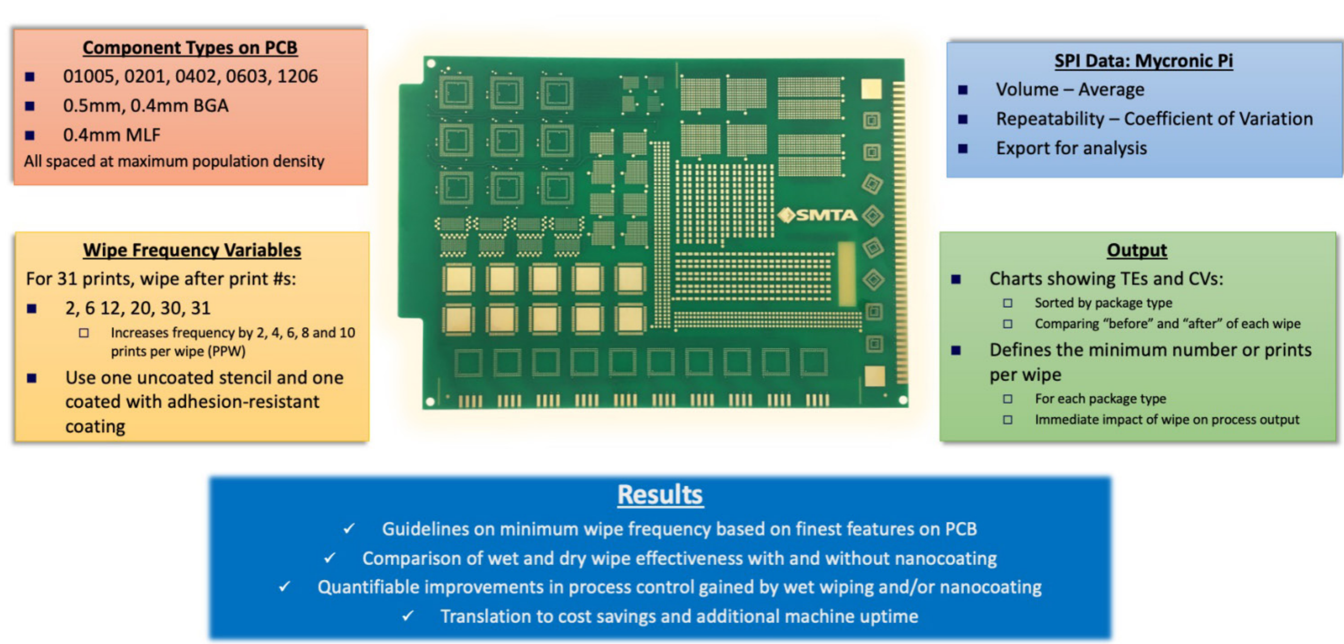

Figure 3. Underwipe experimental design overview.

After kneading four strokes to ensure the solder paste was in its working viscosity range, the stencil was cleaned with a wet-vac-vac (WVV) wipe sequence twice to ensure cleanliness at the start. Two boards were printed, for two PPW, then the stencil was cleaned with a single WVV. This was repeated at wipe intervals of 4, 6, 8 and 10 prints. Two replicates were run for each combination of stencils and chemistries.

The experiment was later repeated without cleaning chemistry. The setup was identical, but the wipe sequence was vac-vac-vac (VVV) without any chemistry.

The order of execution is detailed in Appendix A.

Test vehicle. The test vehicle used was the SMTA test board **(Figure 4)**. It contains footprints for many different sized SMT components. The component sizes of interest in this study are analyzed in the order of decreasing aperture sizes **(Table 1)**.

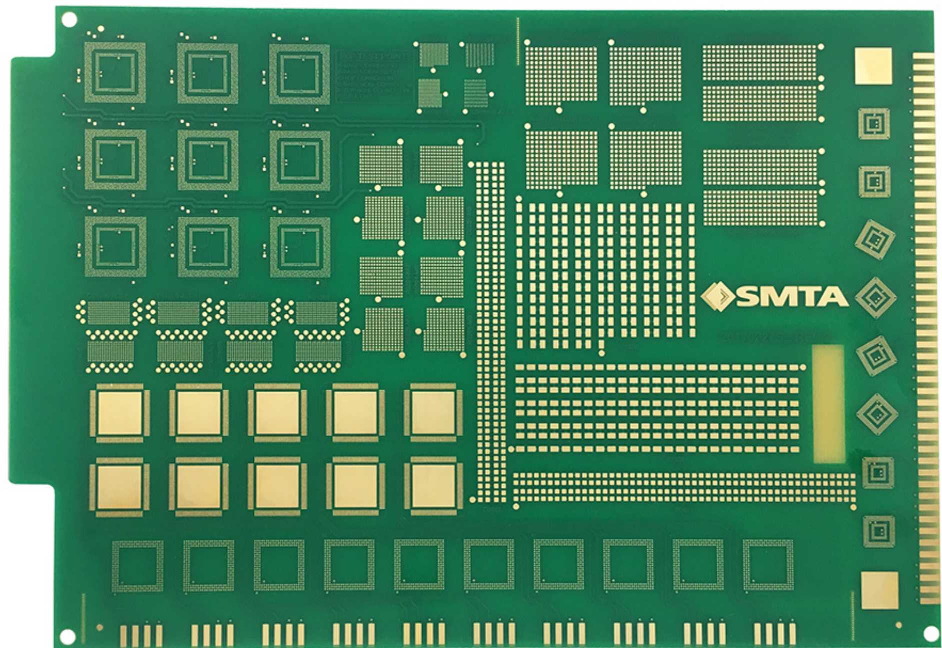

Figure 4. The SMTA miniaturization test vehicle.

Table 1. Device and Aperture Sizes Tested

Component Size		Type	Stencil Aperture Size		Area Ratio
Imperial	Metric		mil	µm	4 mil (100µm) Foil
0201	0603M	Chip	10.8 x 13.5	275 x 350	0.79
20 mil pitch	0.5mm pitch	BGA	10 x 10*	250 x 250*	0.63
01005	0402M	Chip	8 x 8	200 x 200	0.50
16 mil pitch	0.4mm pitch	BGA	7.5 x 7.5*	190 x 190*	0.47

*Indicates a square aperture with radiused corners

Data analysis. Transfer efficiencies (TEs) were exported and consolidated in Excel. Again, TEs express the amount of solder released from the stencil and deposited on the pad as a percentage of the theoretical aperture volume for each deposit.

TE statistics are calculated using pivot tables. The average TEs and coefficients of variation (CVs) are calculated for each component size. The CV is one standard deviation divided by the average. It relates the spread of the data to their mean and is widely used in characterizing stencil printing processes.

Ideally, the CV is less than 10% of the mean, indicated in the output charts by green data points. CVs of 10-15% are considered acceptable and indicated by yellow data points; CVs greater than 15% are considered unacceptable and indicated by red data points.

The rationale behind the CV guidelines is based on a normal distribution of data and typical SPI tolerances of 50-150% the TE goal, as illustrated in **Figure 5.**

Why a CV of ≤ 10%?

<10%: desired

- CVs of 10% or less will produce 99.7 % of deposits within +/- 30% of the average volume, leaving ***plenty of room*** for common (or even some special) causes of variation

10 - 15%: acceptable

- CVs of 10-15% will produce 99.7% of deposits within +/- 30 - 45% of the target volume, leaving ***little room*** for variation

Over 15%: unacceptable

- Almost ***no room*** for variation
- CVs of 16.7% or higher will produce deposits outside the control limits, indicating an out-of-control process.

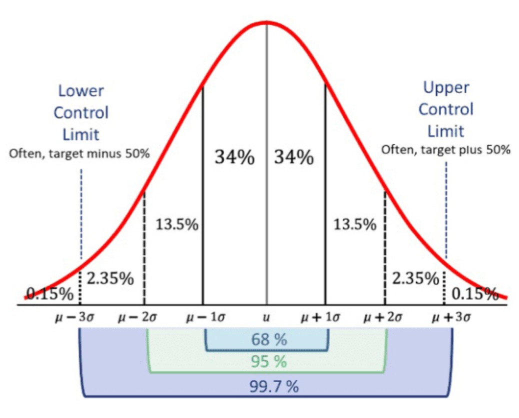

Figure 5. The normal distribution and coefficient of variation.

Analytical Methods and Results

Overall print quality. Print volumes were extremely consistent, indicating a very well-controlled print process.

- 0201 and 0.5mm BGA components all showed >100% transfer efficiency (TE), with nearly all CVs under 10% and only a few in the 10-15% range, on both coated and uncoated stencils **(Tables 2** and **3)**.
- 01005 components showed an obvious trend: The coated stencils produced CVs of at most 11%, whereas the uncoated stencils produced CVs of approximately 30-60% **(Table 4)**.

Table 2. TE and CV for 0201 Components

0201 AR = 0.79				
Chemistry	Uncoated Stencil		Coated Stencil	
A	TE	CV	TE	CV
2PPW	102	6%	114	10%
4PPW	102	7%	109	5%
6PPW	106	7%	109	6%
8PPW	106	6%	110	6%
10PPW	105	5%	109	6%
FinalPPW	106	7%	113	4%
B				
2PPW	105	6%	113	7%
4PPW	106	7%	110	5%
6PPW	107	9%	112	6%
8PPW	108	7%	112	5%
10PPW	108	7%	111	5%
FinalPPW	108	8%	111	5%

Table 3. TE and CV for 0.5mm Pitch BGA Components

05BGA AR = 0.63				
Chemistry	Uncoated Stencil		Coated Stencil	
A	TE	CV	TE	CV
2PPW	112	7%	122	13%
4PPW	110	12%	116	5%
6PPW	113	8%	117	5%
8PPW	112	7%	118	7%
10PPW	112	6%	117	6%
FinalPPW	116	8%	123	4%
B				
2PPW	112	5%	119	5%
4PPW	113	5%	120	5%
6PPW	116	7%	121	6%
8PPW	118	6%	120	4%
10PPW	116	6%	119	5%
FinalPPW	115	5%	120	3%

Table 4. TE and CV for 01005 Components

01005 AR = 0.50				
Chemistry	Uncoated Stencil		Coated Stencil	
A	TE	CV	TE	CV
2PPW	75	45%	108	11%
4PPW	70	59%	105	8%
6PPW	86	41%	105	8%
8PPW	87	28%	106	9%
10PPW	82	36%	103	11%
FinalPPW	70	57%	111	7%
B				
2PPW	81	43%	109	8%
4PPW	75	55%	107	6%
6PPW	80	54%	109	7%
8PPW	84	47%	108	8%
10PPW	82	54%	107	7%
FinalPPW	96	34%	109	5%

This finding illustrates the influence of coating stencils for miniaturized devices. At the AR of 0.63, the coating's impact was not apparent. Using wet wipes, the process was capable even without stencil coating. But at the 0.50 area ratio, it was far from capable without the coating, even with wet wipes and at short wipe intervals.

- The process window for the uncoated stencil closed somewhere between the 0.63 and 0.50 AR, but did not noticeably narrow for the coated stencil until the 0.47 AR **(Table 5)**.

Table 5. TE and CV for 0.4mm BGA Components

04BGA AR = 0.47				
Chemistry	Uncoated Stencil		Coated Stencil	
A	TE	CV	TE	CV
2PPW	70	57%	111	14%
4PPW	72	59%	107	9%
6PPW	94	31%	106	13%
8PPW	88	33%	106	14%
10PPW	83	43%	102	19%
FinalPPW	51	83%	112	12%
B				
2PPW	66	70%	111	12%
4PPW	71	63%	109	11%
6PPW	79	61%	111	9%
8PPW	79	59%	110	9%
10PPW	82	60%	109	10%
FinalPPW	96	39%	111	10%

As anticipated, the uncoated stencil performed more poorly on the 0.47 AR than the 0.50 AR, in both TE and CV. The coated stencil, however, showed >100% TE and the CVs were in the 9-19% range, indicating the edge of the process window, and making it the most informative data set to further explore.

Based on the normal curve model shown in Figure 5, the CVs on uncoated stencils indicate complete incapability and would add statistical noise to the analysis. Therefore, the effects of uncoated stencils are eliminated from the analysis.

It should again be noted that the edge of the print process window was identified at the 04BGA pitch (0.4mm). indicating a very well set up process. Many print processes reach the edge of their window at the 05BGA pitch (0.5mm).

The leading-edge effect. The PCB layout for the 04BGAs is shown in **Figure 6.**

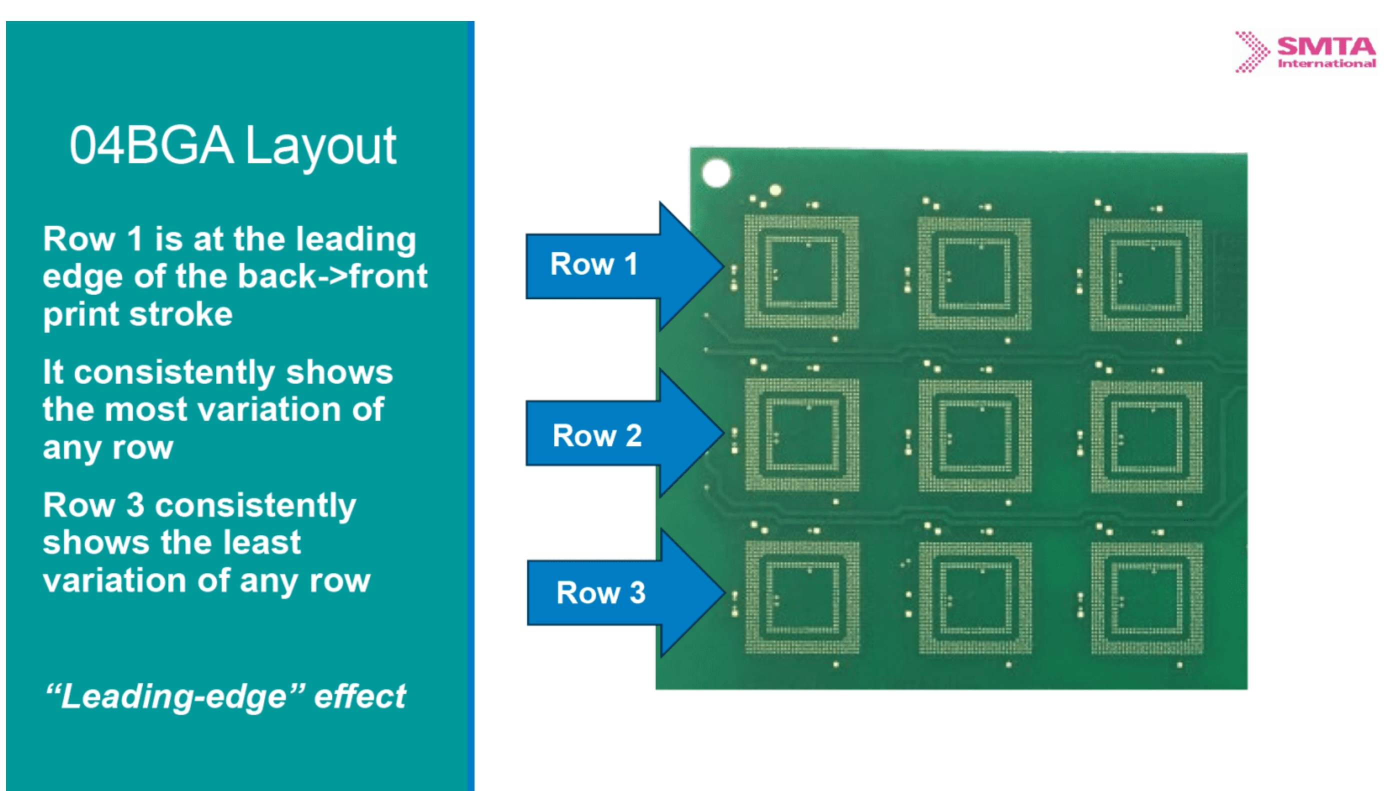

Figure 6. Close up of the layout of 0.4mm BGA on SMTA board.

Row 1 consistently shows the greatest amount of variation. In solder paste printing, this is often referred to as the "leading-edge effect." It is typically observed when the first few apertures in the direction of the squeegee stroke do not get complete fill, and it is more common as aperture size decreases.

Row 3 consistently shows the least amount of variation. It is located in the middle part of the print stroke, where the solder paste has reached its lowest printing viscosity.

Figures 7 and **8** show the differences in print quality among the three rows. TEs in Row 1 are slightly lower than Rows 2 or 3 which appear to be relatively equal. The CVs on Row 1, however, are considerably higher than those of Rows 2 or 3. In fact, the CVs on Row 1 are so high that the process is not considered capable (<15%). Rows 2 and 3

provide better indicators on the effectiveness of under wiping.

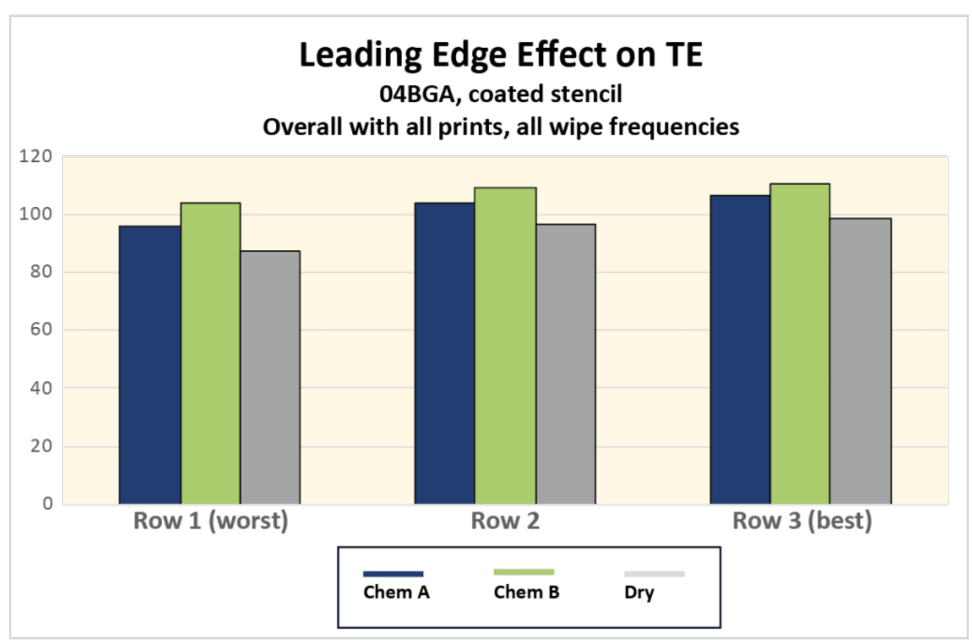

Figure 7. TE for top (row 1), middle (row 2) and bottom (row 3) rows of 0.4mm BGAs.

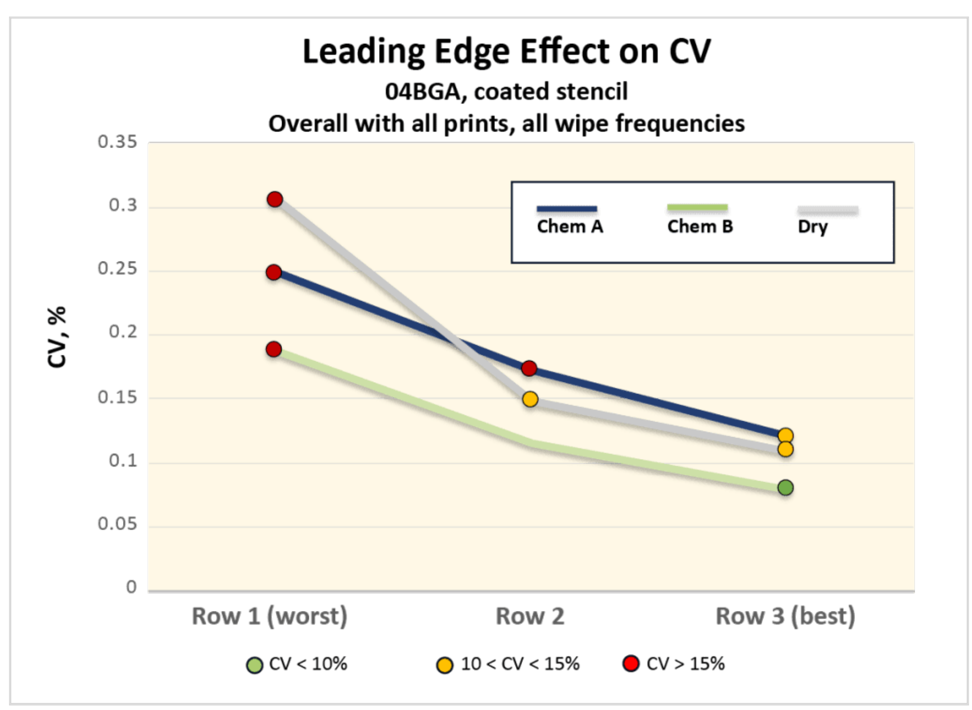

Figure 8. CV for top (row 1), middle (row 2) and bottom (row 3) rows of 0.4mm BGAs.
*Indicates a square aperture with radiused corners.

Further quantification of the leading-edge effect is outside the scope of this study, but may become the subject of others. Data from the leading edge are excluded from further analysis.

Having identified the finest pitch partially capable and eliminated the noise introduced by the uncoated stencil and the leading-edge effect, the effects of the wipe on process capability can be more precisely gauged.

Overall transfer and variation for each wipe type. Each print stroke produces 3,720 data points. There are 620 apertures per component, and six components in the two rows analyzed. Each experiment had two replicates; therefore, the sample size for each stroke is 7440.

The first analysis method examines the overall TE and CV at different wipe intervals *for all prints* in that particular interval, e.g. two prints at two prints per wipe (PPW), four prints at four PPW, etc. The final PPW is actually the 31st print and is performed after the 30th print, or 10 PPW interval.

Results of the first analysis method can be viewed in **Figures 9-11**. Examining the data for groups as a whole, several inferences can be drawn:

- Chemistry B provides the most stable process, with TEs consistently above 100% and CVs less than 15%.
- Chemistry A also exhibits TEs above 100% but does not maintain CVs below 15% at the 10 PPW interval.
- Dry wipe almost reaches 100% TE but does not achieve it. Two CV points are greater than 15%, particularly the final PPW.

To better understand the impact of underwipe chemistry, the data was also analyzed by the print quality before and after each wipe. Results of this second analysis method provide more information on the immediate effects of underwipe as opposed to the overall effects.

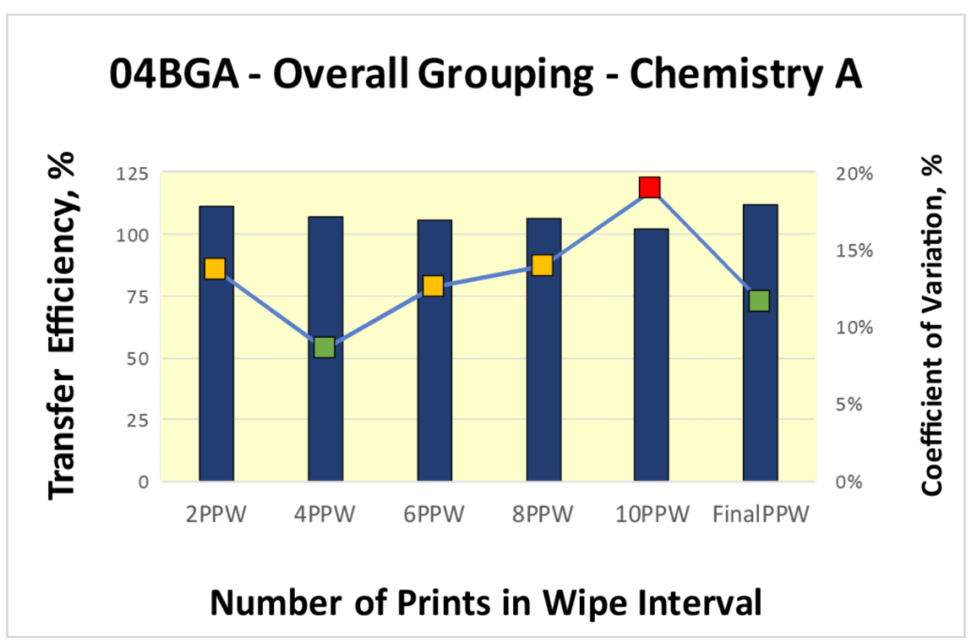

Figure 9. TE and CV at different wipe intervals.

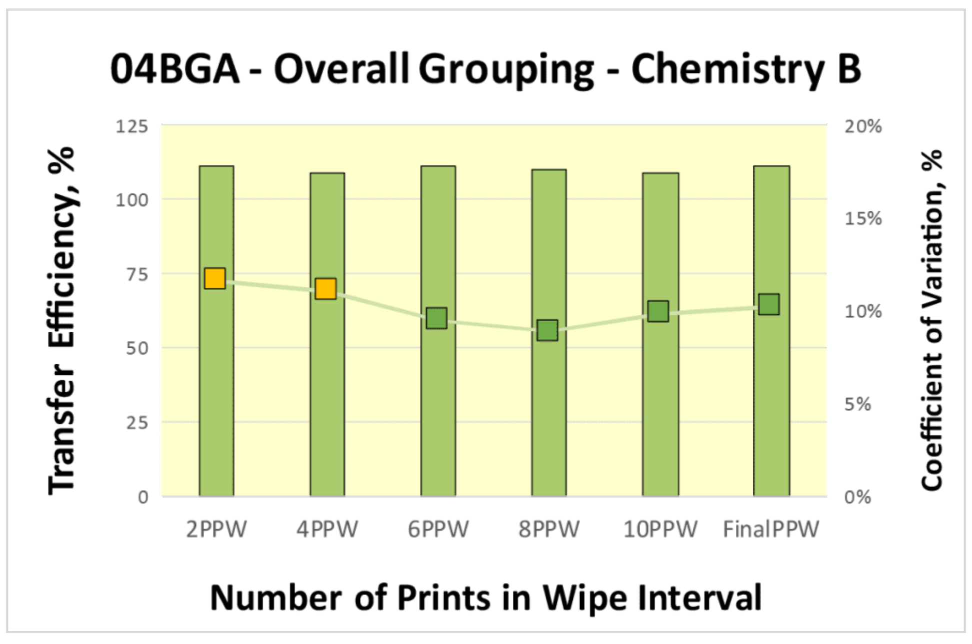

Figure 10. TE and CV at different wipe intervals.

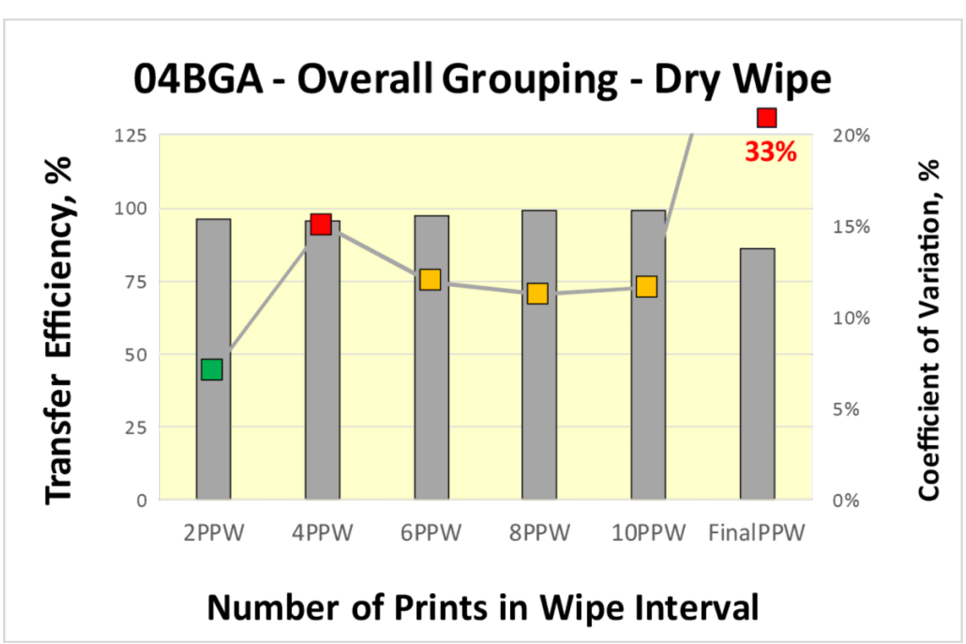

Figure 11. TE and CV at different wipe intervals.

Figures 12–14 take a closer look at what happens to the print process output when an underwipe is applied.

- Chemistry A appears very stable for pre-and post- wipe prints up to four PPW intervals. At six PPW and higher intervals, however, it appears less effective than Chemistry B.
- Chemistry B appears to trend in the opposite direction of Chemistry A. While its pre- and post-wipe prints are all of acceptable quality, the longer wipe intervals show better performance than the shorter ones.
- The dry wipe shows a repeatable pattern in CV: it is better before the wipe than after. Also, with the exception of the two PPW intervals, it shows a pattern of higher TE before the wipe and lower TE after it.

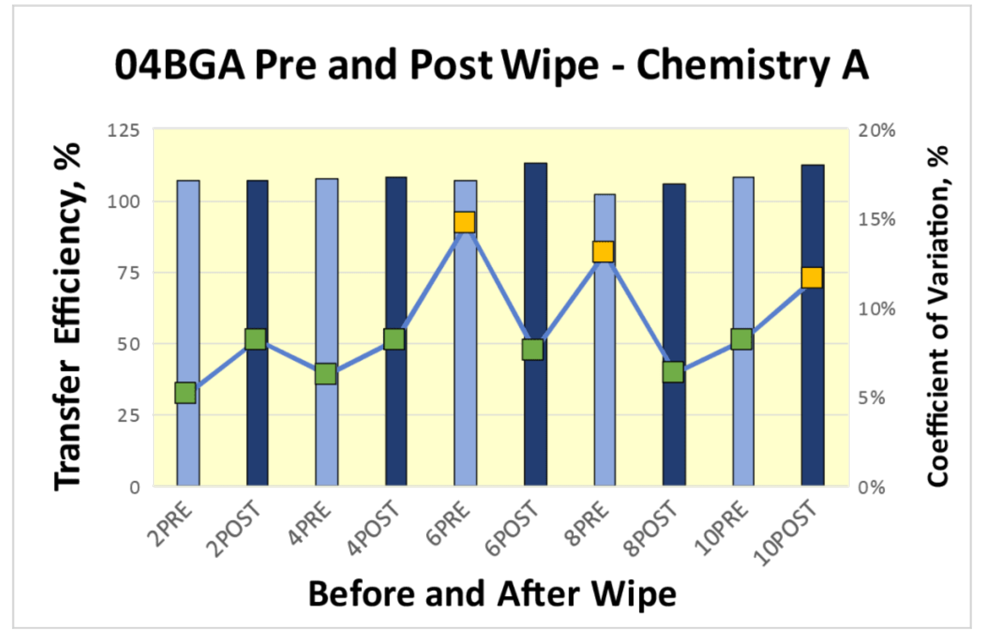

Figure 12. TE and CV before and after wipe.

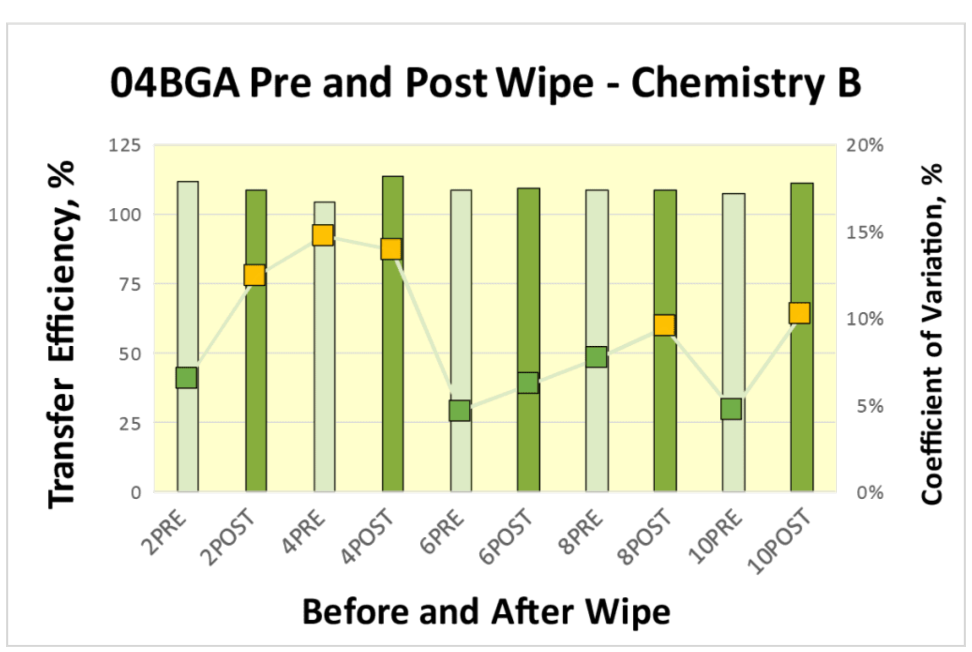

Figure 13. TE and CV before and after wipe.

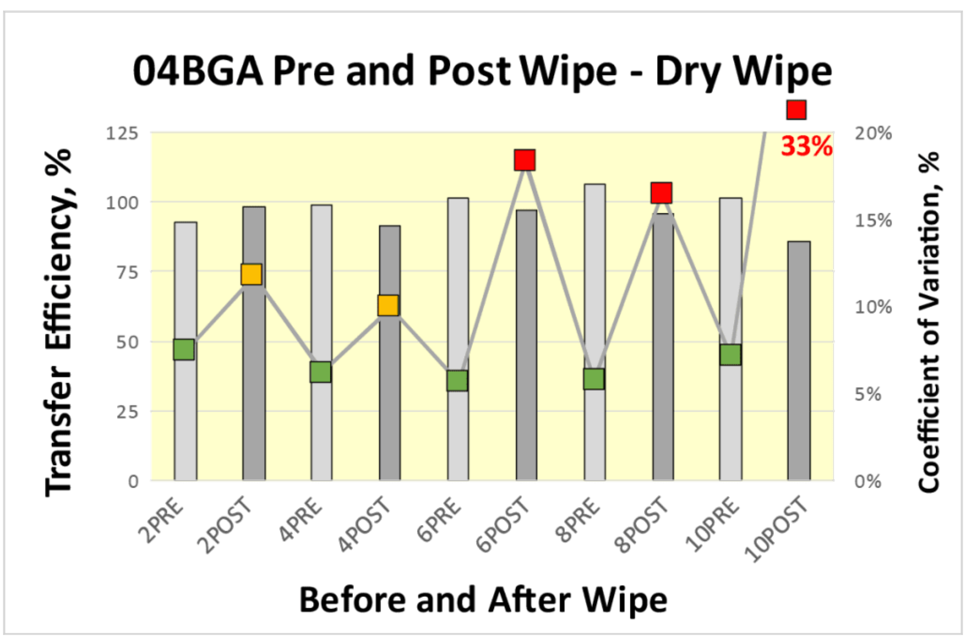

Figure 14. TE and CV before and after wipe.

Discussion and Conclusions

The print quality on these tests was remarkable compared to other production processes. This leads to conclusions that:

- Best practices are deployed throughout the process.
- Results from this study are not necessarily predictive of other production processes that are not as tightly controlled.
- Results from this study are comparable to those performed in laboratory environments rather than production environments.
- With the proper process controls and best practices in place, production environments can perform at the same quality level as laboratories.

The biggest contributor to print quality was coating the stencil with a surface-modifying coating. Stencil surface modifiers have been used for over a decade with well-documented improvements in print quality, especially at area ratios less than 0.60. It should be a given that apertures with 0.47 ARs do not get processed without a stencil coating.

The second-largest contributor was the position of the components relative to the print stroke. Apertures on the leading edge of the print stroke consistently displayed lower TE and higher CV than similar apertures later in the print stroke. Process engineers generally do not have influence over printed circuit board layout, and some printer manufacturers offer machine options to overcome leading-edge effect, including changing squeegee speed or angle as the squeegee position approaches the print area.

On apertures nearer the middle of the board, the variation due to the leading edge is minimized. Focusing on the

apertures on the edge of the process window gains the most insight into the third-largest contributor: underwipe type. It further allows exploration within the wet type of wipe.

Wet wipe outperformed dry wipe in a manner similar to previous studies (results shown in **Figures 15** and **16)**. It provided a consistent process in terms of TE throughout the different wipe intervals.

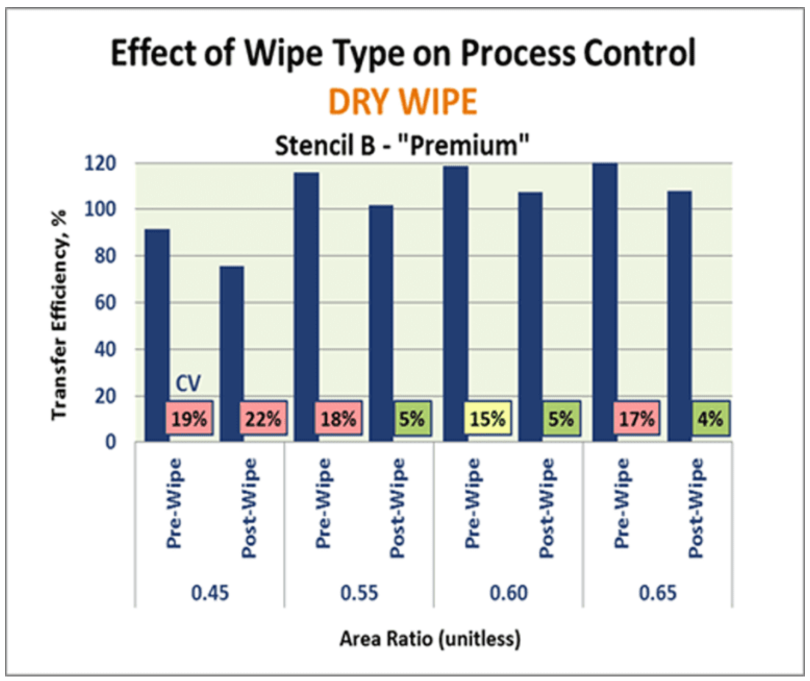

Figure 15. TE and CV with dry and wet wipe on coated stencil from 2016 study.[5]

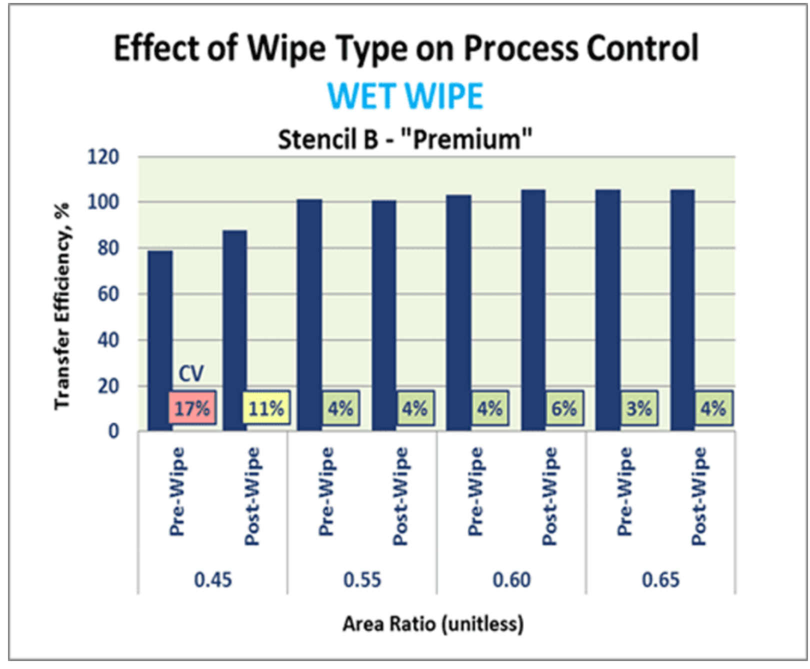

Figure 16. TE and CV with dry and wet wipe on coated stencil from 2016 study.[5]

The data in the figures show the results of a previous study[5] using chemistry B and a different solder paste. The trend is again obvious: the process "bounces" with a dry wipe. The process is consistent with a wet wipe. Similar results were recorded in the same study with an uncoated stencil.

Both studies agree: Wet wipes remove more print variation than dry wipes. Dry wipes tend to show a cyclical pattern of out-of-control and in-control before and after the wipe, whereas wet wipes tend to keep the process steadier.

Of the two wet chemistries, different characteristics were observed:

- A performed better than B on shorter wipe intervals.
- B performed better than A on longer wipe intervals.

This difference in performance – seen in both types of analysis – indicates Chemistry A may dry faster than Chemistry B, but not clean this paste quite as effectively. Conversely, Chemistry B may dry more slowly than Chemistry A, but can clean this solder paste more effectively.

The perceived difference in cleaning and drying capability leads to the conclusion that in processes where frequent wipes are required, i.e. high aperture density and low ARs, Chemistry A would be a better choice for the process. By contrast, Chemistry B would be a better choice for lower density, coarser pitch, or wider boards that would benefit from the slower drying liquid and the longer wipe intervals.

Regardless of chemistry choice, wet wiping clearly improves print performance over dry wipes. The dry wipes show increasing TE prior to wipe, decreasing TE after wipe, and CVs dramatically increasing after the wipe. This is presumably because there is nothing to dilute the sticky paste flux, and dry wiping smears it on the bottom of the stencil (even coated stencils), as demonstrated in previous studies.

Non-conforming solder paste prints cost assemblers in a multitude of ways:

- The lowest cost of a poor print is that of labor: cleaning the bare PCB, drying it and rerunning it.
- The next level of incurred cost is the touch-up or repair labor at the end of the assembly line.
- The cost of repair grows even more if it is found at test, which carries very high overhead expenses.
- The worst cost impact is when the joint fails in service and the PCB must be replaced.

SMT manufacturing is both a cost-conscious and quality-conscious business. Considerations include assembly performance class, projected lifetime, upfront investments, material costs, production costs, repair costs and brand equity. Each assembly operation is unique and has different factors influencing its manufacturing strategy. Systemic defect prevention can often be more economical than specific, after-the-fact remedies.

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CHRYS SHEA is founder of Shea Engineering Services (sheaengineering.com); chrys@sheaengineering.com. **DEBBIE CARBONI** is vice president, sales at Kyzen (kyzen.com); debbie_carboni@kyzen.com. **JOHN HANERHOFF** is senior process engineer at Garmin International (garmin.com).

Stencil Under Wipe Testing Run Sheets

Chemistry A

1) Clean and purge printer's tanks and lines
2) Make sure there's enough wiper material on the roll to complete the run
3) Clean and inspect stencil and blades

	Start Time: ___________				Stencil : Coated or Bare (circle one)
	Print Speed: ___________		Print Pressure: ___________		Separation Speed and Delay: ___________
	Top Side				
Print	Print Number	Board/Barcode Number	SPI index Number	SPI Time Stamp	Observations/Comments
	KNEAD TO ACHEIVE WORKING STATE				Min 4 kneads.Underwipe 2-3X Start print with back->front
	1	101			
	2	102			
	UNDER WIPE				
	3	103			
	4	104			
	5	105			
	6	106			
	UNDER WIPE				
	7	107			
	8	108			
	9	109			
	10	110			
	11	111			
	12	112			
	UNDER WIPE				
	13	113			
	14	114			
	15	115			
	16	116			
	17	117			
	18	118			
	19	119			
	20	120			
	UNDER WIPE				
	21	121			
	22	122			
	23	123			
	24	124			
	25	125			
	26	126			
	27	127			
	28	128			
	29	129			
	30	130			
	UNDER WIPE				
	31	131			

Appendix A – DOE Execution Step-by-Step Directions

Electronics Design Training

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Mike Creeden
Steph Chavez
Gary Ferrari
Rick Hartley
Susy Webb

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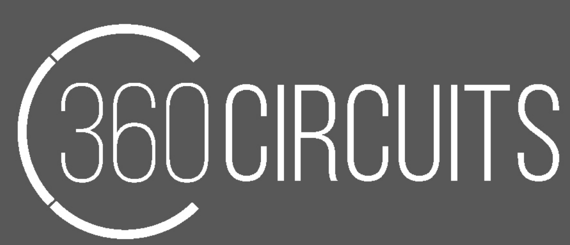

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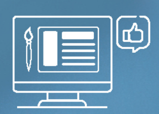

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SOLDERABILITY

Investigating Intermittent Soldering Defects

Resolving solder issues requires an examination of the entire process.

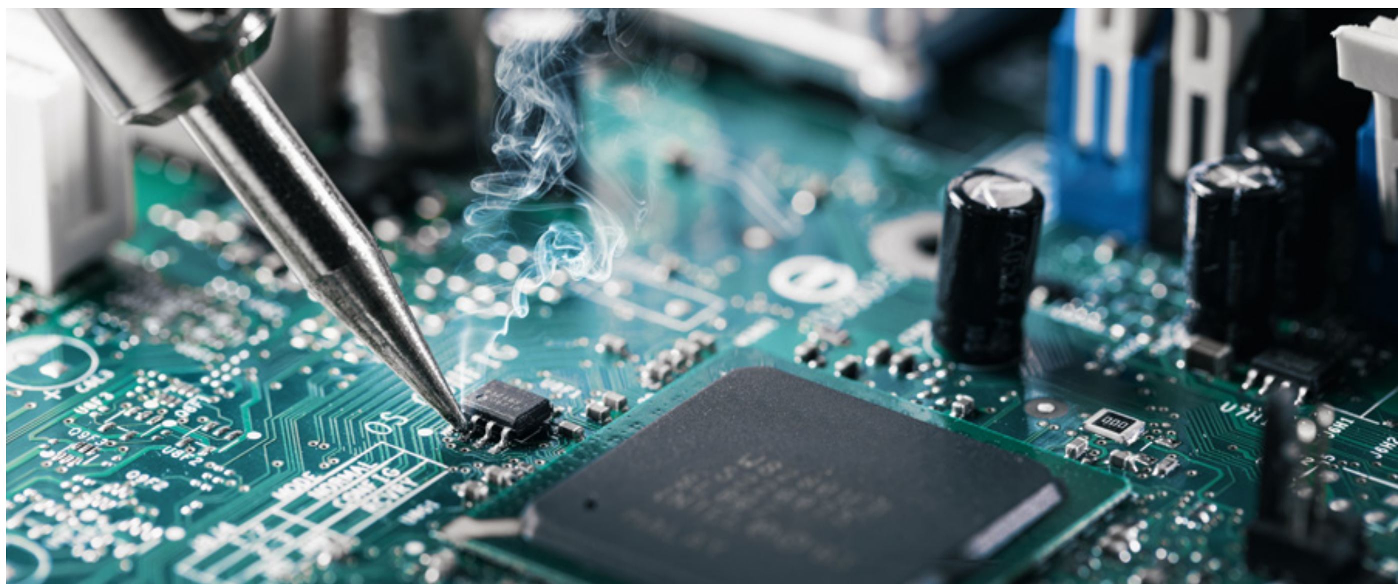
by TIMOTHY O'NEILL

The PCB assembly process creates millions of solder joints with great precision, which is why intermittent soldering defects can be particularly frustrating. It is common to assume that soldering materials, such as solder paste and flux, are the primary cause of these issues. But is solder always to blame?

In this article, we explore a real case study and shed light on the importance of accurate diagnosis and vendor collaboration.

A common misconception is that if there is a solder defect, the soldering materials are at fault. Fortunately, solder paste is not an intelligent entity capable of selectively causing defects. Solder paste is, in essence, a passive material that follows the instructions given to it during the assembly process.

Soldering defects can stem from several factors, including equipment setup, environmental conditions, component characteristics, and handling processes. Therefore, thoughtful examination of the entire soldering process is essential. This includes scrutinizing the printer setup, pick-and-place issues, reflow oven performance, and other relevant parameters.



Baking parts prior to wetting balance testing can reveal process issues and stave off time-consuming rework.

Case Study: Intermittent Solderability Issues

In the following scenario, a PCB assembler encountered a problem with intermittent solderability of a specific component in the PCB assembly line.

The intermittent nature of the issue made it particularly frustrating. At times, the solderability problem would arise, causing disruptions, but it was repairable at the rework station. While this did not completely halt production schedules, it created extra work, wasted time, and raised concerns about the overall quality of the assemblies.

Attempts to diagnose the issue involved multiple visits from the solder supplier's field engineer. Each time the engineer was present, however, the issue did not present itself, leaving the team at a loss. These instances highlighted the difficulty in diagnosing intermittent problems and the complexity involved in root cause analysis.

Investigation Checklist

The following checklist can help guide the initial investigation process:

- Screen printer setup:
    - Check that the screen printer is level and plumb.
    - Ensure screen printer rails are parallel to one another and the floor.
    - Verify the correct tooling is in place.
    - Thoroughly examine equipment cleanliness.
    - Inspect the stencil condition for any damage or clogging.
- Pick-and-place process:
    - Ensure cleanliness of the pick-and-place machine's nozzles.
    - Ensure no contamination is affecting the pick-and-place process.
    - Verify the placement settings are optimized for the assembly and components.
- Reflow oven performance:
    - Check for malfunctions in the heating elements of the reflow oven.
    - Inspect the blower motors for any issues.
    - Verify with a profiler that the reflow oven is functioning properly.

If these factors are ruled out, attention can be directed to other contributing inputs. In the aforementioned case study,

these basic factors were examined, but none was identified as the source of the intermittent solderability issue.

Examining Components, Environment and Process Settings

The next step is to examine the characteristics and behavior of any components involved in the problem, as well as environmental factors and process settings.

Internal handling refers to how a component is stored, handled, and transported within the manufacturing facility. The goal is to identify any possible mishandling and then correct it.

Environmental factors, such as temperature and humidity variations, particularly in regions with extreme climates, can affect the soldering process. In the case study, the production environment was adequately controlled. And while the facility experienced seasonal variation in temperature and humidity, these conditions were not correlated with the solderability issue.

Reflow profile optimization involves fine-tuning the reflow process to accommodate specific assembly thermal characteristics. By optimizing the reflow profile, issues such as residue relocation, solder void elimination, and improved wetting can be addressed. In the case study, the reflow profile was optimized by an SMTA-certified engineer using the latest profile data collection techniques. This optimization ensured that the reflow process was within recommended parameters.

Wetting balance testing is used to determine component solderability. However, the test cannot simulate a reflow profile and cannot detect subtle solderability issues that may occur during a three to five-minute SMT reflow profile. In the case study, wetting balance tests conducted by the component vendor did not indicate any defects, highlighting the need for additional investigation.

Rapid application of high-temperature solder during wetting balance tests may reveal gross solderability issues but can also break down oxides present on the component, unintentionally masking defects that may emerge during the longer, hotter reflow profile. Moreover, the reflow process can exacerbate oxide formation before soldering occurs, potentially worsening any issues.

To overcome these limitations, customer-supplied components were subjected to baking at 125°C for five minutes, mimicking the exposure to reflow. After this treatment, the components were subjected to wetting balance testing.

The results of the bake process were immediately apparent – the components did not solder correctly after exposure to elevated temperatures. This testing was repeated on multiple component lots, and each time, the same solderability issue was observed, consistent with the behavior experienced at the customer's site. The evidence allowed the assembler to present the component vendor with clear and undeniable information, compelling them to address the issue and provide a remedy.

Vendor Collaboration

Resolving soldering issues can be challenging, often complicated by conflicting advice from multiple vendors involved in the PCB assembly process. This can leave manufacturers feeling uncertain and overwhelmed.

It is crucial to recognize that vendors play a pivotal role in addressing soldering issues effectively. They possess valuable expertise, insights, and product knowledge that can contribute to finding solutions. Rather than perceiving conflicting advice as a hindrance, it should be approached as an opportunity to engage in meaningful collaboration and problem-solving.

Commitment, patience and vendor support are key when it comes to resolving soldering issues. Choosing vendors who actively support their products and are committed to assisting with customer processes is a smart decision that can lead to effective resolution.

TIMOTHY O'NEILL is director of product management at AIM Solder (aimsolder.com); toneill@aimsolder.com.

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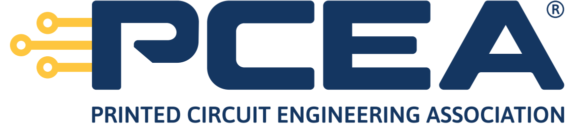

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PiP vs. PTH for Connectors

Which process offers fewer steps – and less contamination?

IN A PERFECT world, the electronics industry would have migrated to 100% SMT by now. Unfortunately, through-hole remains a required technology for some products. In particular, through-hole connectors are often preferred over their SMT counterparts due to the robust solder joints they provide.

From a Lean perspective, a requirement for mixed technology can open the door to several of the seven wastes, as it can drive the need for processes not required for a 100% SMT printed circuit board assembly (PCBA). In particular, the wastes of transport and processing can occur when separate solder processes are required for the same PCBA. The need to do multiple thermal cycles when processing via reflow and wave solder also potentially adds to the waste of defects, as it can plant the seeds for premature component failure and handling damage.

SigmaTron International's facility in Chihuahua, Mexico, utilizes pin-in-paste (PiP) as an alternative to using two separate solder processes. In the PiP process, solder paste is deposited inside through-hole vias and pads prior to component placement. SMT and through-hole components then go through the reflow soldering process. In one recent project, the team selected PiP as an alternative to wave soldering because the customer had concerns about wave soldering's added ionic contamination.

In this specific PiP process, two- and 16-pin through-hole connectors are reflowed using a low-temperature tin-bismuth solder paste that reflows at 190°C. The connectors are tolerant of oven temperatures up to 260°-270°C. The critical-to-quality (CTQ) dimension is the lead-to-hole ratio. Good stencil design is imperative, as the amount of paste in the hole must be carefully controlled.

In developing the process, the team designed the stencil and validated its design through trials. X-ray inspection was used to control filling of the holes. The team utilized 3-D solder paste inspection (SPI) for process confirmation and process monitoring. Automated optical inspection (AOI) was used to confirm good solder fillets.

The advantages to this process include:

- Better solderability
- Ease in controlling the process
- One thermal cycle – which reduces the potential for component failure post-reflow or in the field

- Elimination of the additional handling – and potential handling damage – from a wave solder process
- Elimination of pallets and shielding required for wave soldering
- No added ionic contamination, eliminating the need for aqueous cleaning
- Improved cycle time
- Lower cost than using both reflow and wave solder.

Overall, this simpler approach is inherently Lean because it eliminates the additional processes and handling from using two separate solder processes.

As with any process, PiP is not universally the best choice for mixed-technology PCBAs. Wave solder and selective solder continue to be viable options in some applications. The number of through-hole components on the PCBA, PCB layout, through-hole component heat sensitivity, end-product application, product volumes and specific customer concerns relative to cleanliness or cost can impact preferred choice. Facilities continuously running wave solder equipment would see less of a savings factor than facilities that only intermittently use wave soldering. And while the PiP process is easier to control than traditional wave solder, it does require automated inspection to monitor solder paste deposition and solder fillet quality.

This example illustrates benefits of simple solutions when legacy technology would otherwise drive additional processing. It also underscores the value of inline inspection technology in maintaining levels of process control in solder paste deposition that enable a broader range of soldering options.

ALVARO GRADO is manufacturing engineering & quality manager at SigmaTron International (sigmatronintl.com) in Chihuahua, Mexico; alvaro.grado@sigmatronintl.com.

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ALTAIR SIMSOLID FOR ELECTRONICS

SimSolid for electronics brings multi-physics scenario exploration for electronics, from chips, PCBs, and ICs to full system design. Is said to accurately predict complex structural problems with high speed while eliminating the complexity and labor of modeling. Eliminates geometry simplification and meshing to deliver results in seconds to minutes – up to 25x faster than traditional finite element solvers – and handle complex assemblies. Tackles signal integrity (SI), power integrity (PI), and electromagnetic compatibility/interference (EMC/EMI), all while making electromagnetic simulations more accessible and efficient.

Altair

altair.com

DOOSAN DS-7409DQN CCL

DS-7409DQN and DS-7409DQN2 copper-clad laminates enable large volumes of data transmission with minimal signal loss, for use in switches and routers. Are suitable for a range of applications, including memory semiconductor applications such as mobile and PC DRAM/NAND, and system semiconductor applications such as RF SiP, AiP, FC-CSP, and FC-BGA. Are halogen-free and ultra-low loss.

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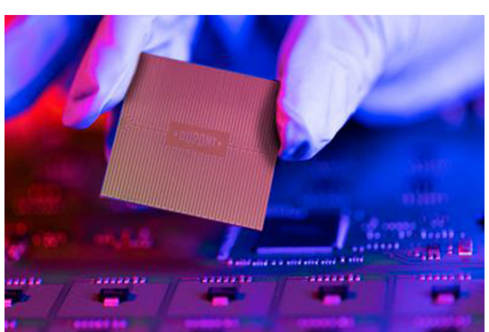


DUPONT PYRALUX ML LAMINATES

DuPont's Pyralux ML double-sided metal-clad laminates are for optimal thermal management for high-reliability applications such as aerospace, defense, electric vehicles, AI-related networking and other electronic devices. Contain metal alloy, such as copper-nickel, featuring Kapton all-polyimide dielectric technology, and provide essential thermal resistance for heating, thermal conductivity to improve the desired heat transfer, resistivity for higher heat output, and thermoelectric properties as needed for the application. Come in a variety of dielectric and foil types, thicknesses and a range of metal constructions, and are fully compatible with most conventional circuit fabrication processes.

DuPont

dupont.com

KYOCERA AVX SNA AND SNL SERIES CAPACITORS

SNA and SNL Series snap-in aluminum electrolytic capacitors are said to deliver high-reliability, high-voltage and high-CV performance over long lifetimes. Are lead-free compatible and RoHS compliant, rated for temperatures extending from -25° to +105°C, and are said to be ideal for use in commercial and industrial applications including frequency converters, solar inverters, power inverters, energy storage systems, and power supplies.

SNA series exhibits high ripple current capabilities, long lifetime performance and endurance of 5,000 hr. at 105°C. Are available with three rated voltages (250, 420, and 450VDC), 24 case sizes spanning 22mm x 25mm to 35mm x 50mm (D x L) and capacitance values extending from 82μF to 1,500μF ±20%.

SNL series exhibits endurance of 3,000 hr. at 105°C. Come in eight rated voltages (160, 200, 250, 350, 400, 450, 500, and 550VDC), 36 case sizes spanning 22mm x 20mm to 35mm x 60mm (D x L), and capacitance values extending from 68μF to 2,200μF ±20%.

Kyocera AVX

kyocera-avx.com

MKS ESI GEODE G2 LASER SYSTEM

ESI Geode G2 laser drill offers advancements in beam control capabilities, optical transmission, thermal management and AOD technology. Features lightweight frame design of the Geode G2 to provide flexibility for factory floor layouts, and utilizes HyperSonix technology that shapes laser pulses with sound waves for better throughput and quality. Also uses AcceleDrill to distribute pulse energy for maximum throughput and permit multiple via sizes in one pass. Beam Characterization Tool for CO_2 via drilling monitors beam quality and spot health.

MKS Instruments
mks.com

SAMTEC RF EDGE LAUNCH CONNECTORS

RF edge launch connectors feature a narrow body design that is said to be 33% smaller than traditional edge launch connectors. Are for use in a lab setting for high-frequency test and measurement applications, high-speed digital component test and evaluation boards. Feature frequency capabilities of DC to 67GHz (185-EL Series), DC to 50GHz (240-EL Series) and DC to 40GHz (292-EL Series) and include interface types of 1.85mm, 2.40mm and 2.92mm. Also feature compression mount to the printed circuit board instead of requiring solder, which permits increased signal integrity performance capabilities and are reusable for up to 500 mating cycles.

Samtec
samtec.com

STACKPOLE AUTOMOTIVE GRADE CHIP RESISTOR

RPCA series chip resistor is AEC-Q200 qualified and is said to provide pulse handling. Passes ANSI/EIA977 sulfur test with minimal resistance shift at 105°C. Is designed for automotive electronics, medical applications, non-established reliability military and aerospace, as well as instrumentation and metering.

Stackpole Electronics

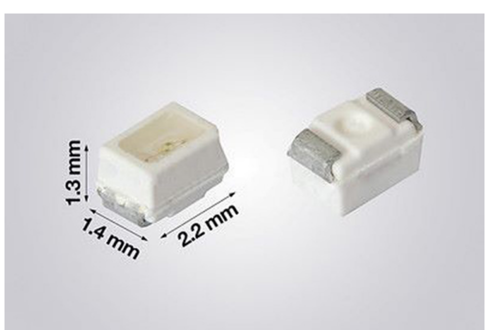
seielect.com

VENTEC BONDPLY DIELECTRICS

Pro-bond and Thermal-bond bond ply dielectrics are formulated for high-speed signal integrity with low losses and thermal management in ML PCB stackups. Initial range includes resin-coated copper (RCC) and resin-coated film (RCF) bondply b-stage dielectric materials. RCC bondply is an unreinforced adhesive system coated onto ultra-thin copper foil (1.5-5.0µm supported on an 18µm carrier foil) for use in high-performance and high-reliability multilayer PCB stackups. RCF bondply is an unreinforced adhesive system coated onto PET film for use in high performance and high-reliability multilayer PCB stackups.

Ventec

ventec-group.com



VISHAY BLUE AND TRUE GREEN LEDS

VLMB2332T1U2-08 and VLMTG2332ABCA-08 surface-mount LEDs measure 2.2mm by 1.3mm by 1.4mm and feature

a luminous intensity of 440mcd and 2300mcd, respectively. Are designed for applications such as medical light treatment; signal lights for agricultural equipment and energy generation systems; indicators and backlighting for office, entertainment and telecommunications equipment; LCD switches and symbols for general use. Feature a lead-frame embedded in a white thermoplast and offer a ±60° angle of half-intensity, a wide viewing angle of 120° for homogeneous illumination and backlighting, and forward voltage of 2.9V typical. Are RoHS-compliant, halogen-free and Vishay Green, available in 8mm tape, offer an ESD-withstand voltage up to 2kV in accordance with JESD22-A114-B and are compatible with preconditioning according to JEDEC Level 2a, IR reflow soldering according to J-STD-020 and automatic placement equipment.

VLMTG2332ABCA features a typical wavelength of 525nm at 20mA, and is said to be ideal for heart rate monitoring applications in fitness trackers and other devices that rely on variations in green light absorption.

VLMB2332T1U2-08 offers a typical wavelength of 465nm at 20mA and is said to be optimized for smoke detectors that utilize short wavelength blue light for the detection of small particles.

Vishay Intertechnology

vishay.com

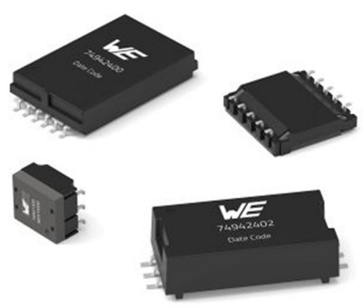
VISHAY TVS SERIES

New series of transient voltage suppressors (TVS) are designed to enhance protection and efficiency in automotive and industrial electronics. 6DFNxxA, 6DFNxxxCA, T6NxxA, and T6NxxxCA series feature a peak pulse power of 600W at 10/1000µs and exhibit low leakage current down to 1µA. Are housed in DFN3820A package, which offers an 85% size decrease compared to SMB (DO-214AA) package and a 42% reduction over SlimSMAW (DO-221AD). Are said to offer clamping capability, with maximum clamping voltages ranging from 16.7V to 137V, and include wettable flanks to facilitate AOI processes. Are RoHS-compliant and halogen-free, with matte tin-plated leads that meet JESD 201 class 2 whisker test.

6DFNxxA and 6DFNxxxCA series are tailored for signal line protection across a range of applications, from server power modules and digital media controllers in computer and consumer sectors to industrial robot control boards and automation systems. T6NxxA and T6NxxxCA PAR TVS series are AEC-Q101 qualified and support high-temperature operations up to +185°C, and are designed primarily for automotive applications including advanced driver assistance systems, battery management systems and infotainment systems.

Vishay Intertechnology

vishay.com

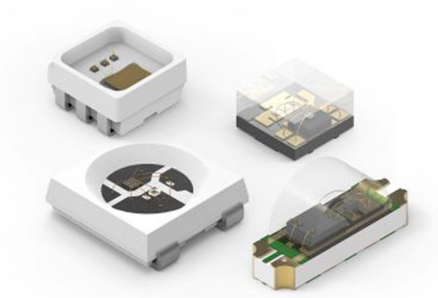


WÜRTH ELEKTRONIK WE-BMS TRANSFORMERS

WE-BMS transformer series for battery management systems now features versions for an operating voltage of $1500V_{DC}$. Features enhanced isolation in line with IEC 62368-1 with triple-insulated wire (primary and secondary side), as well as galvanic isolation and a test voltage of $6400V_{DC}$, and for use in large stationary energy storage systems from solar and wind farms, in intermediate storage systems in high-power charging stations to balance out peak loads, or for uninterruptible power supplies used in critical infrastructures.

Würth Elektronik

we-online.com



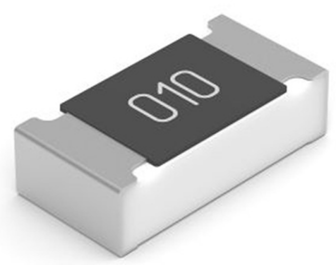
WÜRTH ELEKTRONIK WL-ICLED SERIES

WL-ICLED series combines a red, green and blue LED with a programmable controller IC. Available in four designs (2020 Chip LED compact, 3210 Chip LED Side View, 2121 PLCC6 with bypass and 5050 PLCC4) and is individually controllable in pixel color and brightness levels from 0-100%. Is capable of more than 16 million different color and brightness levels and is compatible with open source libraries such as FastLED. Requires fewer components (such as series resistors) and is more compact than solutions with separate LEDs. Also features an MSL3 moisture sensitivity level, with some models complying with protection class IPx7. Includes gold plating on Chip LED models and silver coating for PLCC models for better solderability. Applications include signal control systems, full-color matrix

displays, audio and gaming systems, indoor lighting and displays on e-mobility charging stations.

Würth Elektronik

we-online.com



WÜRTH ELEKTRONIK WRIS-RSKS RESISTORS

WRIS-RSKS family of anti-sulfur resistors is for applications susceptible to exposure from sulfur compounds. Features an additional layer of nickel-chromium alloy that protects silver-based electrodes from contact with sulfur gasses. Has a sulfur resilience designed for long-term reliability under harsh conditions and is tested in accordance with ASTM B-809. Operating temperature ranges from -55° to +155°C and comes with resistance values from 1Ω to 10MΩ, temperature coefficients of ±100, ±200 and -200~+400ppm/°C, resistance tolerances of ±1% and ±5% and power ratings of 0.1 to 0.5W.

Würth Elektronik

we-online.com

COGISCAN FACTORY INSIGHTS

Factory Insights is a customizable factory data platform built for circuit board assembly and complex manufacturing

ecosystems. Features a fully customizable platform that allows users to build their own KPIs and dashboards, or use and personalize pre-built dashboards. Permits seamless sharing and exchanging of calculated metrics with other AI platforms, as well as role-specific dashboards that visualize relevant KPIs for specific roles.

Cogiscan

cogiscan.com

HENKEL LOCTITE ECCOBOND UF 9000AE ENCAPSULANT

Loctite Eccobond UF 9000AE is designed to protect large die within flip-chip BGA (FCBGA), high-density fan-out (HD-FO), and 2.5-D advanced packaging devices. Completely envelops fine-pitch, low gap height die interconnects for rigid protection against stress, and low shrinkage and toughness provide die and underfill crack resistance, while low CTE protects against warpage. Also features low resin bleed out and forms narrow fillets, permitting the dense die integration inherent in advanced packaging techniques. Is said to demonstrate 20% faster flow on a 40mm x 40mm die, and edge-to-edge capillary flow efficiency ensures interconnect encapsulation prior to any material gelation. Has been validated on dies as large as 50mm x 50mm and within packages up to 110mm x 110mm.

Henkel

henkel.com

MASTER BOND EP114 UNDERFILL EPOXY

EP114 is a two-component, low-viscosity, NASA low outgassing rated, heat-cured epoxy that can be effectively utilized for underfill, coating, impregnating and porosity sealing applications. Features high dimensional stability due to its nano-silica filler material and has been successfully tested for abrasion resistance per ASTM D4060-14 and readily withstands 1,000 hr. at 85°C and 85% relative humidity. Is said to have excellent electrical insulation properties with a volume resistivity greater than 10^{14}ohm-cm and a dielectric constant of 3.35 (60Hz) at 25°C. Features an exceptionally low coefficient of thermal expansion of 20-22 x 10^{-6}in/in/°C, compressive strength of 24,000-26,000psi, ultra-high modulus of more than 1 million psi and hardness of 85-95 Shore D at 25°C. Also has a Tg of more than 200°C, features a mixed viscosity of 500-1,500cps and offers a long working life after mixing.

Master Bond

masterbond.com

MEK EZPRO AOI PROGRAMMING TOOL

EZPro software permits preparation of approximately 70% of an AOI program in typically 20 min. using only CAD + Gerber data, eliminating the need for a PCB. Follows a streamlined, programmer-independent procedure to reduce dependency on specific individuals and conduct constant fine-tuning to enhance overall operational efficiency. Features a user-friendly interface that allows users with minimal technical expertise to operate effectively, and uses AI tools to recognize CAD formats and footprints of package types, including multi-panel recognition. Comprehensive AI package recognition extends to all three dimensions of body and lead dimensions for various package types, such as SOPs, SOTs, QFPs and more. Is said to seamlessly integrate across the ISO-Spector true 3-D AOI system and the full range of Mek THT AOI systems.

Marantz Electronics

marantz-electronics.com

MVP VERSA DUO AOI

Versa Duo AOI features high-resolution optics technologies and a laser profiler to offer advanced inspection across multiple markets. Permits highest defect detection and measurement and traceability in a single platform, and incorporates a precision granite stage to enhance stability and reduce vibrations for heightened positional accuracy. Features advanced laser technology with a repeatability of 0.5µm and has access to MVP's algorithm capabilities to

benefit from decades of defect and measurement-based capabilities.

Machine Vision Products

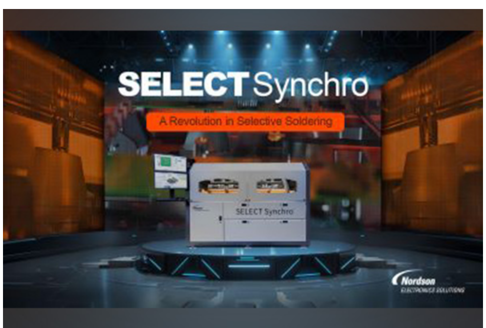
visionpro.com

MYCRONIC DEEPREVIEW ADC SYSTEM

DeepReview automatic defect classification system leverages AI to reduce false call rates while improving first-pass-yield in 3-D AOI. Allows manufacturers to train neural network on their own inspection data, allowing them to apply, adapt and refine their own defect classification models according to in-house inspection standards – resulting in a reported 50-100% reduction in potential false calls for eligible components. Handles various defect sources such as solder joints, bridges, offsets and coplanarity, with plans to expand package library to cover most electronic components in the near future.

Mycronic

mycronic.com



NORDSON SYNCHRO 3 SELECTIVE SOLDERING

Synchro 3 selective soldering system offers up to three solder pots to match manufacturing needs for different alloys, and different or singular nozzles. Uses synchronous motion technology to reduce conveyance time and boost throughput by 20-40% for most applications while reducing footprint up to 60%, and is able to handle boards up to 2500 x 460mm. Automatically balances soldering tasks between pots to increase throughput and features process control features as well as point-and-click programming and fiducial finding. Is part of SELECT Synchro series.

Nordson Electronics Solutions

nordson.com

NORDSON EFD GVPLUS AND PROX DISPENSERS

GVPlus and PROX families of automated fluid dispensing products feature three axes and motion, workspace, repeatability, payload, setup and vision technology enhancements.

GVPlus automated fluid dispensing family features repeatability at 8μm, improving repeatability to ±0.008 mm, as well as easier setup due to a new dual mounting flange that enables a tool payload of up to 4.5kg (10lb.). Also features a working area of 400mm x 400mm, and enhancements to CCD smart vision camera deliver high quality images even on surfaces like glass, mirrors, plastics and nontransparent clear surfaces. Proprietary dispensing software confirms and automatically adjusts as in-process variations occur.

PROX automated fluid dispensing family features new linear motors that offer better actuation speed, reduced maintenance needs and improved durability. Extend a best-in-class X, Y, and Z-axis repeatability of ±0.003mm and the working area is expanded to 500mm x 500mm. Also features a CCD smart vision camera that provides precise, high-quality images that are confirmed by proprietary DispenseMotion software and operates on challenging surfaces like glass, mirrors, plastics and non-transparent clear surfaces.

Nordson EFD
nordsonefd.com

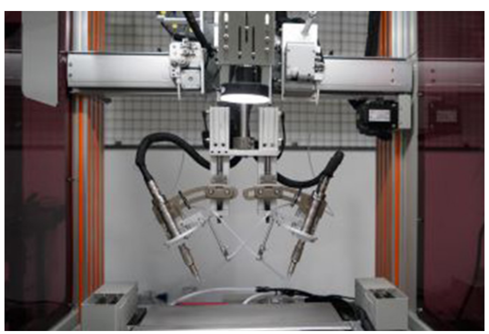
PANASONIC NPM-GH PICK-AND-PLACE MACHINE

NPM-GH is a pick-and-place machine with a mounting accuracy of ±15μm. Uses a smaller and lighter mounting head to achieve high-level productivity of 51,000cph and can also be configured as what is said to be the industry's first ultra-precise specification (±10μm). Includes an enlarged operation screen featuring an intuitive user interface,

making the machine easy to train on and execute operations in real-time.

Panasonic Connect

panasonic.com



SASINNO IBOT-I1/2S SOLDERING SYSTEM

iBot-i1/2s soldering system features PC-based control system for accuracy and an intuitive user interface compared to traditional teaching pad-based controls, as well as integrated advanced cameras for both programming and fiducial checking. Also includes a drive system using servo motors and ball screws that eliminate the need for regular tension adjustments common for timing belt-driven stepper motors, and features original JBC solder stations to offer heat recovery and durability. Also offers dual-tip soldering capabilities on a single table to streamline the soldering process.

SASinno Americas

sasinno.com

TRI TR7600F3D SII PLUS AXI

TR7600F3D SII Plus 3-D CT AXI integrates a next-generation 110kv x-ray source and 3-25µm high-resolution detectors and AI-powered inspection algorithms. Is capable of inspection across various components, including BGA, QFN, SiP, PTH, PoP, wire and die bond, and is designed for the inspection of high-reliability electronics manufacturing industries such as advanced packaging, automotive, aerospace and medical. Features EtherCAT for enhanced

connectivity and Smart Board Warpage Control, plus integrates with Smart Factory production lines and the MES of user's choice. Supports current Smart Factory Standards, including IPC-CFX, IPC-DPMX, and The Hermes Standard (IPC-HERMES-9852).

TRI
tri.com.tw

pcbchat.com

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The PCB Podcast

In Case You Missed It

AOI

"PCB Defect Detection Algorithm Based on CDI-YOLO"

Authors: Gaoshang Xiao, *et. al.*

Abstract: Existing deep learning-based PCB defect detection methods are difficult to simultaneously achieve the goals of high detection accuracy, fast detection speed, and small number of parameters. Therefore, the authors propose a PCB defect detection algorithm based on CDI-YOLO. First, the coordinate attention mechanism (CA) is introduced to improve the backbone and neck network of YOLOv7-tiny, enhance the feature extraction capability of the model, and thus improve the accuracy of model detection. Second, DSConv is used to replace part of the common convolution in YOLOv7-tiny to achieve lower computing costs and faster detection speed. Finally, Inner-CIoU is used as the bounding box regression loss function of CDI-YOLO to speed up the bounding box regression process. The experimental results show that the method achieves 98.3%mAP on the PCB defect dataset, the detection speed is 128 frames per second (FPS), the parameters are 5.8M, and the giga floating-point operations per second (GFLOPs) is 12.6G. Compared with the existing methods, the comprehensive performance of this method has advantages. (*Nature*, March 2024, https://doi.org/10.1038/s41598-024-57491-3)

Depanelization

"Review of Methods for PCB Panel Depanelization and Methods for Correct Assembly of Electronic Components on PCB Panels"

Authors: Mateusz Łyczek and Wojciech Skarka

Abstract: Currently, processes related to PCBs, such as depanelization and checking the correct functioning of the boards, are carried out in separate devices. The authors review the literature and analyze trends related to these aspects of PCB panel manufacturing. The purpose of this analysis is to indicate the currently used depanelization methods and methods for checking the correctness of the assembly of electronic circuits on PCB panels. The publications were found in such knowledge bases as Scopus, IEEE Xplore or Emerald insight. In the following article, a systematic literature analysis along with a mapping study is used. This publication provides a review of selected scientific papers found in the above-mentioned databases. Based on these analyses, insights related to future work on both aspects of PCBs were presented. These insights are part of the development of new integrated devices for depanelization and verification of PCBs. (*Electronics*, March 2024, https://doi.org/10.3390/electronics13071255)

DRC

"Methodology of Resolving Design Rule Checking Violations Coupled with Fully Compatible Prediction Model"

Authors: Suwan Kim, *et. al.*

Abstract: Resolving the design rule checking (DRC) violations at the pre-route stage is critically important to reduce the time-consuming design closure process at the post-route stage. Recently, noticeable methodologies have been proposed to predict DRC hotspots using machine learning based prediction models. Little attention has been paid to how the predicted DRC violations can be effectively resolved, however. The authors propose a pre-route DRC violation resolution methodology that is tightly coupled with fully compatible prediction model. Precisely, the authors devise different resolution strategies for two types of DRC violations: 1) pin accessibility (PA)-related and 2) routing congestion (RC)-related. To this end, the authors develop a fully predictable ML-based model for both PA and RC-related DRC violations, and propose completely different resolution techniques to be applied depending on the DRC violation type informed by the compatible prediction model such that for 1) PA-related DRC violation, the authors extract the DRC violation mitigating regions, then improve placement by formulating the whitespace redistribution problem on the regions into an instance of Bayesian Optimization problem to produce an optimal cell perturbation, while for 2) RC-related DRC violation, the authors manipulate the routing resources within the regions that have high potential for the occurrence of RC-related DRC violations. Through experiments, it is shown that the authors' methodology resolves the number of DRC violations by 26.54%, 25.28%, and 20.34% further on average over that by a conventional flow with no resolution, a commercial ECO router, and a state-of-the-art academic predictor/resolver, respectively, while maintaining comparable design quality. (*ISPD '24: Proceedings of the 2024 International Symposium on Physical Design*, March 2024, https://doi.org/10.1145/3626184.3633324)

Flexible Electronics

"Density Functional Theory of Straintronics Using the Monolayer-Xene Platform: A Comparative Study"

Authors: Swastik Sahoo, *et. al.*

Abstract: Monolayer silicene is a front runner in the two-dimensional (2-D)-Xene family, which also comprises germanene, stanene, and phosphorene, to name a few, due to its compatibility with current silicon fabrication technology. Here, the authors investigate the utility of 2-D-Xenes for straintronics using the *ab initio* density functional theory (DFT) coupled with quantum transport based on the Landauer formalism. With a rigorous band structure analysis, the authors show the effect of strain on the *K*-point and calculate the directional piezoresistances for the buckled Xenes as per their critical strain limit. Further, the authors compare the relevant gauge factors (GFs) and their sinusoidal dependencies on the transport angle akin to those of silicene and graphene. The strain-insensitive transport angles corresponding to the zero-gauge factors for silicene and germanene are 81° and 34° for armchair (AC) and zigzag (ZZ) strains, respectively. As the strain limit is increased to 10% in stanene, there are notable changes in the fundamental parameters, which entail a change in the critical angle along the armchair (69°) and zigzag (34°) directions. The small values of gauge factors can be attributed to their stable Dirac cones and strain-independent

valley degeneracies. The authors also explore conductance modulation, which is quantized in nature and exhibits a variation pattern similar to that of other transport parameters against applied strain. Based on the obtained results, the authors propose the buckled Xenes as an interconnect in flexible electronics and as promising candidates for various applications in straintronics. (*ACS Applied Nano Materials*, January 2024, https://doi.org/10.1021/acsanm.3c05288)

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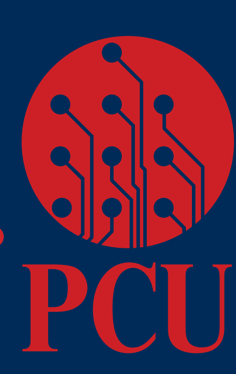

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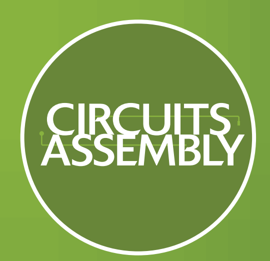

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