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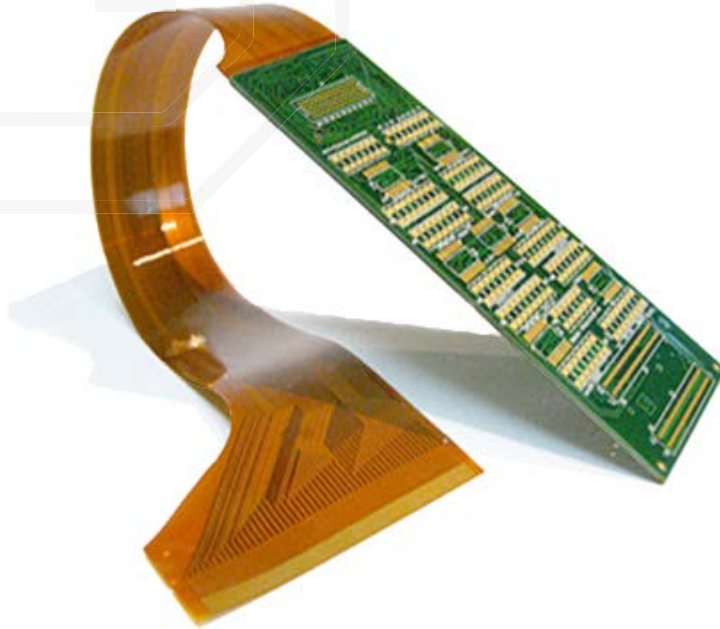
MORE *than* MOORE

Are System-in-Package
Solutions the Way Forward?

• A Visit to **ASC Sunstone**
PCB East Highlights Healthy Industry
Implementing **AI** in PCB Design •

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FIRST PERSON

THE ROUTE

Mapping the path for AI.

Mike Buetow

MONEY MATTERS

BOARD BUYING

More tariffs aren't the answer.

Greg Papandrew

FOCUS ON BUSINESS

A private equity investment checklist.

Jake Kulp

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E. Jan Vardaman

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John Burkert Jr.

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Alun Morgan

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Alvaro Grado

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AROUND THE WORLD

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OFF THE SHELF



FEATURES

PCB FABRICATION

Sunny Times at Sunstone Circuits

Fresh off its merger with American Standard Circuits, ASC Sunstone is entering a new phase of its business with higher technology and more advanced capabilities. PCD&F visited the company in April to get an inside look at its growing operations.

by TYLER HANES

PCB EAST RECAP

'Everybody is Growing'

This year's exhibition at PCB East featured more than 65 companies across the printed circuit industry, and reports from the show floor show that the industry is healthy and growing.

by TYLER HANES

DESIGN TOOL ADVANCES

AI: The Shiny New Tool in the Engineer's Toolbox

AI use in the PCB design field is still developing, but capabilities are rising. By taking advantage of its ability to learn from both good and bad designs, AI can become a valuable tool for new designers to perform tasks traditionally achievable only by experts.

by DAVID WIENS

PACKAGING (COVER STORY)

System-in-Package and Multichip Module Technology

The development of the system-on-chip (SoC) has led to smaller form factors in electronics, but those complex systems generate high costs and have other market constraints. The integration of separately manufactured components into a higher-level assembly – system-in-package (SiP) – can leverage the advanced capabilities of packaging technology but with better yield and lower overall cost.

by YANIV MAYDAR

SMT SOLDERING

How to Stay Within the SMT Assembly Process Window

The assembly process window is the range of parameters within which solder paste will meet optimal performance standards, and straying outside that window can lead to defects, rework and inconsistencies. Understanding the interplay between paste properties and the broader assembly environment can allow professionals to maintain a high standard of efficiency and reliability.

by KEVIN PIGEON

ON PCB CHAT (PCBCHAT.COM)

PCB Chat

DESIGNING ELECTRONICS FOR HARSH ENVIRONMENTS
with DR. ANDRE KLEYNER

SMT SOLDERING AND INSPECTION
with GUS MAVROU, MARK STANSFIELD and JESPER LYKKE

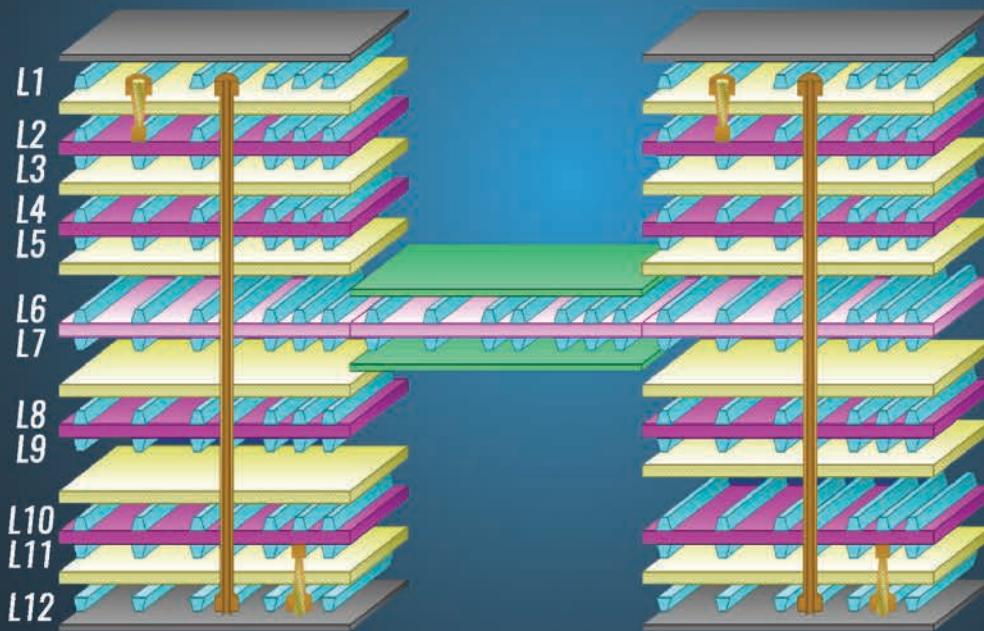


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DIRECTORY OF EMS COMPANIES



A Status Plan for Implementing AI Takes Shape

ARTIFICIAL INTELLIGENCE AS applied to electronics design and manufacturing is in its infancy, but interest is high and questions abound as to what it means – and even what it is.

AI is seen as similar to the Internet in 1995: a big, wide-open technology that companies had to embrace and understand. Success depends on narrow implementations that permit companies to see clearly what the return or improvements will be.

AI holds the potential to revolutionize the creation and manufacturing of electronic products. Unlocking this potential, however, requires collaborative efforts to ensure its effective understanding and implementation. Without concerted action, the realization of AI's transformative promise in the electronics industry may remain elusive.

To address this challenge, the PCEA Technical Action Group (AI TG) convened a meeting of select representatives of early adopters and providers of AI tools for the electronics sector. The primary aim of this gathering is to solicit input from industry stakeholders to shape an AI Status and Action Plan.

This plan will serve as a roadmap, guiding the industry's efforts in leveraging AI across circuit board assembly, design, and fabrication processes. It will outline key initiatives, milestones, and strategies necessary for the successful integration and utilization of AI technologies.

We held our first task group meeting in April. The goals of the meeting were: first, to obtain consensus support for authoring a document to educate and to help facilitate acceptance and implementation of AI-assisted tools. And second, we wanted to start an outline of the document. Both goals were achieved.

The document, tentatively called a roadmap, will consider AI as it is applied to the electronics industry. It will review key problems and challenges, IP issues and case studies. It will offer use models, data management recommendations, and propose standards. And it will identify educational needs and guidelines.

Given the dynamic changes occurring, the AI task group's efforts will be structured as an ongoing and open effort intended to benefit the whole of the electronics industry.

The initial draft has been circulated among representatives from almost 25 companies. The focus is to develop a white paper detailing the status of the technology, the priorities, standards, obstacles to implementation, and timeline.

One of the obvious issues is that AI tools depend on a mode of crowd-sourcing in order to build and refine their models. Developers need users to share designs and data so that the models can learn from real-life situations. Many

companies, however, are reluctant to share that data, which in practice would be used to enable their competitors. One of the observations that came out of the discussion was that industries such as medical are way ahead of electronics when it comes to adopting open-source standards. Can the gaps be bridged in our space, or are they too large to overcome?

Under the guidance of Phil Marcoux, an advisor to AI companies and well known in the industry for his early adoption of future mainstream technologies such as SMT and multichip module packaging, the AI Task group plans to roll out the roadmap document this fall at PCB West.

Readers interested in participating on the task group may contact me at mike@pcea.net.

Speaking of [PCB West](#), those interested in AI might take a look at the [conference schedule](#). Among the talks scheduled are ones on Harnessing the Power of AI in PCB Design: Addressing Challenges and Unlocking Opportunities and AI and PCB Design: Where are We and Where are We Going? There also will be a special panel discussion on Oct. 9 as part of the free sessions.

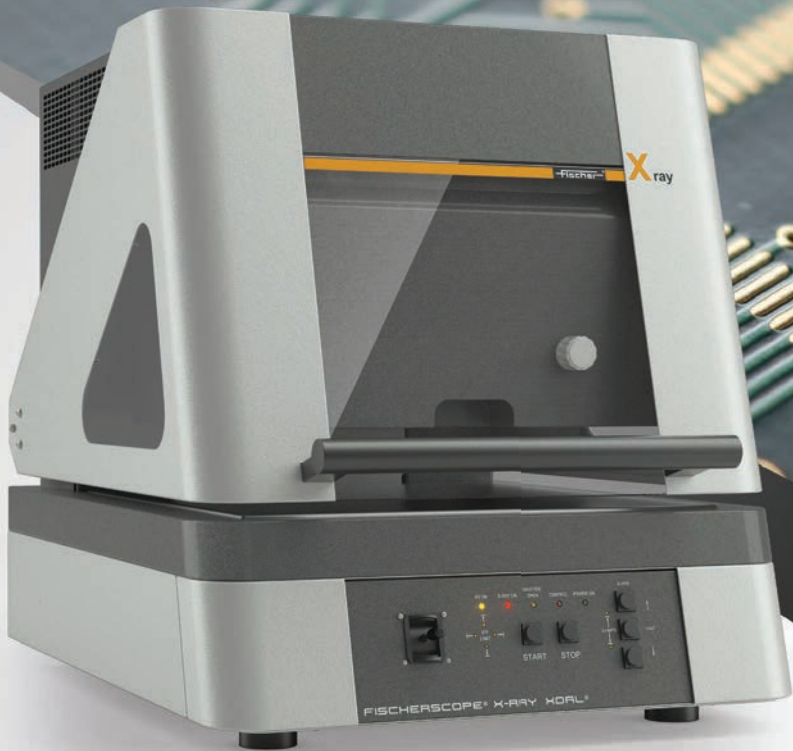
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NextFlex Launches \$5.3M Funding Opportunity for Hybrid Electronics

WASHINGTON – NextFlex, the Department of Defense-sponsored Manufacturing Innovation Institute focused on maturing hybrid electronics, released Project Call 9.0 (PC 9.0) in June, its latest call for proposals that seek to fund more than \$5 million in projects that further the development and adoption of hybrid electronics while addressing key challenges in advanced manufacturing.

The total PC 9.0 project value is expected to exceed \$11 million (including NextFlex investment and performer cost-share), bringing the total anticipated investment in advancing hybrid electronics since NextFlex's formation to \$143 million.

Building from the success of past Project Calls, PC 9.0 uses broadly defined topics to enable a diverse proposer base, with special emphasis on areas in which hybrid electronics can impact high priority U.S. manufacturing opportunities and areas of emerging importance within the electronics manufacturing community. PC 9.0 emphasizes projects that address critical hybrid electronics manufacturing challenges, enabling the transition of hybrid electronics devices into applications that require superior performance, assured reliability, and improved environmental sustainability.

“NextFlex Project Calls advance the state of the art of hybrid electronics technology and have proven to push the field in new directions, with each marking development milestones that have been collectively achieved by the NextFlex consortium. PC 9.0 continues this trend, with increased emphasis on projects that will lead to technology transitions into both commercial markets and defense programs.” said Dr. Scott Miller, director of technology at NextFlex. “As hybrid electronics technologies increasingly find their way into products and manufacturing, these developments will expand the range of applications in aerospace, automotive, structural health monitoring, and medical wearables.”

Proposals focused on manufacturing challenges and advancing technology transitions are sought in these topic areas:

Topic 9.1: Manufacturing of High Resolution, Multilayer Electronic Packages and Devices

Topic 9.2: Thermal Management for Power Electronics

Topic 9.3: Reliable Hybrid Electronics for Extreme Conditions

Topic 9.4: Conformal & Structurally Integrated Hybrid Electronics

Topic 9.5: Additive Processes for Improved Environmental Sustainability of Electronics Manufacturing

Topic 9.6: Open Topic for “New Project Leads”

In addition, NextFlex announced the release of its latest public Hybrid Electronics Technology Roadmaps. Developed by subject matter experts from industry, academia and government, the NextFlex Technical Working Groups in 11 technical areas of emphasis – Automotive; Device Integration & Packaging; Materials; Modeling & Design; Printed Components & Microfluidics; Standards, Test & Reliability; Asset Monitoring Systems; Flexible Power; Human Monitoring Systems; Integrated Antenna Arrays; and Soft Wearable Robotics – update the roadmaps each year.

The public roadmaps summarize the detailed information on the current state of the art, market opportunities and needs, key stakeholders, a five-year forward-looking development roadmap, and prioritized technical gaps identified by each Technical Working Group in the full-version roadmaps to which NextFlex members have access. These roadmaps inform the priorities and shape the topics for NextFlex Project Calls.

More information on NextFlex’s PC 9.0, including proposal submission instructions and the Proposer’s Day & Teaming webinar that was hosted on Jun. 10, can be found at nextflex.us/project-call-9-0. Proposals are due Jul. 24.



Report: EU Electronics Manufacturing to Continue Decline

BRUSSELS – Despite the adoption of the European Chips Act, the EU’s market share in critical electronics components beyond chips, including PCBs, EMS and advanced packaging, will decline to 15% by 2035, according to a new report.

The [Securing EU’s Electronics Ecosystem](#) report finds that the continent’s PCB industry segment has faced significant erosion over the last two decades, and revitalizing and growing electronics manufacturing – beyond chips – is essential to building a secure and robust European electronics ecosystem. A “silicon to systems” approach is necessary to support ongoing EU technological leadership and meet strategic goals.

“An innovative and resilient European electronics manufacturing industry is vital to ensuring the region’s access to defence and aerospace systems, medical technologies, and communications infrastructure. The growing strategic dependencies highlighted in the report are alarming as they undermine Europe’s ability to achieve key strategic priorities from a strengthening of the defense industrial base to the green and digital transitions,” said Sanjay Huprikar, president of Europe and South Asia operations, IPC, which released the report.

The report assesses how reliant Europe is on non-EU manufacturing across eight strategic sectors including aerospace/defense, automation, mobility, healthcare, and renewable energy. Highlights of the report include:

- Across the key sectors, EU electronics production is expected to lag behind global trends and decline from 16.5% global market share today to 15% by 2035.
- Those numbers become starker when looking at subsectors of the European electronics manufacturing industry, such as PCB production (1.7% global market share by 2035), advanced packaging (1.4%) and IC substrate production (0.7%) respectively.

- Europe's share of electronics manufacturing has fallen significantly in the last two decades despite demand for electronics soaring.
- Global PCB production has more than doubled since 2000 with European demand today at an estimated €7.87 billion (\$8.44 billion).
- Despite soaring demand for PCBs, European PCB production is projected to satisfy only 11% of European demand for PCBs (down from 17.5% today).

The study findings echo growing calls for strategic investments and comprehensive policies to enhance the EU's competitiveness including the European Council's conclusions in April stating that Europe "needs to reduce its strategic dependencies in sensitive sectors – energy, critical raw materials, semiconductors, health, digital, food and critical technologies – and in other sectors such as chemicals, biotechnology and space."

In response to the study, the European electronics manufacturing industry calls for an "Electronics Manufacturing Strategy" under the 2024-2029 European Commission mandate to help the EU better withstand global disruptions and maintain a competitive edge. An industry "Call-to-Action" shared in June includes support from leading European electronics manufacturers and Trade Associations raising awareness for this situation.

"Any new industrial policy supporting competitiveness needs to embrace electronics manufacturing as a key enabler for innovation and resiliency in strategically important sectors, like aerospace and defence. A dedicated strategy, including EU targets for electronics manufacturing, will help Europe compete with global competitors" said Alison James, IPC senior director, European government relations. 

Seacomp Opens Assembly Plant in Tijuana


CARLSBAD, CA – Seacomp in May opened a new 60,000 sq. ft. assembly facility in Tijuana, Mexico.

The new plant features 5,000 sq. ft. of space dedicated to PCB assembly, featuring solder paste printing and inspection, automated SMT placement, and reflow soldering.

"Manufacturing is a global industry, but it's also a hands-on business," said CEO Michael Szymanski. "That's why we've made the decision to bring most of our leadership team back together under one roof and introduce a new Seacomp facility just an hour away from our command center in Southern California."

Mexico's close proximity to other North American businesses promises an unmatched opportunity to diversify product supply chains, reduce costs and lead times, and provide increased possibilities for "hands-on" collaboration throughout the product development process, the company said.

Seacomp celebrated the factory's official launch on May 9, with a grand opening event that included a ribbon-cutting ceremony, facility tour, and networking opportunities for 115 partners, customers and global employees.

The new facility will create a total of 100 jobs in 2024, about a third being highly skilled roles in engineering and management, the company said. 

Tyri Begins In-House Circuit Board Production in Sweden

KUNGSBACKA, SWEDEN – Tyri, a manufacturer of lighting equipment for work machines, is starting in-house production of circuit boards in Sweden.


The company's 1,800 sq. m. facility will make Tyri self-sufficient in this area, giving it increased control, higher quality, and more reliable deliveries, the company said.

“We see many advantages in producing the circuit boards we need ourselves. Increased quality and delivery reliability are two of the most important reasons. We will produce for our production facility in Gothenburg and also for our production units in the UK and the USA,” said Jimmy Nordén, factory manager at Tyri Sweden.

Tyri said it plans to be self-sufficient in circuit boards for all the lamps produced in the group's three factories by 2025, which will reduce the impact of global uncertainties and ensure more secure deliveries to customers.

“We have many colleagues in the producing industry who have their circuit board production in southwest Sweden. A cluster of knowledge and experience has been built up here, and we want to contribute with our knowledge to make the region even stronger in this area,” said circuit board production manager Per-Johan Edgren.

The company said digitalization is the focus for the future, and the 30 m. line is prepared from the start for continued digitalization.

“To achieve profitability in in-house circuit board production, a high degree of digitalization is required,” said Edgren. “We have done our homework, we are using the technology available today, and have prepared ourselves for future continued digitalization. Much of it is about improving productivity with high quality. That was the condition for making this investment, and it seems we have succeeded.” 

Apple Among New Members of IPC-2581 Consortium

WESTBOROUGH, MA – Apple, Beta CAE and Panasonic Connect were welcomed as the newest members of the IPC-2581 Consortium during the group's May meeting.

“We would like to support IPC-2581 as a standardized format to enable better communication between, for example, fab and assembly vendors,” Apple said in a statement.

During the meeting, members also discussed the use of a coin shape as an interesting application in a CAD system for PCB design, as well as a new via type to handle the application and how it would be defined in the CAD system. Other topics of discussion included the need for improved communication of materials and stack-up definitions to

manufacturers – including composite and roll-up materials, the need to define and name dielectric layers in the stack up, particularly for trench vias, and the inclusion of span information for these layers.


The IPC-2581 Consortium is a group of PCB design and supply chain companies whose collective goal is to enable, facilitate and drive the use of IPC-2581 – a generic standard for printed circuit board and assembly manufacturing description data and transfer methodology – in the industry. 

Doosan Named CCL Supplier for Nvidia AI Chips

SEOUL – Doosan Electro-Materials is anticipating a boost in copper-clad laminate sales after being selected as CCL supplier for Nvidia’s AI chip substrates, according to reports.

Doosan, the world’s largest CCL manufacturer, recently began mass production for Nvidia’s next-generation GPU B100, which is scheduled to be released in the fourth quarter.

Doosan’s first-quarter sales were 186.5 billion won (\$135 million), and are projected to reach 900 billion won this year.


The global CCL market is set to grow at a compound annual rate of 6%, from \$15.08 billion in 2022 to \$21.2 billion by 2028, according to market research firm Global Information. The CCL market for AI chips is expected to reach \$10 billion in 2025. 

Flex Acquires FreeFlow B2B Platform

AUSTIN, TX – Flex has acquired FreeFlow, a company that specializes in global secondary markets and circular economy tracking and reporting.

FreeFlow’s B2B digital marketplace platform enables customers to sell surplus and returned inventory while protecting primary sales channels. Flex said the addition adds services for customers across multiple markets, including data center, enterprise, and lifestyle, to create additional revenue streams and accelerate sustainability through second life products.

“The acquisition of FreeFlow reaffirms Flex’s commitment to deliver the highest value to our customers, addressing their evolving business and sustainability needs across the product lifecycle while increasing our addressable market,” said Michael Hartung, president of Agility Solutions at Flex. “This addition further differentiates our end-to-end services and will enable a wide range of customers, from cloud to lifestyle, to realize the benefits of second life products, and ultimately deliver on their environmental commitments.”

Flex said it plans to expand FreeFlow and digital circular economy tracking and reporting capabilities into additional industry segments and major regions to help new and existing customers securely access secondary markets and drive faster adoption of sustainable solutions. 

ASMPT Reorganizes American SMT Business

MUNICH – ASMPT has reorganized its SMT Solutions segment in the Americas (USA, Canada, Mexico and Brazil), adding a new division between the North and South America regions.


The division of the business, which was previously managed centrally from Suwanee, GA, will allow the company to adjust its market focus to better meet the specific needs and requirements of the different markets, ASMPT said in a release.

The company said the markets in Mexico and Brazil differ from those in the US and Canada, with mainstream solutions for the high-volume production of consumer goods, computers and automotive electronics being the main drivers in Mexico and Brazil, while the Canadian and US markets focus on innovative and customer-specific advanced packaging solutions for high-mix production and on the development of special products for medical technology, the aerospace and defense industries, as well as industrial electronics.

“Serving these different market requirements required an operational separation of the Americas organization, which had previously been centrally coordinated from Suwanee, GA,” said Josef Ernst, CEO of ASMPT SMT Solutions. “Splitting the areas of responsibility allows ASMPT to focus on the specific needs of the markets in North and South America in a more targeted manner.”

Ramon Hernandez is responsible for Mexico and Brazil, and Alexander Hagenfeldt is in charge of the US and Canada. Backoffice and support operations in the Americas will remain largely unchanged under the leadership of the previous managers, the company said.

Hernandez has 23 years of experience in various positions in the electronics industry. He has been general manager for Mexico for ASMPT.

Hagenfeldt has been with ASMPT for 13 years, holding roles in marketing and service. 


Keytronic Confirms Data Breach After Ransomware Attack

SPOKANE VALLEY, WA – Keytronic in June began notifying potentially affected parties and regulatory agencies of a breach that saw more than 500GB of personal data stolen.

The EMS company reported the cyberattack in an SEC filing in May, saying that the attack disrupted its operations by limiting access to business applications essential for corporate activities, and its domestic and Mexico operations were shut down for two weeks to address the incident.

Keytronic has resumed normal operations, but an investigation found that personal information had been stolen during the attack, the company said.

“Since the date of the original report, the company has determined that the threat actor accessed and exfiltrated limited data from the company’s environment, which includes some personally identifiable information,” Keytronic’s SEC filing said.

The company also said the production loss caused by the attack could impact its financial condition for the fourth quarter, which ended Jun. 29, and it incurred around \$600,000 in expenses for external cybersecurity experts, with more costs anticipated. 

PCD&F

Amber Enterprises reportedly plans to invest ₹2,000 crore (\$239 million) to set up a PCB manufacturing facility in India.


Bittele Electronics completed an expansion and installed improvements at its Markham, ON, PCB manufacturing facility.

BPL set up a new manufacturing unit for printed circuit boards in Bengaluru, India.

Eton Electronics will invest no more than \$100 million into a new PCB production base in Thailand.

Jianding will invest \$250 million to build a second PCB manufacturing facility in Vietnam.

Shenzhen Derongji Circuit Board Co. and **Guigang Hongxin Electronic Circuit Board Co.** have committed CNY156 million (\$21.5 million) to build PCB production facilities in Taiwan's Gangbei District.

Ucamco announced that a global leader implemented its Jayda PCB quoting software in its new web shop. 

CA

Aaloktronix announced the availability of PCB assembly services tailored for the aerospace industry.

AIM Solder joined the International Electronics Manufacturing Initiative (iNEMI) and announced a distribution partnership with **EIS** in Mexico.

Altus will distribute **PVA's** Delta 6 robotic conformal coating/dispensing system in the UK and Ireland.

BAE Systems won a \$95 million contract to supply advanced electronic warfare (EW) pods for the US Navy's P-8A aircraft.

Beifu Electronic installed **Eurolacer's** Atom range of pick-and place machines.

Bentec appointed **SMTVYS Technology** manufacturers' representative for its Prey UPI in Mexico.

CE3S will distribute **SCS's** ESD process control products.

Circuitronics installed a **Sasinno Americas** Ant-i2 selective soldering machine.

Dixon Technologies India has lined up ₹1500-1800 crore (\$179.5 million to \$215.4 million) in investments over the next three years to expand production capacity and component manufacturing in the country.

Flex is investing €90 million (\$96 million) to manufacture high-tech electric and hybrid vehicle components at its two sites in Zalaegerszeg, Hungary.

Foxconn is partnering with **Nvidia** to develop generative AI software for electric vehicles.

Heraeus Electronics successfully defended a European patent encompassing the use of specific metal sintering preparations, as well as the metal sintering preparations themselves.

India is reportedly planning a new production-linked incentives (PLI) scheme for electronic components.

Intel is reportedly halting plans for a \$25 billion factory in Israel.

Malaysia is targeting at least 500 billion ringgit (\$107 billion) in investment for its semiconductor industry as the country looks to position itself as a global manufacturing hub.

Meta System will use **Critical Manufacturing's** MES in its new electronics facility for e-mobility production.

Michigan will invest \$10 million in a public-private initiative that aims to develop a talent pipeline to accelerate semiconductor applications in the mobility sector.

Micron Technology willfully infringed a pair of **Netlist** computer memory patents and owes \$445 million in damages, a Texas federal jury determined.

Nidec announced a collaboration agreement to manufacture probe cards and probe card parts for **Synergie Cad**.

Nokia partnered with **Foxconn** to make 5G devices in northern Vietnam.

Odyssey Electronics purchased a **Mirtec** MV-6 AOI machine.

Padget, a subsidiary of **Dixon Technologies**, will reportedly make **Google's** Pixel 8 smartphones starting in September following a deal signed with **Compal**.

Semi-Kinetics purchased a Decan S SMD placer from **Hanwha Techwin Automation Americas**.

SolarEdge Technologies selected **Cogiscan** to digitize its manufacturing operations.


STMicroelectronics is planning a new chip manufacturing plant in Italy with an investment of around €5 billion (\$5.42 billion) that will come with some state support.

Tagarno relocated its US headquarters from Atlanta, GA, to Tampa, FL.

Tata Group is reportedly engaging in serious negotiations with Chinese smartphone supplier **Vivo** for a controlling share in its India operations.

Tesla is reportedly “aggressively” pushing its suppliers to start making key components outside of China and Taiwan.

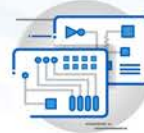
Wistron is set to invest \$45 million more in its factory in Vietnam’s northern province of Ha Nam, raising the total investment to \$363.9 million.

Zollner Elektronik selected **Luminovo** as a core partner for its digitalization strategy. 

Support For Flex, Rigid Flex and Embedded Component Designs Now Available.



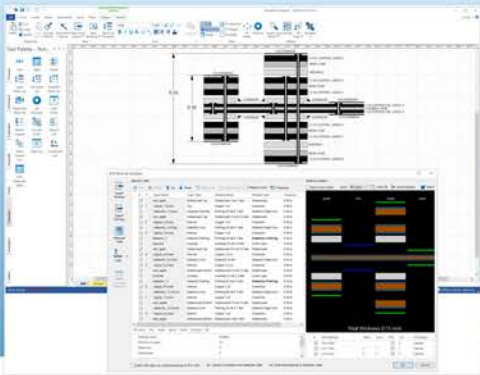
BluePrint-PCB



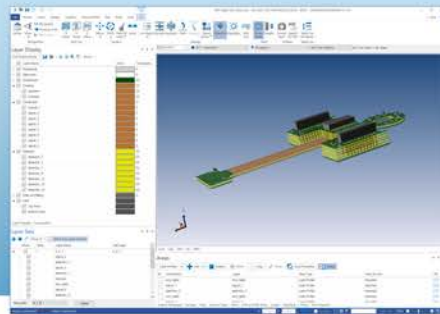
CAM350

DownStream's CAM350 and BluePrint-PCB support importation and visualization of PCB designs containing Flex, Rigid Flex or Embedded components. Visualize designs in both 2D and 3D, and easily document complex Flex or Rigid-Flex Stack-Ups for submission to PCB Fabricators.

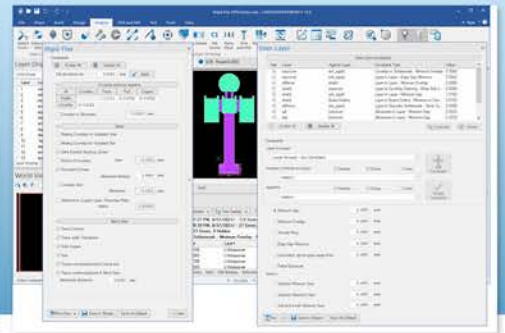
- Import and Visualize Flex, Rigid-Flex and Embedded Component Designs
- 3D Visualization to Validate PCB Construction and Component Assembly
- Manage Variable Stackup Zones for Rigid-Flex Designs
- Easily Create Custom Flex or Rigid-Flex Fabrication and Assembly Documentation
- Use DFM analysis to analyze a flex or rigid-flex design for potential fabrication or bend related defects



Use Stack Up Visualizer and BluePrint's Rigid-Flex Stackup template to easily manage and document rigid-flex stackups.



A rigid-flex design in 3D. Shown with layers spread out to improve visualization of the layer stackup.



Use Rigid-Flex and Inter-layer DFM analysis to analyze flex and rigid-flex designs.



For more information visit downstreamtech.com or call (508) 970-0670

PCD&F



Shane Whiteside



Travis Kelly



Bryan Fish




Vishnu Gangaswamy Venkatesh

PCBAA named Summit Interconnect CEO **Shane Whiteside** chairman following the end of **Travis Kelly's** term.

Garmin promoted **Aaron Parker** to technical lead PCB designer.

HT Global Circuits hired **Bryan Fish** as regional sales manager.

Sanmina named **Vishnu Gangaswamy Venkatesh** to succeed senior VP **Brent Billinger**, who is set to retire in January.

TE Connectivity named **Ted Shpak** global senior director of quality assurance. 

CA



Chris Matthews



Mhanny Aguillo



Richard Timms



David Suh



Bob Doetzer



Tim Glasgow



Werner Wagner



Jayson Moy



Rajesh Sethi



Todd Kelsey



David Lane



Jeff Bullock



Michael Sedgwick

AIM Solder promoted **Chris Matthews** to business development manager for the Americas and appointed **Mhanny Aguillo** Southeast Asia technical sales manager.

Eurolacer appointed **Richard Timms** international channel manager.

Hanwha Techwin Automation Americas appointed **David Suh** application engineer.

Heller Industries named **Bob Doetzer** sales representative for North and South Carolina and **Tim Glasgow** sales representative in Georgia, Tennessee, Alabama and Mississippi.

Indium Advanced Materials appointed **Werner Wagner** general manager.

Kyzen named **Jayson Moy** product line director.

Lava International appointed **Rajesh Sethi** CFO.

Plexus named **Todd Kelsey** president to replace **Steven Frisch**, who is retiring on Sept. 28.

Summit Interconnect named **David Lane** general manager and vice president, Advanced Assembly.

Syrma SGS Technology named **Jeff Bullock** vice president of business development.

Sypris Solutions appointed **Michael Sedgwick** vice president and general manager of Sypris Electronics.

USPAE named **James Will** executive director. 

PCB East 2024 Registration Up 18% YoY

PEACHTREE CITY, GA – Registration for the PCB East 2024 conference and exhibits rose 18% overall year-over-year, the Printed Circuit Engineering Association announced in June. Conference registration was up 12% from last year, while the expo-only trade show registration rose 9% over the same period.

The exhibition was held June 5 at the Boxboro Regency Hotel and Conference Center in Boxborough, MA. In all, more than 65 leading suppliers of electronics design tools, manufacturers of bare boards and assemblies, suppliers of fabrication and assembly equipment and materials, and related industry companies exhibited at the show.




“PCB East continued its growth this year as the region becomes more aware of the opportunities for education and networking,” said Mike Buetow, conference director and president, PCEA. “Our post-show surveys indicate 100% of respondents would either likely or definitely recommend the conference to a colleague.”

“Attendees represented 35 states and 42 countries,” Buetow added, “a recognition of the timeliness and scope of the event.”

“Another great show at PCB East!” said Lauren Waslick, director of PCB design, Newgrange Design. “I gave my first professional talk and met a lot of great people. Thanks to the Printed Circuit Engineering Association for putting on a great event!”

“It’s always great to sync up with my dear friends, as well as many industry colleagues old and new at PCB East,” said Stephen Chavez, senior product marketing manager, Siemens Digital Industries and chairman of PCEA. “A big shout-out to the entire PCEA staff for putting on another great industry event! I can’t wait to attend PCB West later this year! I hope to see you there!”

PCB East 2025 will be held at the Boxboro Regency Hotel and Conference Center in Boxborough, MA, from April 29 to May 2 with a one-day exhibition on April 30. 

2025-26 Board of Directors Slate Announced


PEACHTREE CITY, GA – The PCEA Nominations Task Group has chosen three new members to join the board of directors for the upcoming term.

The board in June also voted for Matt Leary and Jim Barnes to join the board, effective immediately, to fill two open positions.

[Barnes](#) is corporate senior vice president, strategic global sourcing, at Generac Power Systems, a leading energy technology company. He is an expert in strategic planning, outsourcing, and manufacturing operations, having held a variety of management roles at multinational EMS SigmaTron prior to joining Generac in 2022.

[Leary](#) is president of Newgrange Design, a Boston-area design service bureau he founded in 1996. He has lengthy experience in printed circuit design, executive management and sales and business development.

Ballots for the 2025-26 board will include the following individuals: Jim Barnes, Stephen Chavez, Tomas Chester, Doug Dixon, Justin Fleming, Rick Hartley, Matt Leary, Charlene McCauley, Scott McCurdy, Anaya Vardya, Susy Webb and Eriko Yamato.

Ballots will be circulated in July, per PCEA bylaws requiring voting to begin a minimum 60 days prior to the annual meeting, which is scheduled for Oct. 8 at [PCB West](#) in Santa Clara, CA. 

PCB East Seeks Abstracts for 2025 Conference

PEACHTREE CITY, GA – The PCEA Conferences Task Group seeks abstracts for next year’s PCB East technical conference.


The conference will focus on training and best practices for printed circuit board design engineers, electronics design engineers, fabricators and assemblers.

The four-day technical conference will take place April 29 to May 2, 2025, in Boxborough, MA. The event includes a one-day exhibition on April 30.

Papers and presentations of the following durations are sought for the technical conference: one-hour lectures and presentations; two-hour workshops; and half-day (3.5-hour) and full-day seminars.

Preference is given to presentations of two hours in length or more, and no presentations of less than one hour will be considered.

Abstracts of 100-500 words and speaker biographies must be submitted to PCEA. Papers and presentations must be noncommercial in nature and should focus on technology, techniques or methodologies related to printed circuit board design, fabrication, assembly, test, components or packaging, and additive manufacturing.

Abstracts due are due Sept. 6 and must be [submitted online here](#). No emailed abstracts will be accepted. Speakers will be notified in November and presentations are due April 11. 

PCEA CURRENT EVENTS

CHAPTER NEWS

General. The annual PCD&F salary survey of printed circuit board designers, design engineers and other layout specialists is open and may be taken

at: <https://www.surveymonkey.com/r/2024pcdfdesignerssalary>. PCD&F publishes the aggregate data in a free downloadable report on its website and in the magazine. Individual responses are not shared.

To find the latest on chapter events, visit <https://pcea.net/events>.

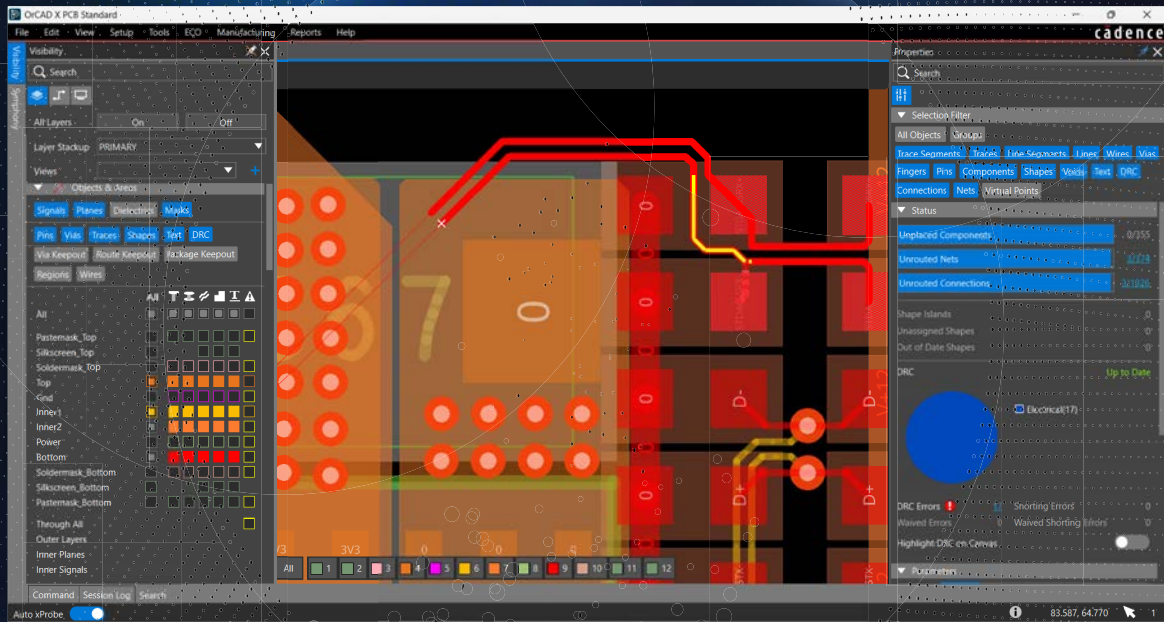
Boston. We are planning to hold our next meeting in July via Zoom. The chapter has launched a LinkedIn page at [PCEA-Printed Circuit Engineering Association – New England Chapter](#).

Portland. Our June meeting featured a talk on IPC-2581 vs. Gerber and AI in PCB design. We meet monthly, usually by Zoom. Contact Stephan Schmidt at stschmidt@pcea.net for an MS Teams invitation.

San Diego. In June we featured a presentation on IPC J-STD-001 Compliant Solder Pattern Calculations for DfA as part of a joint meeting with SMTA. 

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India EMS Market Set to Soar

PARIS – India’s domestic electronics manufacturing services revenues are on track to more than double over the next three years, reaching \$55 billion by 2027.

That’s according to a report by BNP Paribas, which forecasts investments led by companies such as Apple and Samsung will add significant heft to the nation’s EMS industry.

Apple, the bank’s report says, will increase investment to \$40 billion over the next four to five years to boost domestic production capacity of laptops as well as smartphones. Lenovo intends to build servers in support of its growing data center business, while Acer, HP and Nokia are also expected to expand domestic operations.

BNP forecasts the total addressable domestic EMS market will grow at a 27% compound annual growth rate to \$100 billion by 2027 from \$40 billion in 2023. Local customers’ appetite for consumer products and white goods, increased domestic component production, and government incentives to build the Indian manufacturing capacity will all contribute, BNP said.

Computer Crush				
Trends in the US electronics equipment market (shipments only)				
	FEB.	% CHANGE		YTD
		MAR. [†]	APR. [‡]	
Computers and electronics products	0.1	-0.2	0.2	1.8
Computers	2.8	-0.1	3.9	25.6
Storage devices	1.6	-5.1	2.9	10.7
Other peripheral equipment	6.3	-5.8	7.0	5.2
Nondefense communications equipment	0.7	0.6	0.6	0.2
Defense communications equipment	-2.5	3.6	2.0	-2.6
A/V equipment	-0.8	1.6	-0.8	32.0
Components ¹	-0.4	-1.1	0.5	7.0
Nondefense search and navigation equipment	-1.6	2.3	2.2	2.5
Defense search and navigation equipment	-0.3	0.6	0.2	6.5
Electromedical, measurement and control	-0.9	0.2	-0.1	-0.4

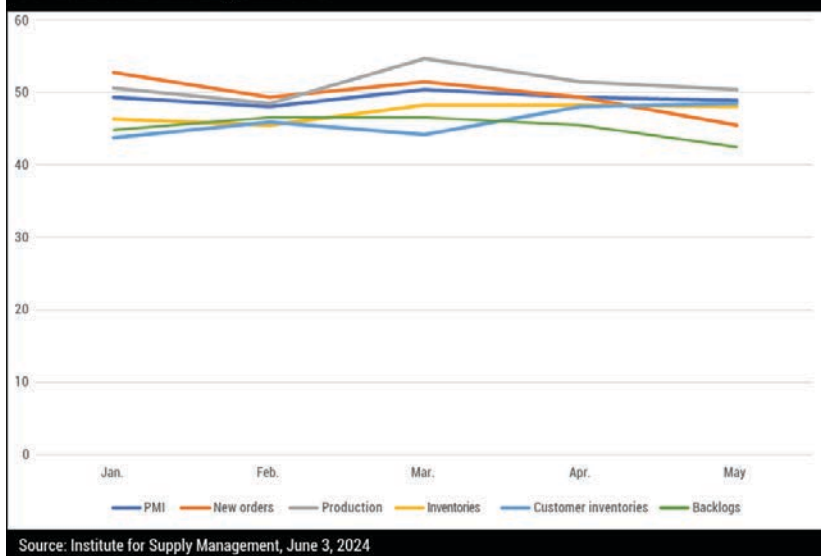
[†]Revised. [‡]Preliminary. ¹Includes semiconductors. Seasonally adjusted.
 Source: US Department of Commerce Census Bureau, June 4, 2024

Key Components

	JAN.	FEB.	MAR.	APR.	MAY
EMS book-to-bill ^{1,3}	1.15	1.22	1.31	1.42	1.36
Semiconductors ^{2,3}	15.2%	16.3%	15.2%	15.8%	TBA
PCB book-to-bill ^{1,3}	0.93	1.07	1.13	1.06	0.95
Component sales sentiment ⁴	98.0%	100.8%	106.9%	124.1%	112.3%

Sources: ¹IPC (N. America), ²SIA, ³3-month moving average, ⁴ECIA

US Manufacturing Indices



Hot Takes

First quarter **smartphone production** grew 18.7% year-over-year to 296 million units shipped, but remained below pre-pandemic levels of over 300 million units. (TrendForce)

Semiconductor exports from China rose at a faster pace in the first five months of the year. (China government)

The expansion of **semiconductor fab capacity** in 2024 is expected to be 4% as manufacturers let capacity utilization rates recover from the low levels experienced in 2023. (Knometa Research)

Global shipments of **augmented reality and virtual reality (AR/VR) headsets** declined 67% year-over-year in the first quarter. (IDC)

Global **semiconductor sales** were \$46.4 billion in April, up 15.8% from 2023. (SIA)


DRAM sales rose 5.1% sequentially in the first quarter to \$18.4 billion, driven by rising contract prices for mainstream products. (TrendForce)

Global **semiconductor equipment** billings contracted 2% year-over-year to \$26.4 billion in the first quarter. (SEMI)

China's electronics manufacturing sector grew by 13.6% year-on-year, outpacing both the general industrial sector and the high-tech manufacturing industry. (IBS Electronics)

Worldwide **smartphone shipments** are forecast to grow 4% year-over-year in 2024 to 1.21 billion units. (IDC)

India's electronics manufacturing industry is urging the government for a ₹30,000-₹35,000 crore (\$3.6 billion to \$4.2 billion) production-linked incentive scheme for components and sub-assemblies.

Orders of **manufacturing technology** reached \$318 million in April, down 26% from March and down 5.4% from April 2023. (Association for Manufacturing Technology) 

PCBWay

PCB Prototype the Easy Way

PCBWay assists electronic enthusiasts and companies in overcoming these challenges through its specialized offerings in PCB prototyping and assembly. Whether it's small-volume or large production, the company delivers its expert PCB services, all under one roof. As one of the most experienced PCB manufacturers and SMT Assemblers in China, PCBWay prides itself as the best business partner in every aspect of your PCB needs.



PCB PROTOTYPE AND FABRICATION

Up to 14-layer PCB
Standard PCB, HDI PCB, Alumium PCB, flex and Rigid-flex PCB

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PCB ASSEMBLY

Start from **only 30 USD**
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Is Private Equity Investing in Your EMS?

Getting a grip on the many moving parts.

MUCH OF MY time this decade has been spent supporting private equity (PE) firms considering an investment in the EMS space, with no prior EMS experience on their staff. Those of us who have spent years in this space know there are vast amounts of “moving parts” involved with running a solid EMS business.

I’ve been told that my audits and SWOT writeups proved to be very valuable, provided accurate insight into a business the potential investors knew very little about and reduced previously unknown risks that would have crept into the deals.

Many similarities exist among the audits I’ve conducted over the past few years. Many of these findings would not surprise EMS industry veterans. But these situations may not be self-evident to an investor who hasn’t previously worked in this complex service industry. I have also seen many of these elements of risk at my direct EMS clients managed to different degrees of efficiency.

Some questions/topics to consider before making any investment decision include:

- Aging capital equipment. SMT lines and supporting capex expenditures like AOI and x-ray equipment are very expensive and with the increasing costs of doing business, many capital expense budgets have been reduced, so unexpected short-term expenses could be looming for a new investor.
- Identifying where the products (PCBA/box-builds) fall on the technology scale. Most EMS companies market their company as a “leading-edge” or “high-technology” manufacturer. The reality is many offer low- to medium-technology and therefore are a less “sticky” business, making it easier for customers to move programs to an EMS competitor. I don’t believe companies are intentionally deceptive in stating they build leading-edge electronics. Rather, I have found they just don’t realize the degree of complexity some EMS business models are operating in. (You don’t know what you don’t know.)
- Determining if the top leadership is selling with a goal to punch-out. If so, you must assess the current staff, or have competent replacement leadership on the outside ready to take over the business for the investors. Even with some level of earnout, many leaders are not giving 100% as they did prior to the sale closing. This is a critical factor in the final valuations of the deal.
- Were the 2021 and 2022 topline revenue figures due to the EMS simply requiring longer visibility on POs so they could drive long-lead components, or were new customers, new programs, higher-level assemblies, and/or market share gains being won part of that revenue growth? Time was, our industry was happy with six

months of firm bookings. That extended to 18 to 24 months during the pandemic due to component lead-time extensions. Those are now returning to historically normal schedules. If topline growth was based solely on POs being booked out longer, it's reasonable for topline revenues to shrink when that trend eases.


- What were historical inventory turns pre-2022? How are lower inventory turns being managed to abate the EMS risks and conserve cash? What is being done to mitigate the cost of stagnant inventory waiting for the “golden screw” to arrive and having lost any asset value for their revolver and borrowing limits?
- Are the sales and marketing functions driving growth, increasing brand awareness, differentiating from their competition, aggressively growing new customers, aggressively growing new sales partners (direct and indirect), and what support is being given to the business office to gain share at their existing customers? Does the business office know what their market share is and who has the balance of obtainable business at the existing accounts? Are the sales folks and business office simply order-takers? Is the sales tool kit robust and enabling the closure of new deals?
- Are too few, or too many, KPIs being tracked and managed and are the critical ones in the mix? I've heard “we measure everything,” and because of that lack of focus, seen how no KPI is more important than any other KPI, with no real focus on the critical few. Does the EMS realize it can't run a company just from its dashboards?
- How does the market mix and customer concentration look? Some markets are counter-cyclical to others, so some diversity is usually less risky than a non-diverse mix. Many EMS companies also suffer from having a giant revenue client that could crater the business if they leave or have a terrible year. Ideally, I like to see no client larger than 12% to 15% of the total revenue, with a few other customers close to that percentage, across a few targeted markets.
- Are the software systems robust enough to scale the business and handle an increasing complexity of daily activities?
- Is problem-solving all “firefighting” or is there evidence of “fire prevention” at work? It could be continuous improvement programs/Kaizen events, floor employee suggestions being acted on and celebrated, Lean manufacturing events, a value-stream mapping “war room,” and various other visible activities or cases the EMS can demonstrate.
- Are there frequent top-down communications with employees about the state of the business, opportunities, upcoming audits, benefits, and relevant topics? Does executive management walk the plant with some frequency, getting personally involved with the employees? Is there a culture supportive of what [Abraham Maslow](#) described as “belongingness?”
- Is there evidence all executive staff are involved in cultivating “customers for life,” and is the EMS committed to delighting their clients? (I have been to places where the customer is denigrated and looked at as a necessary evil.)
- Does the EMS live by a principle that taking equal care of all four elements of any business is a must? Those elements are: customers, employees, vendors and, of course, shareholders.
- Does the QMS (Quality Management System) and subsequent quality certifications support the stated targeted markets the EMS is trying to grow? For instance, if the facility is not ITAR and with the AS9100 certification,

can you really claim a focus on the A&D market?

- Are the manufacturing floor processes institutionalized so consistency of process exists or is each day more of a brute force attempt to make committed shipments?
- How robust is the new product introduction (NPI) process? Is NPI a new adventure with every new SKU launched and is each NPI leader doing it differently, or is a repeatable process following the same steps for the first new product launch as it is for the fiftieth?
- Are the standard terms and conditions fair to the customers while still protecting the EMS from issues that could damage the business but are out of its control? Has the EMS executed egregious OEM contracts accepting unfair terms it can't control? Speaking of legal documents, if manufacturer reps are part of the sales team, are those contracts fair to the reps or are they so one-sided the EMS can't recruit good rep firms?
- How good is the materials team and business office at managing excess and obsolete inventory? Are there clearly stated executed agreements in place documenting when the possession of slow-moving or obsolete inventory becomes the OEM's responsibility? Are there software systems in place to manage these events?
- Has the EMS negotiated favorable terms from its vendors and is it meeting its end of the deal, such as on-time payment?
- Is the quote model capturing all applicable recurring and non-recurring costs and maximizing opportunities? Is it refined so that mid-level management can plug and play or does a senior executive have to administer all variable costs?
- How are scrap rates, internal captures, and external escapes (RMAs) measured? Are internal bone piles growing or are they managed well and in a timely fashion?
- Is the EMS trying to serve too many customers, stealing resources from its actual growth/strategic accounts?
- Does the EMS really understand who its best clients are? Can it define the cream of the crop besides just using total spend?
- Is there a universal understanding of what a "good fit" customer looks like or does the EMS simply require a pulse from a new prospect to engage?
- Is a system in place to act as an early warning system (canary in the mine) so the EMS can take action to repair growing dissatisfaction at existing customers, before it becomes a lost cause?
- Is digital marketing keeping pace with current trends?

These are just some of the deep-dive topics a PE firm should consider when performing diligence on a potential EMS investment. Even something as simple as auditing the MRB cage should not be overlooked: Often it contains too much idle cash with slow-dispositioned defective raw materials or is a catchall storage location for items that should be stored elsewhere. Safety, housekeeping, and many hours' worth of Q/A often uncover not only risks but areas an EMS excels in, and I just summarized a few.

I encourage any investor group thinking of investing in the EMS space to reach out and discuss ways to mitigate their risk with the details obtained through a preaudit survey, an on-site audit, and a thoroughly documented SWOT

analysis. 

JAKE KULP is founder of JHK Technical Solutions, where he assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc. He can be reached at jkulp@cox.net.



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PCB Tariffs are All the Rage. They Aren't the Answer.

Supply chains are stronger when spurred by private investment.

BOTH THE TRUMP and Biden administrations have taken measures aimed at bringing manufacturing back to the US. But realistically, when will that happen?

And how much longer will we ask domestic PCB buyers who must rely on Asia for product to pay a tax for boards they cannot get made in a reasonable amount of time in the US?

In late May the [US trade representative announced one more year of reprieve](#) from the 25% tariff for two- and four-layer rigid printed circuit boards.

While two- and four-layer boards represent only a narrow portion of the PCBs manufactured in China, an exemption continuance is good news and will provide some relief to many OEMs and EMS companies struggling with supply chain challenges.

India is jumping on the tariff bandwagon as well. Its [Central Board of Indirect Taxes and Customs \(CBIC\) recently imposed a five-year, 30% "anti-dumping duty"](#) on bare PCBs manufactured in China and Hong Kong. The measure is billed as a way to ensure fair trade and provide a level playing field for the country's domestic board industry.

Boards made in China may qualify for a number of exemptions to the tariff, however, especially when it comes to high-tech boards. The exemptions lay bare the challenges India faces when it comes to technology and volume production.

The truth is, even with the new tariff, India will need to continue buying higher-tech PCBs manufactured outside its own borders. And China will continue to be a major supplier.

Meanwhile, European officials are expected to soon impose their own tariffs on PCBs made in China. It will be interesting to see how the issue of exemptions will be handled.

In addition to supply chain concerns, the drive for green energy coupled with the government-imposed need to have it *now* is driving up material costs.

President Biden said in May that he would impose tariffs of up to 100% on imports of Chinese green technologies, including electric vehicles. This targeted escalation has raised import barriers for clean-energy products manufactured in China. This means the measures will slow progress and come at a higher cost for meeting those very clean energy goals set by his administration.

Does this mean national pride comes before a greener planet?

With all the supply chain issues of higher material costs and freight surcharges that domestic EMS companies and OEMs currently face, adding government-imposed inflation of PCB pricing hurts the overall domestic market.

History has shown that tariffs tend to increase domestic prices and raise costs to businesses and consumers. It is a double-edged sword that usually ends up cutting the wrong way.

Protectionist strategies won't solve the problems we face, and tariffs are essentially a punitive measure that interferes with PCB buyers' decisions about what is best for their operations and their customers.

Yes, it is important to have strong domestic manufacturing. But at what cost?

Instead of punishing the consumer, why don't we incentivize businesses to receive private investment? Instead of those punishing tariffs, how about the government offer a three- to five-year tax holiday to those that invest in domestic manufacturing?

Private investment could be ramped up quickly, and monies invested would be more likely to be well spent, as investors would hold manufacturers accountable and help ensure more efficient operations.

Additionally, the government could support *more* workforce development programs tailored to the needs of the manufacturing sector. Government investment is needed to help bridge the skills gap and ensure a steady pipeline of qualified workers, which is essential for the sustainability and growth of domestic manufacturing.

By investing in education and training, the government can help create a robust workforce that is capable of meeting the demands of modern manufacturing industries.

Also, better infrastructure can enhance supply chain efficiency. Upgrading transportation networks, ports and logistics systems would reduce bottlenecks and improve the movement of goods. This not only benefits domestic manufacturers but also makes the entire supply chain more resilient to disruptions.

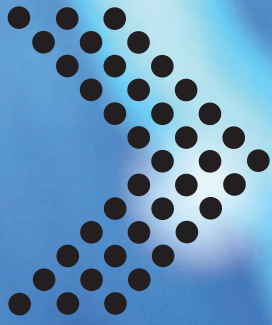
And how about cutting unnecessary red tape? Simplifying the regulatory framework and ensuring it is conducive to business growth can attract more companies to set up manufacturing operations domestically.

Finally, establishing strategic partnerships and trade agreements with other countries can help diversify the supply chain and reduce reliance on any single source. By collaborating with allies and fostering international cooperation, the supply chain can become more robust and less susceptible to geopolitical tensions.

Instead of resorting to punitive tariffs that increase costs, why not try a combination of private investment incentives with infrastructure improvements, workforce development, red tape cutting, and international collaboration?

That's how I believe we can build a stronger, more resilient domestic manufacturing sector. These strategies would not only help alleviate current supply chain challenges but also position the PCB industry for sustainable growth in the future. 🚀

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.



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Hybrid Bonding and Thermal Concerns Heat Up Denver Discussions

IEEE's annual conference of academic and research leaders reveals equipment and process advances.

THE HEAT WAVE covering much of the Rocky Mountains in June was an apt metaphor for the annual IEEE Electronics Components and Technology Conference (ECTC) in Denver, where some 2,000 attendees heard the latest developments in advanced packaging. Thermal issues were as much a part of the proceedings indoors as out.

The conference in the Mile High City opened with a Heterogeneous Integration Roadmap (HIR) session. Presentations addressed the thermal challenges and specifically called out the needs for developments in metrology focused on thermal measurement. The conversation carried over into a parallel special session on metrology where participants from NIST, ASE, Intel, TSMC and KLA discussed challenges and opportunities in advancing metrology for next-generation microelectronics. The discussion culminated with a call to action to incorporate metrology challenges in every aspect of the HIR moving forward and potential for a future NIST workshop.

Thermal challenges continued to be a hot topic with the special session on efficient and innovative thermal management for power-hungry AI/ML applications featuring presentations from key players. Many papers highlighted thermal challenges and some solutions were discussed. TSMC presented its development of an energy-efficient Si-integrated micro-cooler for high power computing. The Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems co-located its ITherm conference in the same venue, where a keynote from Nvidia discussed how generative AI and accelerated compute are creating the next-generation liquid-cooled data centers with a focus on challenges, opportunities and the road ahead. Thermal management was a key topic in AMD's presentation on next-generation AI architectures. Analytics for thermal management of data centers was highlighted by Segunte, UC Irvine discussed fundamentals of machine learning for phase change heat transfer, and NXP provided additional observations on the role of AI in thermal management. IBM Research provided insight on how AI can be used to provide thermal management solutions.

Additional ECTC special sessions explored the impact of industry-government co-investment for the advanced electronics sector in North America, Asia and Europe. The RF packaging special session discussed substrate options such as glass and fan-out and progress made to extend laminate substrates into higher frequencies. One special session featured startup presentations complete with judges (ECTC's version of *Shark Tank*). Challenges in education and workforce development were discussed with university and industry participation.

Hybrid Bonding Tops the List

ECTC featured almost 70 presentations on hybrid bonding. Samsung described its work in hybrid copper bonding technology (HCB), demonstrating a 16-high DRAM stack and the use of metrology to predict Cu expansion and target the Cu pad dishing control. SK Hynix described its development of a low-temperature process using SiCN and surface activation. TSMC, Sony, IBM, Imec and Intel discussed extending Cu-to-Cu bonding to submicron pad pitch. Process in die-to-wafer (D2W) hybrid bonding was discussed by IBM, Imec, IME and A*Star. Wafer-to-wafer (W2W) hybrid bonding advancements were presented by Applied Materials, CEA Leti and others. Micron Technology focused on the development of a double cantilever beam technique for W2W bond energy measurement.

New developments for hybrid bonding by equipment and material companies including Besi, EVG, SUSS MicroTec, Sony Semiconductor Solutions, TEL, Toray Engineering, Yamaha Robotics and Mitsui Chemical were presented. While Besi and Applied Materials focused on D2W, EVG discussed W2W bonding for highly bowed wafers and other process developments.

CMOS image sensors (CIS) were an early adopter of W2W hybrid bonding. Sony and CEA Leti presented new research. CEA Leti discussed a new generation of image sensors with the introduction of AI features that permit the sensor to process image data, understand the situation, and intervene. Both hybrid bonding and high-density through silicon vias (TSVs) are used (Figure 1). Sony discussed its D2W 6 μ m pitch hybrid bonding three-layer stacking process for image sensors. Sony also presented its study of 0.4 μ m pitch W2S developments for CIS. Samsung described its 0.5 μ m pixel three-wafer-stacked process.

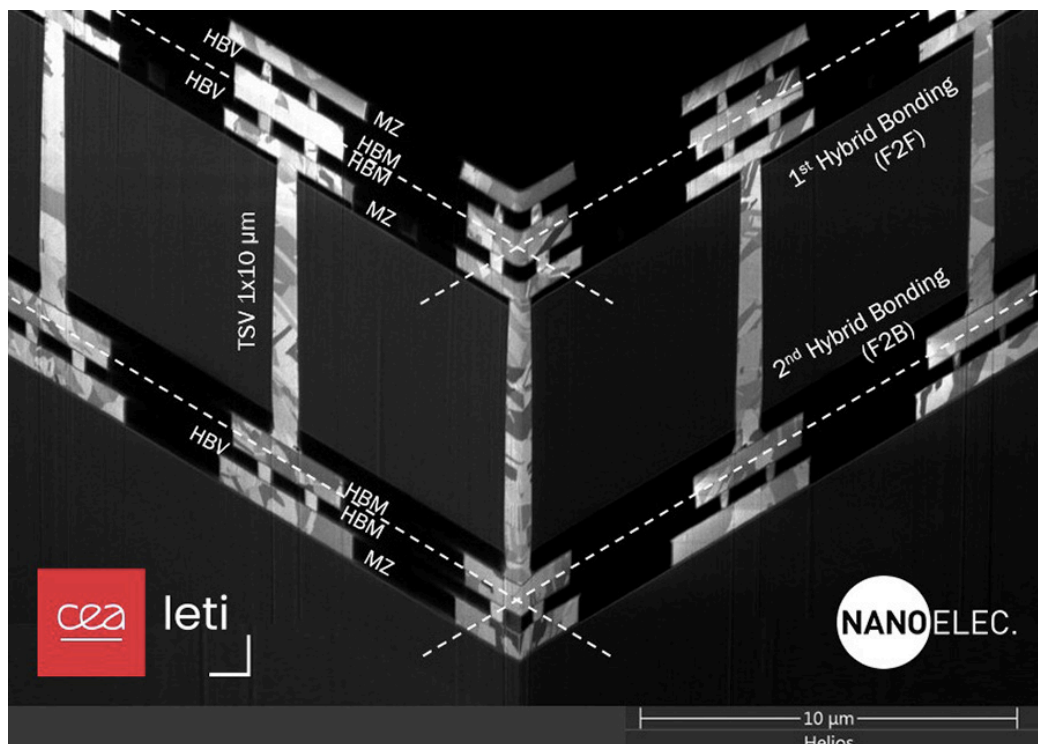


Figure 1. FIB-SEM 3-D cross-section of the entire test vehicle structure. Pitch is 6 μ m for the hybrid bonding pads; HD TSV dimensions are 1 \times 10 μ m.

Fan-Out Wafer Level Packaging and Substrate Developments

An evening panel organized by Rapidus addressed Substrate-Scaling Challenges in Chiplet Integration with speakers from Intel, TSMC, Synopsys, Resonac, Applied Materials, SPIL and start-up LQDX.

IBM described its developments in stacked via substrate designs and achievements of 30 μ m pitch for a bridge solution. Resonac discussed dry film developments for 1.5 μ m line and space build-up features. Applied Materials presented its work on silicon core substrates for signal and power integrity optimization. Canon discussed next-generation RDL packaging for large interposers. Intel discussed a CMP process for panels with glass cores. Applied Materials presented a dry process to fabricate fine features on advanced substrates. Arakawa Chemical Industries highlighted the use of direct laser patterning for RDLs. DNP discussed its glass core substrate developments while Yield Engineering Systems detailed high-aspect-ratio through-glass via etch performance for glass core substrates.

Presentations from Fraunhofer IZM, Samsung, Nepes and DECA focused on developments in panel FO-WLP. Mediatek examined FO package-on-package solder joint reliability during system power cycling. Panel FO as an alternative to leadframe packages was presented by Nepes. SK Hynix discussed a vertical fan-out package for mobile applications providing a thinner package with higher performance. RDL interposer developments included TSMC's discussion of CoWoS-R where a redistribution layer (RDL) interposer is used instead of silicon and SPIL's RDL structure with an embedded bridge technology. ASE and National Cheng Kung University (NCKU) discussed void migration kinetics in fine-line Cu RDL under high current stressing. Fraunhofer researchers discussed wafer-level packaging for high-performance computer modules. Amkor examined different Cu RDL designs for wafer-level packages.



Figure 2. Turnout was strong for the annual conference.


Co-packaged Optics Just Over Horizon

A special keynote by Professor Keren Bergman of Columbia University focused on petascale photonic chip connectivity for energy efficient AI computing. Co-packaged optics (CPO) sessions included presentations from Broadcom and SPIL, Corning, Tokyo Institute of Technology, Kyocera, Cisco Systems, IBM, Marvell and TSMC. Sumitomo Electric Industries described a 3-D-printed beam expanding lens for chip-to-fiber vertical coupling. Furukawa Electric discussed air cooling for QSFP and OSFP CPO modules. IBM Canada and Globalfoundries presented developments on fiber attach for CPO. Imec with Ghent University, Rain Tree Photonics with IME A*STAR, Senko Advanced Components, and Clemson University also discussed recent developments.

Sensors for Wearables

Numerous presentations discussed sensor packaging for wearables and medical applications. MIT Lincoln Laboratory presented on reworkable superconducting qubit packages for quantum computing. CEA-LETI, Kobe University, and IME A*STAR also discussed qubit bonding developments for quantum applications.

Kioxia presented an option for high-bandwidth memory using vertical wire bonding.

Next year, ECTC will be held in Dallas, TX. 

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Getting Flexible

Rigid-flex brings the best – and worst – of both worlds.

COMBINING ALL ASPECTS of a flex circuit with a rigid board that makes full use of HDI techniques is one of the breakthroughs of our time. The stacking connectors for board-to-board or the typical flex circuits are bypassed. If you've ever tried to connect a flex circuit to a stacking connector, you know that's a bottleneck in the process – blindly positioning the flex connector over the mating connector can be fiddly to the point of destroying the connectors. Now what?

Rigid-flex projects remind me of digital/analog projects: the best of both worlds and the worst of both. Just for starters, if the team is taking this route, you know they are serious about holding things together with all possible integration. Both technologies are well understood on their own, though the rigid camp is larger and better understood.

Flex circuits on their own. Flexible printed circuits (FPCs) require more than a change of materials from their stiffer cousins. Additional tolerance must be designed into the data. Reason: The different types of material stacks used in the manufacturing process. For the most part, a flex will also have a rigid section where the connector is mounted. The stiffened area could also be extended to host the ESD protection, an LED or microphone; we're flexible.

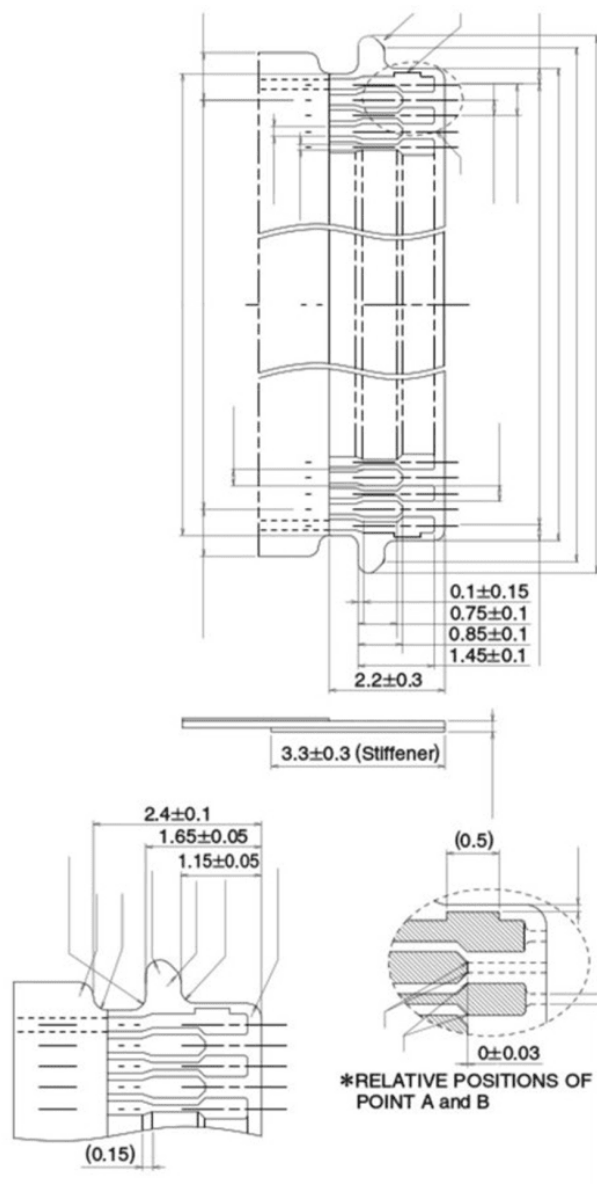


Figure 1. A printed connector with staggered pins.

Capturing this footprint manually was no picnic.

Thankfully, they are downloadable these days. (Source:

Hirose)

A good example of this is a zero-insertion force (ZIF) connector that can be printed on the flex. That approach offers a stiffener at the tail of the FPC that provides a backstop for the pins. It slides into a mating connector, and a lever on that connector locks the flex tail in place. I prefer these to the stacking connector method, whether it's a pure flex or a rigid-flex. Assembly is easier with ZIF connectors.

A rigid-flex use case. Contributing to wearable technology provides interesting outlines. At one point, there were circular islands where we glued on a stiffener in the middle of the flex. Small colonies of components clustered over the stiffener islands while circuitry passed by on all sides. Rigid zones were built into the augmented reality helmet where it passed by the ears, among other locations. Tour an FPC factory or see their boards at a trade show booth; the applications are widespread. I, for one, can't seem to get away from them.

Something like eye tracking required a more sophisticated approach. A 12-layer board isn't a flex no matter what you use for the dielectric material. I've only read about the semi-flexible boards. That sounds cool. With rigid-flex, you get all those extra layers where they are needed.

Then there's the flex core jutting out to get busy with a specific collection of nets. The configuration I've seen most is a three-layer flex inside an eight- or 10-layer board. An odd number of layers starting with a single sided flex for ultimate flexibility is not uncommon.

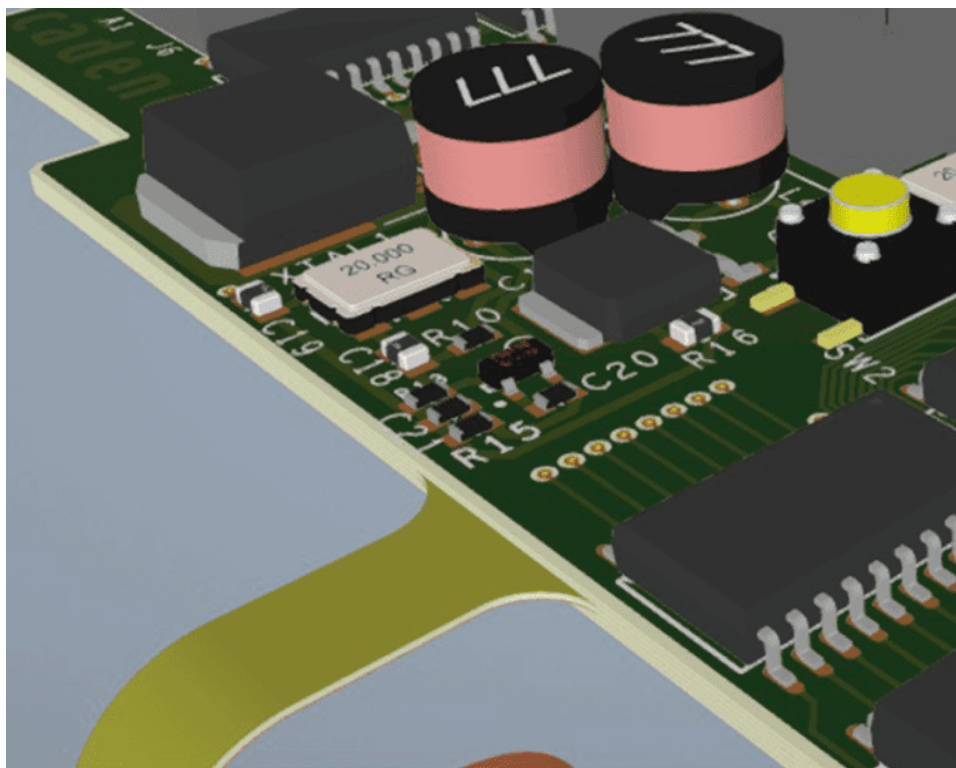


Figure 2. Note the radius where the flexible core extends from the rigid section. This plus a bead of epoxy act as stress relief for the flex tail. (Source: Cadence)

The advantage of rigid-flex. The polyimide core stackup opens the door for components on both sides of the rigid area. Most of the time, the form factor is going to be “as small as you can make it.” This isn't a low-tech solution, so you know the problem you're solving is going to be complex. Enter the ball grid array (BGA) and all its little constituents. Smaller BGAs support the bigger ones, though they may wind up on a different piece of rigid material elsewhere in the rigid-flex board.

Sticking with the AR theme, one of the use cases was an antenna flex extension where the location and orientation of the antenna was part of the overall product outline. The radio chip was on the rigid-flex board so the remote antenna would be part of the flex appendage. Special cases like that might also get their dedicated layer of EMI shielding.

This EMI suppression material must be soldered to the ground mesh that is selectively filled in for the purpose. A small number of slots must be cut in the coverlay to expose those filled areas since the EMI film goes on last. These things need to be accounted for in an extended number of artwork layers.

Being a good neighbor is a universal goal. Coexistence is always front of mind, especially early on. Once a working solution is found, try removing the safeguards to see if it still meets the design criteria. That's what we call lean design, as the parts count reduces over time. In practice, it's just as likely in the early goings that the design will want more filters or some other improvements that add to the parts list.

If you're familiar with the FPC process, then you know the transition from the stiffened area to the flex area is one of the pain points. The same holds true for exiting a rigid zone. The polyimide spans the entire rigid zone plus any flex excursions out to their destinations. Those destinations can have an entirely new board with the same construction as the primary rigid zone. Otherwise, the usual type of stiffener and connector options are in play.




Figure 3. The options are endless with segmenting electronics over rigid-flex designs. (Source: Cadence)

What you don't get to have is a four-layer board in one location and a 10-layer in another. It's all baked as the same layer cake, so the lamination process is the same for all multilayer rigid sections. At the far end of the flex tails we can deploy the usual assortment of flex geometries. We usually picture a connector, but it could be any sort of component mix that can be implemented on a single-sided FPCA.

Routing controlled impedance lines on a rigid-flex PCB. This scenario comes up often. We want to extend some differential pairs from the rigid zone out across a flex zone. We have to assume a three-layer flex with ground mesh on the outer layers and signals inside the Faraday cage. That's the table stakes for controlled impedance. Having the signals in the center of the flex stackup reduces stress on the signals as they occupy the centerline of the flex stack. A two-layer approach stretches and compresses those traces where the flex has a bend region.

We want to maintain the impedance from inside the rigid zone to outside. The way to do that is to continue the mesh on the outer layers of the polyimide wherever those traces may go. Beyond that controlled impedance routing region,

it's more likely that we would go with a solid ground plane on those outer flex layers. We're not maintaining flexibility, but we are maintaining the reference planes above and below the transmission lines.

If you want to cut down on connectors with their inherent failure modes and assembly challenges, rigid-flex might be the way forward. They take more time to floorplan and get them to conform to the fabricator's limitations, but the results in assembly can be their saving grace. The increased reliability is just icing on the cake. You can be rigid and flexible at the same moment. 

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

Talking Points

While AI offers specialized communication skills, it creates new data-storage and security challenges.

MANY OF US would struggle to grasp the concept of a zettabyte in any practical sense. Mathematically, it's 1 trillion gigabytes and, between we humans and our machines, we expect to generate more than 180 zettabytes of digital data in 2025. Right now, about 330 million terabytes are being introduced into the world every day – that's equivalent to the entire US population filling their OneDrive allowance on a daily basis. According to [this essay](#) on the World Economic Forum, storing our data will present major challenges: the way things stand, in 100-150 years' time there will be more data bits than atoms on the Earth and storage will consume more than the total energy generated today.

Problems notwithstanding, our prodigious output is an impressive human achievement. We have progressed through cave paintings, smoke signals, the invention of paper and books, to the many prolific techniques we have available today. It's all about the drive to communicate and express ourselves, which is embedded deeply in our nature.

Now assisted by AI, we could exceed even our own predictions. With more or less universal access to large-language models like GPT (generative pre-trained transformer), we can produce text at an incredibly fast rate. Text-to-image models like OpenAI's DALL-E and Google's Imagen now provide even more powerful tools for creative expression. We can create digital artwork that most of us simply would not have the skills to produce any other way, and in vastly less time than would be needed using traditional media or even manual digital tools. This is incredibly empowering technology that can be used to share ideas, visions and creative passions in more natural and intuitive ways than previously possible. On the other hand, the data mountain is set to grow exponentially.

There will also be transformative effects on our ability to communicate from person to person in real time, in the real world. Soon, we could be able to translate directly between languages, when talking face-to-face, with no discernible latency. By promoting interactions across language and cultural barriers, this could greatly enhance mutual understanding and realize numerous benefits.

On the other hand, while the extent, volume and importance of our digital communications increases with the assistance of AI, the same technology is also putting more power in the hands of fraudsters. While AI can help us to express ourselves, it can help others to overcome the authentication mechanisms that protect our personal content and our identities on social platforms, financial services, healthcare, and other Internet-based services.


Some recent scams have sent texts to victims, claiming to be a friend in trouble and seeking assistance, usually involving a money transfer to bail them out of a desperate situation. Some wary targets have had the presence of mind

to call their friends for confirmation. But a deepfake capable of replicating voice or appearance would be much more difficult to detect. Then imagine that deepfake further augmented with recognizable personal characteristics such as mannerisms or idiosyncrasies like favorite phrases or even words that we may misuse or misspell. Recall that spooky scene in the first *Terminator* movie, when the cyborg replicates a female voice to get information during a phone call; now modernized and more powerful. We may need the help of defensive AI to spot the anomalies.

A US study of identity fraud by [Javelin Strategy and Research](#) found there were 15 million US victims in 2023, losing \$23 billion to scams alone. Since the pandemic, online identity fraud has increased significantly as scammers joined the work-from-home revolution, creating fake online accounts using stolen identities and taking over existing accounts. Strengthening authentication mechanisms using techniques such as two-factor identification and biometrics is the necessary next step in what will certainly become an escalating battle.

Deepfake has the potential to overcome biometric authentication, including fingerprints, retinal scans and behavioral biometrics. According to security experts, combining multiple authentication mechanisms can strengthen protection. Token- or certificate-based authentication can be more resilient against stolen credentials. On the other hand, these are more complicated to implement and gaining access can take longer. The ease of use that goes hand in hand with the convenience and immediacy we enjoy needs to be preserved.

While the battle against AI-powered fraud will continue, data centers face their own battle to handle the increasing intensity of AI workloads. Photonics may be able to help, and startups are already finding ways to create the faster and more efficient modulators that will be needed. Optical networking is already reaching ordinary homes, but here the opportunity is to use photonics at the server level to move data at extremely high speed between processors, and even within the chips themselves, to utilize the computing resources available throughout the data center to maximum effect.

Board-level photonics at these data speeds is an esoteric technology that's consuming significant startup capital. It could quickly become routinely adopted in our quest to manage the huge amounts of bits that make up the data we are now seeking to collect, process, create and store in every minute of every day. Ultimately, our goal is to communicate – the process of sharing information, knowledge, emotions, experiences, feelings, helping us all increase our understanding of ourselves, each other and the world around us. 

ALUN MORGAN is technology ambassador at Ventec International Group ([ventec-group.com](https://www.ventec-group.com)); alun.morgan@ventec-europe.com. His column runs monthly.

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Sunny Times at Sunstone Circuits

One year out from its merger with American Standard Circuits, the West Coast fabricator is evolving to meet a changing customer base.

by TYLER HANES

From its inception as part of Electronic Controls Design in 1972, to its joining with American Standard Circuits last July, Sunstone Circuits has been committed to innovating in the industry – for instance, it is said to be the first to offer online quoting and ordering in the 1990s – as well as providing exceptional customer service.

To better understand what makes Sunstone go, PCD&F visited the company's 32,000 sq. ft. facility in Mulino, OR, in late April, and took an inside look at its operations.

The company has historically been focused on high-mix, low-volume offerings with an emphasis on quickturns – having around 99% on-time delivery – and quality – with less than a 1% return rate, said vice president and general manager Matt Stevenson.

“That’s kind of what we’ve been known for over the years,” he said.



Matt Stevenson

ASC Sunstone usually has in the neighborhood of 4,000-5,000 active customers, and that customer base has always ranged from students at a local university or high school and local companies making audio equipment or aftermarket car parts, to entrepreneurs and inventors or Fortune 500 companies.

“It has really run the gamut,” Stevenson said.

Quite a few of those customers remain, but the company's customer base has begun to narrow toward the military and aerospace industries, and with that change, ASC Sunstone has worked to meet the new requirements that come with those industries.

"Over the last 10 or 12 years we've been advancing our technology and advancing our ability to do more volume and offer more than we were in the past," he said.

Those new customers are primarily looking for domestic PCB suppliers with ITAR certification that can meet the strict standards for military and aerospace work.

"We're starting to see more stringent prints and kind of a higher level of overall requirements from our customers," he said, "rather than just the mom-and-pop inventors who are sending us a simple double-sided board without any other requirements."

That has led to a shift not just for the manufacturing side of the business, but also from a sales standpoint, as the stricter requirements require everyone to make sure they dot their i's and cross their t's, Stevenson said.

"It's challenging us to be better and understand everything a bit more," he said.

But even with the higher level of technology and changing customers, ASC Sunstone is not moving far from its roots, Stevenson said.

"We're still quickturn; if you need it in two days, even if it's 50-60 panels, we can still do it. We still like to do it," he said. "But our technology is getting higher and our ability to do more volume has gotten higher as well."



ASC Sunstone Circuits operates out of a 32,000 sq. ft. facility in Mulino, OR.

Last July, [American Standard Circuits and Sunstone Circuits merged](#) to form the new ASC Sunstone, which boasts a broad range of PCB types, materials, and certifications, and that has opened more opportunities for Sunstone to grow its services and customer base, Stevenson said.

He said in the past, Sunstone had to rely on recommending other manufacturers when customers needed capabilities the company didn't have, and even those other manufacturers had some limitations in what they could offer.

Today, with the addition of ASC's certifications and capabilities, there are very few jobs the company can't take on.

He said those new capabilities, combined with the knowledge sharing between staff members and the blending of the two companies' business models and customer service experience, are allowing ASC Sunstone to take the best of both worlds and elevate the business to new heights.

"We're now able to market and help customers with just about any PCB need they have," Stevenson said.

When it comes to the advancing technology and needs in the industry, ultra HDI is the next big step on the horizon, and there is a growing demand for heavier and thicker copper, quicker heat distribution, and higher-performance materials, he said.

"There's a lot more things to consider today than there ever were," he said.

Stevenson said those new demands, plus the continued growth of additive manufacturing processes for PCBs, mean the industry will likely look a lot different in the coming years.

"I could see in the next five to 10 years, it's a different industry from today," he said. "From a manufacturing as well as an engineering standpoint."

Sunstone has always evolved to keep up with technological curve, but has not traditionally been on the forefront, while ASC has specialized in the upper tier of technology and capabilities, Stevenson said.


So with Sunstone being one notch behind ASC on the proverbial tech ladder, the plan for the combined company's future is to follow that same trajectory, he said.

"Hopefully we can move up that curve at that same rate so they can start offloading some of their work to us as we're able to do it," Stevenson said. "Then they're able to take on more of the more high-tech, cutting-edge stuff."

With that plan for the future of the company in place, Stevenson also made sure to point to Sunstone's history and experience as a PCB fabricator, as well as its role in innovating the industry.

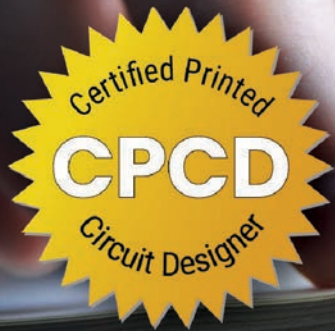
"Sunstone has been manufacturing in one location for 50 years, so we've got history behind us," he said. "And we've got people that have been here almost as long as that, so we're a company that's built on experience."

With the ASC merger, everything that a customer could want from a circuit board standpoint, whether its domestic production in Mulino or Chicago or offshore manufacturing of PCBs or anything else in the supply chain through ASC's Global Sourcing Division, the company has it all covered, Stevenson said.

"We are aiming to be that solutions provider," he said. "The ultimate source for PCBs in the industry for those companies." 

TYLER HANES is managing editor of PCD&F/CIRCUITS ASSEMBLY; tyler@pcea.net.

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'Everybody is Growing'

The East Coast trade show brings news of a steady industry, while puncturing myths about AI.

by TYLER HANES

Members of the electronics community gathered in the Boston suburb of Boxborough in early June for the return of PCB East, PCEA's annual event featuring four days of technical sessions and a one-day exhibition.

This year's exhibition featured more than 65 companies running the gamut of the PCB industry, from fabrication, design, and assembly to test and inspection, and most of those companies reported steady growth thus far, with small gains over 2023.

For Cadence Design Systems, revenue has continued to grow over the past few years and is up around 15% so far in 2024, said product management director Patrick Davis.

"Cadence is doing great," he said.



Cadence Design Systems' Scott Burton, on left, and Patrick Davis speak to attendees at PCB East in June.

Davis said the company has expanded with new acquisitions and personnel over the past year, and CEO Anirudh Devgan believes the company is on the right track to continue that growth into the future.

“Anirudh has a very good vision for where Cadence is going,” he said. “I think it’s the beginning of a very cool rise.”

Business has also been good for Newgrange Design, with plenty of growth in 2023 and forecasts for continued success in the future, said president Matt Leary.

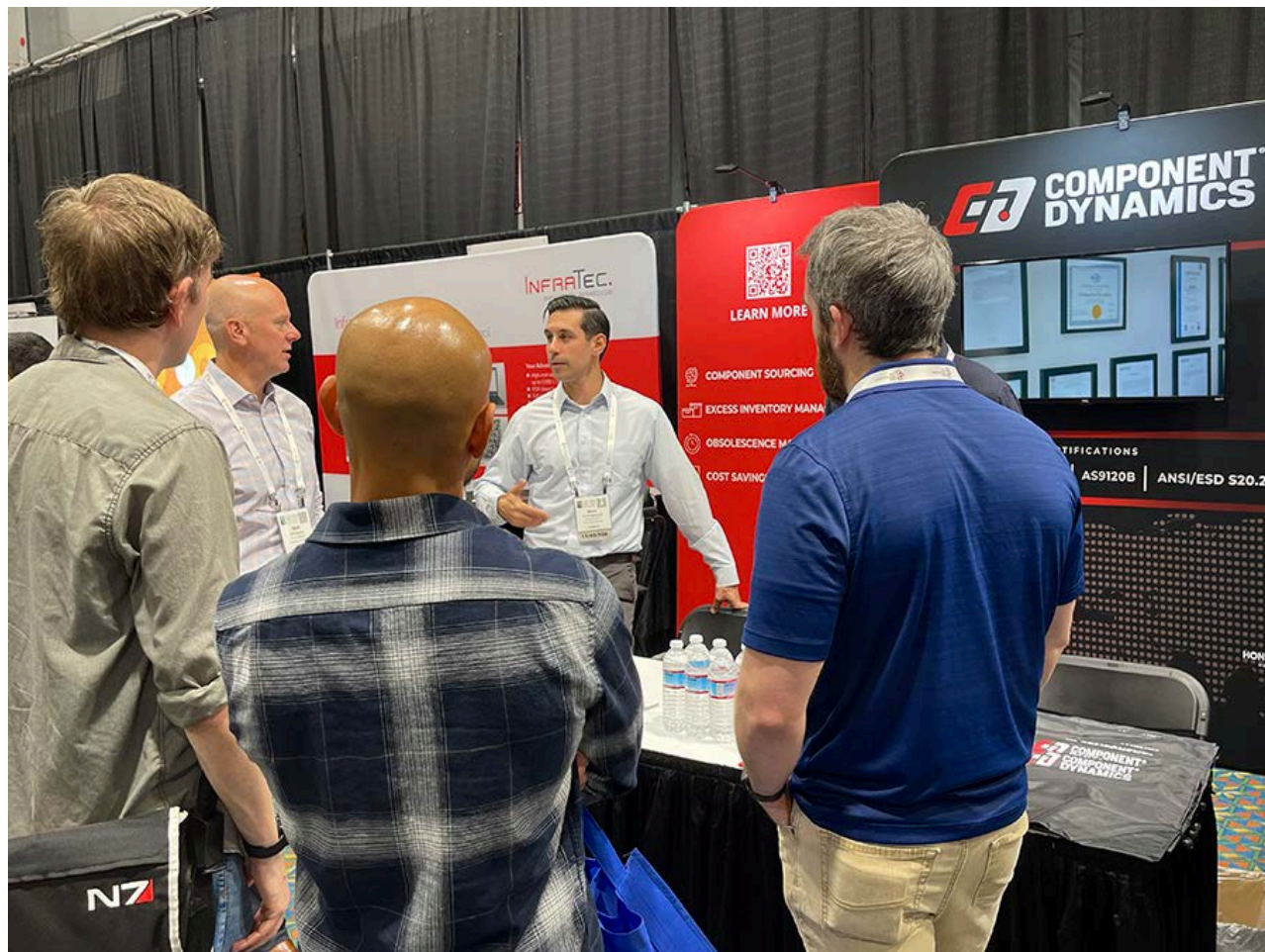
“It was our best year ever,” he said. “We hope and expect to continue to grow in the coming 12-24 months.”

He said right now is a good time to be in the electronics hardware industry with its continued expansion into other sectors.

“Virtually every industry is using electronics to increase data collection and improve connectivity,” Leary said. “We expect that to continue for the foreseeable future.”

Elsyca, a provider of simulation electrochemical process software including PCB DfM and plating, is relatively new to the PCB industry, but shows like PCB East and PCB West are helping to spread the word about that side of the business, said sales engineer Agnieszka Franczak.

The company is also benefiting from nearshoring and reshoring efforts that are seeing PCB production moving away from China, and business has been good so far in 2024 as those efforts gain strength, she said.



Component Dynamics' Marc Schwanbeck speaks to exhibition goers during June's PCB East.

With the respective Chips Acts in Europe and the US to bring in more domestic semiconductor fabrication, PCB production will also see more shifts into Europe and North America, she said.

Electric vehicles are also growing, and eventually will be the norm for the US and Europe, which will benefit the PCB industry and the entire electronics industry, she said.

“If this is the future, then this is also the future for PCB business growth,” she said. “Then the next question is how small we’re going to go with these electronics, but that’s another conversation.”

At Optris Infrared Sensing, a company specializing in infrared measurement devices for noncontact temperature measurement, business has been close to the same as last year, said sales application engineer Chris Sullivan. That includes the usual fluctuations that come from being a company that specializes in inspection, he said.

“There’s been a little bit of a decline, but our stuff is usually what I call a lumpy business,” he said. “We might have a month where a bunch of systems come in and the next month nothing, so it’s still a little lumpy for me, but overall, my answer would be steady.”

Fine-Line USA CEO Eran Navick reported a growing PCB fabrication business in the US, and said the company has been meeting its revenue goals for the year.

He said he expected a mediocre year for the business, and while 2024 has been better than expected, orders have been smaller, meaning it has taken more work to bring in business and keep revenue up.

Navick thinks industry will pick up a bit for the second half of the year, but with material costs rising and some uncertainty in the speculative market, he isn't anticipating large growth.

For assembly services provider SVTronics, the company is getting ready to add another shift of production after seeing strong business over the past year.

"Business has been really good," said salesman Ryan Dickey. "It's been across the board, but particularly in the aerospace and semiconductor industries."

During the slowdowns caused by Covid, the company moved to a single shift, but after seeing growth over the past year, SVTronics is getting close to bringing back another shift for continuous assembly, he said.

"We're about to start picking back up on a second shift and go 24 hours again," Dickey said.



All Flex Solutions' Amanda Schaner-Martinez, on left, and PowerRep's Kerry Montani discuss the company's offerings with PCB East attendees.

PCB label provider Identco has been growing its team and adding new talent to meet needs of customers that are continuing to grow, said sales manager Kendall Brooks.

“Everybody is growing, and we get to grow with them,” he said.

Brooks said the company has seen growth throughout the electronics industry, but one main source of growth has been the rise in AI servers, which has included customers from PCBs to power distribution.

“Almost every single one of them has at least some piece of that AI infrastructure coming into play,” he said.

He said another interesting shift has been customers redesigning their products to be greener and more sustainable, and it’s exciting to see where the industry will end up as those changes take hold.

“When you’re in the middle of that kind of shift, it’s always fun to see,” he said.

AI: The Future is Now

PCB East also featured another look into the future from keynote speaker Harold Moss, who shared his vision for AI in the electronics industry.

Moss is regarded as an expert in AI, cybersecurity and cloud solutions, beginning his career with IBM, where he led significant advancements in the company’s enterprise computing systems. He later held roles at EMC, Akamai Technologies, and various other organizations, and is currently CEO of Tautuk.

Moss said electronics design revenue grew to \$4.7 billion in last year’s third quarter, and will continue to grow through 2024 and beyond, so companies will be looking to increase their productivity – particularly through the use of AI as a design tool.

“It’s going to be here whether you like it or not, and I’ll tell you it’s not 50 years away,” he said.



Tech visionary Harold Moss speaks about AI's growing role in electronics manufacturing during the PCB East 2024 keynote address.

AI's strength in the design industry will not be generating entirely new designs, but it will be able to analyze proven designs and use that knowledge to check designs created by a human, he said.

"AI isn't about generation, it's about the ability to constantly take inputs in and evolve its thinking just like a person does," he said.

Moss said the visions and fears of AI taking jobs from workers or taking over the world like *The Terminator's* Skynet are unfounded, because AI will only ever be as smart as the average labrador retriever – able to run and get a ball when told, but not do anything more complicated than that.

"It doesn't give you a lot of value, it just helps automate and make things go faster," he said.

Moss said humans have always been afraid of change, and pointed to the slow adoption of the light bulb over candles, trains over horse-led carriages, and cellphones over landlines. But he also pointed out that each of those changes took place over shorter periods of time.

While it took decades for people to fully adopt the light bulb, smartphones began to take over in a matter of years, he said, showing that people are getting faster when it comes to accepting new technologies.

When it comes to the next major technological change, AI is at its center, but it will act as an enabler and an equalizer – not as a replacer, Moss said.

“AI doesn’t replace people, it just allows them to do the next cool thing,” he said. 🗣️

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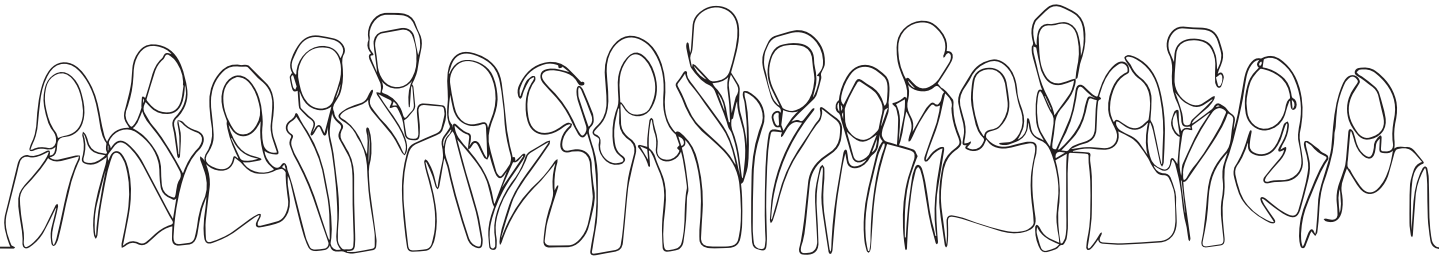
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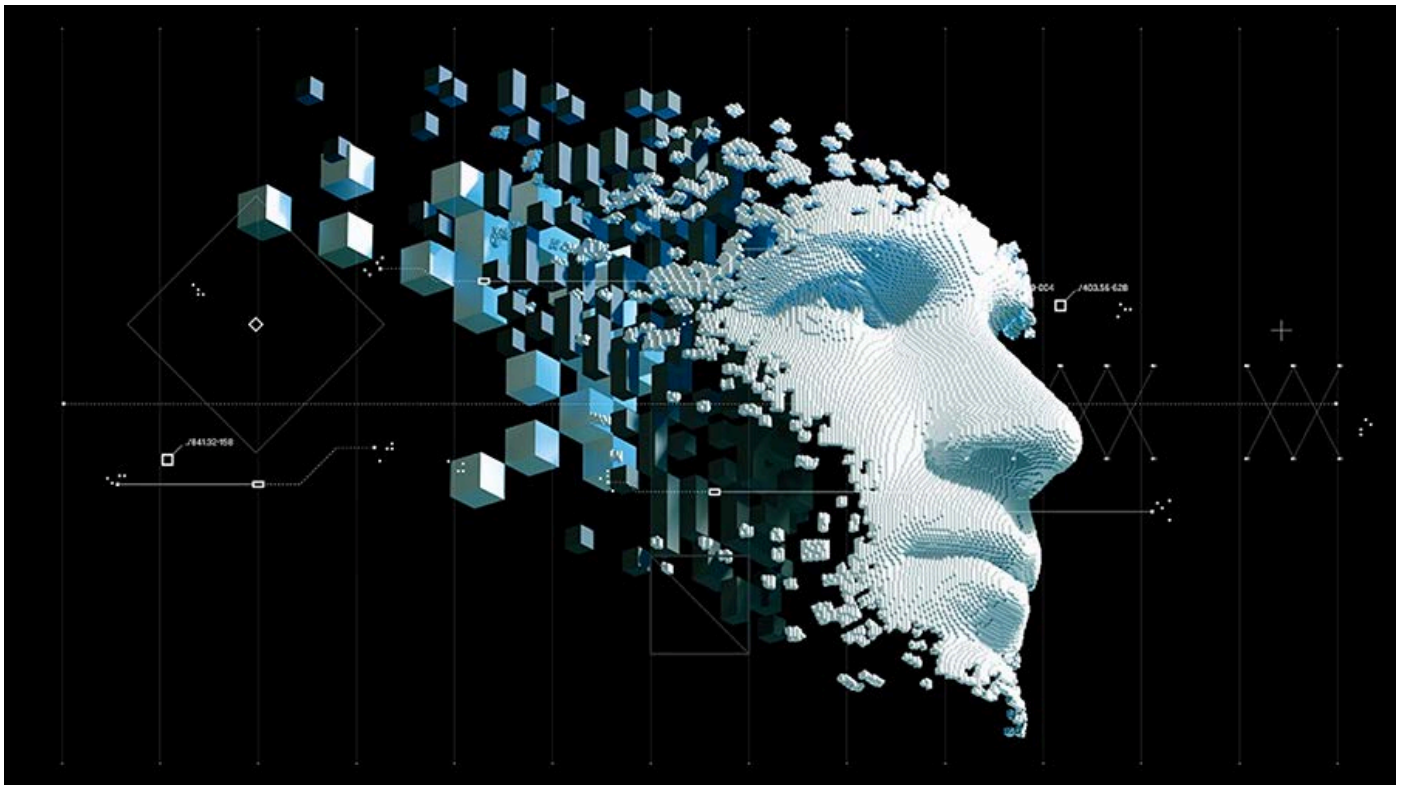
AI: The Shiny New Tool in the Engineer's Toolbox

Searching for components and automating schematic capture are just two of the ways AI will be implemented in PCB design.

by DAVID WIENS

During the past 10 years, artificial intelligence (AI) has progressed from a visionary concept to a mainstream reality in many large companies. AI is becoming a crucial lever for improving operational productivity and user expertise.

AI is a set of computational technologies that enable a machine to reason and infer without any human intervention. These technologies are developed using cross-disciplinary approaches based on mathematics, computer science, statistics, and psychology. AI based solutions can analyze high volumes of data to identify trends and patterns which can then be used to improve existing processes and make recommendations to assist users in making better decisions.



The world of AI opens a new realm of technologies to propel electronic systems design into the future.

With significant developments in visual and voice recognition, natural language processing, autonomous vehicles, and data mining, AI technologies have become even more advanced and capable of offering enormous advantages toward reducing the complexity of electronic system design and boosting design efficiency, quality and productivity.

Key areas for applying AI for PCB design are those that are largely manual or require expert knowledge of electronic systems design tools. AI enhanced tools empower entry-level users to perform tasks traditionally achievable only by experts.

Expert PCB designers use tools in specific ways to accomplish good design. These users have a deep understanding of the domain and circumnavigate around the nuances of the tools to deliver efficient designs. While it is possible for any engineer to become an expert, it takes years to develop the required skills.

AI mines completed designs for patterns of how tools are used to accomplish a design task and manages that knowledge in a reusable form. This supports better design quality by guiding the designer or engineer to the next logical step without having to search for the step.

Specifically, in the typical electronic systems design process AI technologies – including machine learning and deep learning – can be leveraged in a number of areas to accelerate decision-making, automate mundane processes, improve the efficiency of new users, and optimize the performance and manufacturability of multi-domain systems. These include the following:

Component selection. Design engineers spend a substantial amount of time researching and selecting components that meet the design requirements. They go through datasheets from multiple component manufacturers to find the right set of components that can be used in the design. A model could be developed based on historical information and used to recommend viable options to narrow the search. For example, when a processor is selected, the machine learning model could predict other components needed based on historical knowledge.

Component model creation. Generating models to represent the components (e.g., symbols, 2-D/3-D physical geometries, and simulation models) also takes a substantial amount of time. In large organizations are teams of librarians tasked to go over datasheets of components and convert them into models that can be used in design tools. This not only requires deep electronic domain knowledge but also an understanding of the various tools used to generate models. By using AI technologies, these datasheets can be processed automatically by the system to generate the required models.

Schematic connectivity. Once components are placed in the schematic, establishing the connections is another manual task which is time consuming and error prone. Training a machine learning model by extracting information from a completed design about how components are used and how they are connected enables the schematic capture tool to recommend the components a user might place in the schematic. Once the user confirms the placement, the tool can suggest pin-to-pin connections to speed up the design task.

Dynamic reuse. Functional blocks from completed designs could be analyzed for reuse and managed in an intelligent database that can be searched using various parameters. Training a model with deep learning algorithms to


generate a system enables design tools to predict the potential function of a block. Analyzing the components that are placed in the schematic and using the trained machine learning model, schematic design tools can recommend a matching functional block. Similarly, reusable placement and routing blocks can be extracted from completed designs and presented while the designer is laying out a board.

Constraints. PCB designs typically adhere to numerous rules (constraints) for layout, high-speed design, manufacturing and test. This information is usually entered manually into each of the various design tools – a time-consuming and error-prone process. This risk can be considerably managed if the tool can recommend the set of constraints and values that need to be defined for various design objects. These recommendations should be based on the technology used in the current design and knowledge collected from released designs.

Layout – placement and routing. Placement of components and routing of traces take a significant amount of the overall time in a project. Harnessing the knowledge from completed designs, an AI system can recommend placement and routing strategies.

Analysis and verification. Utilizing AI algorithms, analysis and verification tools can generate better designs by understanding various design sensitivities, such as changes in electrical material properties, physical design dimensions and their impact, transceiver I/O characteristics, temperature/voltage variations, and the combined effects of all these variables on the board or system. AI algorithms can be applied to deliver better mesh refinement, to fine-tune user options to produce more accurate simulation results, and to provide better surrogate modeling for via, trace and cable optimizations. Recommending appropriate values for various settings to run various simulations based on historical runs yields better results.

Design synthesis. The ability to auto-generate PCB designs as required and the corresponding manufacturing outputs is the ultimate goal of applying AI to electronic systems design. This not only reduces the time required to complete a design but also eliminates costly mistakes usually caused by manual efforts. Generative design relies on AI algorithms to find an optimal solution through the systematic variation of parameters, structure, or shape of a board. Innovation in AI-driven behavior models for the well-known parts of the board design process speed development of generative design technologies.

By incorporating multi-physics simulation, data analytics, and AI capabilities, EDA vendors' products can demonstrate the impact of design changes, usage scenarios, environmental conditions, and other variables. This will drive down costs, reduce development time, and improve the quality of products and processes. 

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System-in-Package and Multichip Module Technology

Moving forward on the 'More than Moore' roadmap.

by YANIV MAYDAR

We're witnessing a rapid evolution in advanced semiconductor nodes and market growth due to the meteoric rise of AI, mobile, [autonomous automotive](#), IoT, communications and cloud, health tech, and wearables. The various technologies driving the overall functionality of systems and devices associated with these applications have increased exponentially, impacting factors such as device performance, energy consumption, power dissipation, and space (miniaturization).

Development of the system-on-chip (SoC), combining digital and analog, MEMS and photonic sensors, has led to the small form factors used in smartphones, health monitors, smart homes, and more. Advancements in smaller feature sizes and the resulting billions of transistors per chip translate into increased functionality, enhanced performance, and greater power – but these benefits come at a price. SoCs are hugely complex systems that generate very high NRE costs and involve other budgetary, time, and market constraints. For this reason, it has become clear that alternative technologies are now urgently needed.

The heterogeneous integration of separately manufactured components into a higher-level assembly – system-in-package (SiP) – is able to leverage the advanced capabilities of packaging technology by creating a system close to the SoC form factor but with better yield, lower overall cost, higher flexibility, and faster time to market. A recent paradigm shift from SoC-centric solutions to SiP-centric solutions has occurred, even for high-volume products.

Differences between multichip modules (MCM) and SiP technology are mainly in their respective scope and functionality. The MCM isn't necessarily a complete system, whereas an SiP is purpose-built to be a complete system within a single package. SiP integrates multiple ICs, along with supporting passive devices, into a unified package, while the MCM represents a tightly coupled subsystem or module packaged together. An MCM can act as a cohesive unit, however, even though it may not encompass the entirety of the system's functionality.

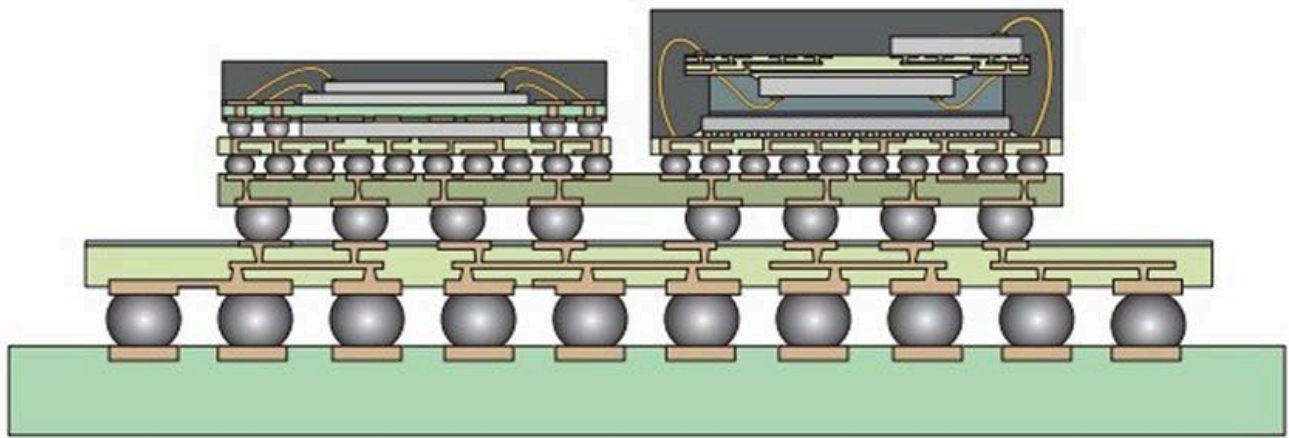


Figure 1. A SiP may contain active and passives components, MEMS, optical components, and other packages or devices, including a combination of bare dies and SMT components.

SiP, Up Close

SiP technology is a combination of multiple active electronic components of diverse functionality assembled in a single unit that performs multiple functions associated with a system or sub-system. The SiP may optionally contain passives, MEMS, optical components, and other packages or devices, including a combination of bare dies and SMT components.

SiP typically refers to standard packages (QFN, BGA, CSP, LGA) that can include different semiconductors (Si, SiGe, SiC, GaAs, GaN) and semiconductor technology generations (CMOS 65nm, 45nm, 28nm, 14nm, etc.).

The SiP-tech evolution is focused on an approach based on current and emerging generations of packages and technologies. Currently, more than 1,000 package families, with sub-groups and specialties, are available in the market. Some packages are highly specialized to niche markets, others are customized for specific functionality, while others are still more generic, serving multiple applications.

Successful design concepts will depend largely on selecting the right SiP configuration based on specific needs for each application and the availability of the components, which can then be integrated into a SiP using the appropriate technologies, including interconnect technology, die attach and seal or encapsulation technologies.

Various technologies can be used in SiP design: interconnect technologies (vertical and horizontal), encapsulation technologies (protection and stabilization), and packaging architectures. The number of available technologies for SiP implementation is growing rapidly and includes not only side-by-side integration but is also moving toward 3-D, with many different interconnect options.

Interconnect Options

Interconnection takes place a variety of ways. Vertical electrical contacts include through mold interconnection, film-assisted molding, X-via, wire stands embedded interposers, and dies. Horizontal electrical interconnects include high-density line and space using subtractive, mSAP, and SAP processes. Specific options include:

- Wire bonding, including stacking options, using various wire bonding diameters and materials.
- Flip-chip, high-resolution and high-density interconnects, enabling fan-in and fan-out technology.
- L/S high-density and high-resolution line and space, down to $25\mu\text{m}$ in substrates and $2\mu\text{m}$ in RDL technology.
- Encapsulation used to protect the sensitive wire bonds and dies from environmental influences.
- 3-D (PoP) package-on-package technology, based on a through-mold interconnect and use of a lid interconnect to enable dies to fan-out and interconnect vertically.
- Fan-out panel-level packaging (FOPLP) and fan-out wafer-level packaging (FOWLP) are among the latest packaging trends in microelectronics for higher productivity, lower costs, and higher yields.
- Interposers, which enable interconnect between low- and high-resolution substrates, matching CTE, as well as stiffening the mechanical structure (**Figure 2**).

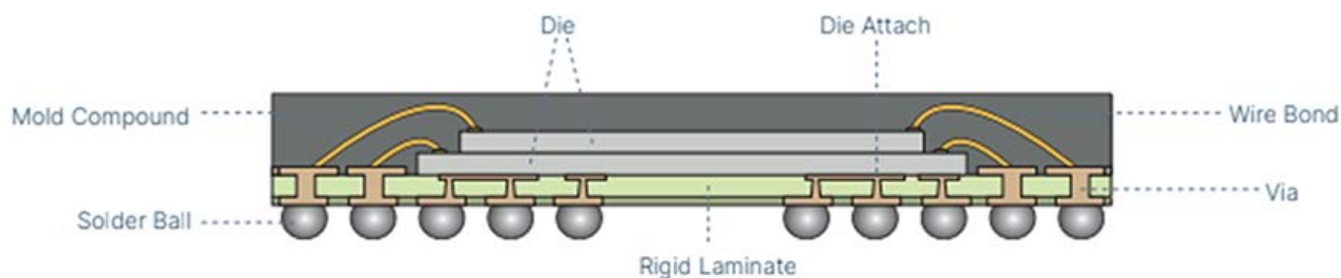


Figure 2. Cross-section of a SiP.

Applications

Most of the requirements and challenges SiP technology has faced have been dictated by the needs of the many diverse applications it serves. SiP, with all its challenges, remains a viable alternative to SoC manufacturing. Provided time-to-market and production costs remain key considerations, SiP will thrive and grow in mainstream technology.

Power functionality: Power semiconductors such as silicon carbide (SiC), gallium-nitride (GaN), and power systems in a package are becoming readily available due to innovative packaging power dissipation concepts.

MEMS functionality: Autonomous vehicles and smart homes are main drivers for sensor modules. MEMS and sensor packaging in general add many challenges to the package design picture, however, such as stress sensitivity, open access to sensor surfaces, and materials and process compatibility in sensing functionality.

Complex IoT devices/edge computing: The internet of things (IoT) can be described as a paradigm whereby objects equipped with sensors, actuators and processors can communicate with each other. IoT devices consist of a

processor with an IP stack and RF interface, and require sensing abilities to interact with the ambient environment.

Application-Related Challenges

SiPs are not a panacea, of course. They come with certain challenges, including wiring density in 2-D/3-D, thermal management, COTS and bare-die co-assembly and processing, and multi-domain testing.

Functionality increases due to the growing demand for diverse device functionality means co-designing will become more relevant. Non-electronics will play a more dominant role in functionality. Co-design of non-electronic functions – optical, mechanical, cooling, and others – which were previously implemented by separate stakeholders for large systems, will now be integrated by manufacturers early in the value chain.

Assembly processes will transform challenges in SiP manufacturing – especially for multi-domain (more than Moore) functionalities, which lies in the assembly process itself – enabling next-level MCM technology (**Figure 3**).



Figure 3. SiPs can be placed on panels using automated SMT equipment.

Finally, reliability requirements must be adapted seamlessly to application needs, which will bring attention to new or unaddressed reliability challenges for sectors such as automotive, aerospace and satellite.

Reliability Analysis and Testing

While significant performance, functionality and form factor improvements are enabled using advanced system-in-package and substrate technologies, a systematic approach and methodology is imperative to mitigate thermo-

mechanical risk and other challenges associated with SiP solutions.

All designed package structures must be analyzed for reliability to have any application value. SiP reliability refers to the statistical probability of product failure during its lifetime, stemming from environmental effects, such as temperature, humidity and radiation, or from the application itself, such as with vibration, pressure, acceleration, etc.

While performing failure analysis for package dependability, possible issues can include warpage, chip cracking, delamination, toughness fracture, plastic deformation, and many other complications. Breaking it down further may encompass hundreds of failure items, wherein the entire analysis process becomes particularly laborious, requiring more time, higher costs and additional testing.

To keep it simple, root causes of dependability issues can be divided into three main categories: [thermal](#) management, mechanical stress and electrical properties.

Although many potential failure modes exist in system design, reliability issues mainly revolve around the following failures: stress fracture, high-temperature deformation, high-temperature deterioration, open circuit, short circuit, line impedance mismatch, electromagnetic interference, and others.

The analysis and testing of temperature, mechanical stress, and electrical system-level reliability issues are summarized below. It's important to note that the implementation of new processes and structures can also introduce new and previously untested reliability issues. If these issues are not detected and resolved in time, they can lead to system abnormalities, causing equipment failure or even major accidents.

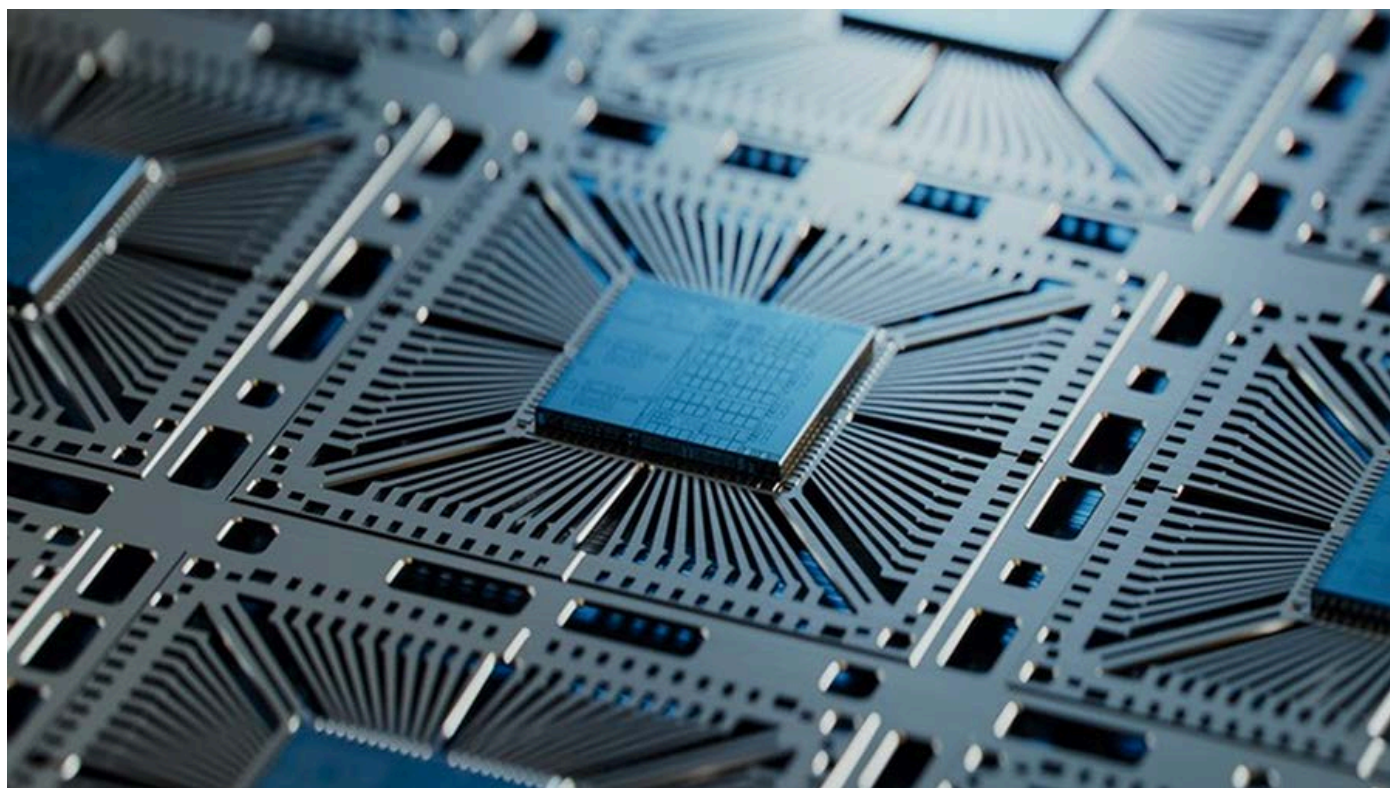


Figure 4. A mounted SiP.

Thermal management. Since no electronic device can operate at 100% conversion efficiency, as some amount of electrical energy is always lost to heat, SiP technology helps to achieve system integration with its unique advantages of small size and high density. Due to the dense placement of multiple chips, however, heat density inside the SiP is higher than that of discrete devices, with heat transfer paths further restricted by the limited space. According to the heat transfer equation, elevated temperatures caused by the SiP configuration are more pronounced than that of packages such as QFN or BGA.

$$Q = kA\Delta T/\Delta x$$

where

Q = heat

k = heat transfer coefficient

A = heat transfer area

ΔT = changes in temperature, and

Δx = changes in distance.

Heat dissipation of the entire system will be impacted, resulting in elevated internal temperatures, if the thermal conductivity issues of the encapsulated system are not resolved.

Irregularities in mechanical stress become evident in cases of excessive differences in coefficient of thermal expansion (CTEs) of adjacent materials. As the temperature rises due to ongoing heat buildup, component performance is also impacted, which in turn affects the overall electrical properties of the system. As a result, most reliability issues are caused by temperature issues, which necessitate thermal simulation analysis.

Mechanical stress. Another important factor in determining the dependability of SiPs is the examination of mechanical stress. In system-level packages, materials used for chips, substrates, leads and solder connections vary. When subjected to influences such as temperature changes or other external environmental issues, various materials will shrink or expand at different rates in accordance with their unique qualities and structure. This can lead to specific consequences in deformation and mechanical stress.

To illustrate, the formula for CTE:

$$\alpha = \Delta l / (l \times \Delta T)$$

where

α = CTE

l = length, and

Δl = length change.


When two different materials heat up, their CTEs vary, creating a noticeably inconsistent strain on system components and resulting in extreme stress conditions. This falls under the category of mechanical stress. Loss failure and overstress failure are the two primary types of failure brought on by mechanical stress. The former refers to the

buildup of low stress continuously applied over an extended period, leading to component loss (dysfunction) that produces system failure. The latter refers to failure brought on by an acute stress event or moment that far exceeds the components' stress tolerance levels.

Much focus is placed on loss failure since such a significant portion of mechanical stress is caused by imbalances in CTE of various materials in high-heat situations. Therefore, it is imperative to investigate the specific causes of this type of failure thoroughly. Because loss failure occurs more frequently in all packing systems than overstress failure, it becomes the more valuable analysis in predicting and preventing unforeseen or uncontrollable catastrophic events.

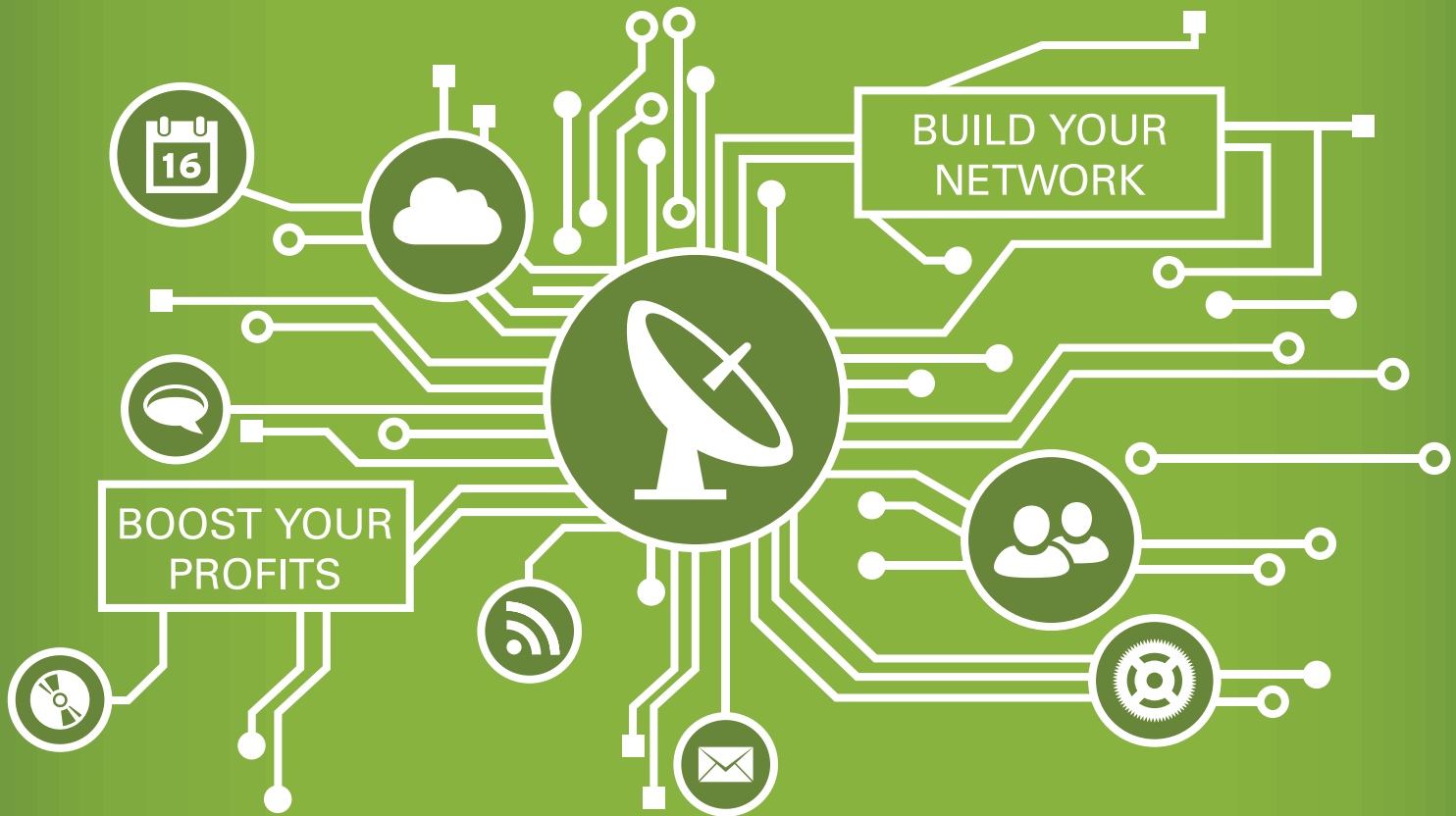
Electrical properties – Outcome of thermal and mechanical stress. Reliability considerations with SiP ultimately manifest as problems with electrical properties because of both thermal and mechanical stress issues. Examining electrical performance is another useful technique to determine SiP dependability and to ensure that it's functioning to specification. The electromagnetic environment of the entire package system is extremely complex. Because of the increasing density of SiPs, and interconnection channel effects on the signal, complete checks are of paramount importance. Critical factors to consider while evaluating electrical performance include EMI, SI (signal integrity) and PI (power integrity).

Conclusion

SiP is the most effective, time-to-market, cost and functionality technology available. It's the main option able to move us forward on the "More Than Moore" roadmap. 

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How to Stay Within the SMT Assembly Process Window

Navigating the balancing act with the application constraints.

by KEVIN PIGEON

Understanding and controlling the assembly process window is not just about managing the solder paste. It's about mastering all process variables across the entire SMT assembly process for optimal outcomes.

The assembly process window defines the range of parameters within which solder paste will meet optimal performance standards. Straying outside this window can lead to defects, rework and inconsistencies, affecting the efficiency and output of the electronics manufacturing process.

These parameters may include acceptable ranges for a number of areas, including but not limited to:

- Total reflow profile time from ambient to peak
- Peak reflow oven temperature
- Time above liquidus
- Rate of temperature change
- Squeegee pressure
- Squeegee speed
- Stencil thickness, design, aperture size, and coatings
- Precision of component placement
- Solder volume
- Component and PCB finish.

Note that the process window index (PWI), a statistical measure determined by the solder paste flux and alloy, is alone insufficient for defining the assembly process window. All the factors above must be considered, too.

Factors to Consider

Parameters that define the assembly process window are not isolated. Rather, they interact in complex ways, each influencing and being influenced by the others. Understanding and managing this interplay is not just about maintaining balance; it is about orchestrating harmony in the entire soldering process.

Reflow temperatures must be high enough to activate the flux and form a reliable solder joint, but not so much as to damage the delicate components or PCB substrates. The thermal profile is also influenced by various factors, including the oven type, conveyor speed, and the thermal mass of the assembly.

The PCB design, including the layout of pads, ground planes, traces and any fixtures required, determines how heat is distributed. Materials with different thermal properties behave differently under the same thermal profile.

Adjustments in reflow profile as well as stencil modifications may be needed to strike the right balance.

The stencil determines the shape and volume of solder deposits. Closeness and depth of apertures can affect how likely bridging or other defects may occur. Whether the stencil is coated or not can also affect how likely the paste is to adhere to the stencil as opposed to releasing cleanly after printing. These factors, together with the solder paste characteristics, will determine the acceptable range of print settings.

Solder paste is a meticulously engineered mixture composed of solder powder and a specialized flux medium. The solder powder's size, shape, and metallic alloy composition determine its melting behavior, while the flux medium's chemistry dictates its activity level and performance under heat. We will look at this in more depth in the next section.

Solder Paste Composition and Impact

The solder alloy determines the mechanical strength and electrical properties of the resultant solder joint. Smaller powder sizes often lead to better printability, enabling finer-pitch applications, but may also increase the risk of oxidation, bridging and voiding.

The flux medium is responsible for removing oxides from metal surfaces, protecting the solder area from further oxidation, and enhancing the wetting process. The composition of the flux medium influences the activity level, viscosity, slump characteristics and residue properties for a particular type of solder paste. Manufacturers must consider:

- **Reliability:** The alloy composition of the solder powder, combined with the protective action of the flux, contributes to the long-term reliability of soldered connections.
- **Printability:** This property is influenced by the physical characteristics of the solder powder and the rheology of the flux medium. Optimal printability ensures consistent deposition volumes (as measured by solder paste inspection), crucial for minimizing defects in fine-pitch applications.
- **Reflow performance:** The flux must activate at the right temperature, promoting excellent wetting and spreading of the solder alloy. The paste should also exhibit good coalescence, leading to well-formed solder joints without excessive voiding.

- **Residue characteristics:** Post-reflow, the residue left by the flux medium can affect the performance and aesthetics of the PCB. Noncorrosive, no-clean fluxes may leave minimal, benign residues, while water-soluble and rosin-based fluxes require a cleaning step.
- **Environmental compliance:** Solder pastes must comply with environmental regulations. Most applications require lead-free alloys, and some now specify that fluxes be halogen-free.
- **Operations:** Consider shelf life, storage requirements, humidity window and tack. These factors will determine how easy the product is to use for an application.

This is only a fraction of the total picture. There can be dozens of additional considerations, including customer-specific criteria, all requiring just the right balance.

The radar chart in **Figure 1** gives an idea of how one might compare different flux types across these factors, enabling prioritization of certain features over others for a particular application.

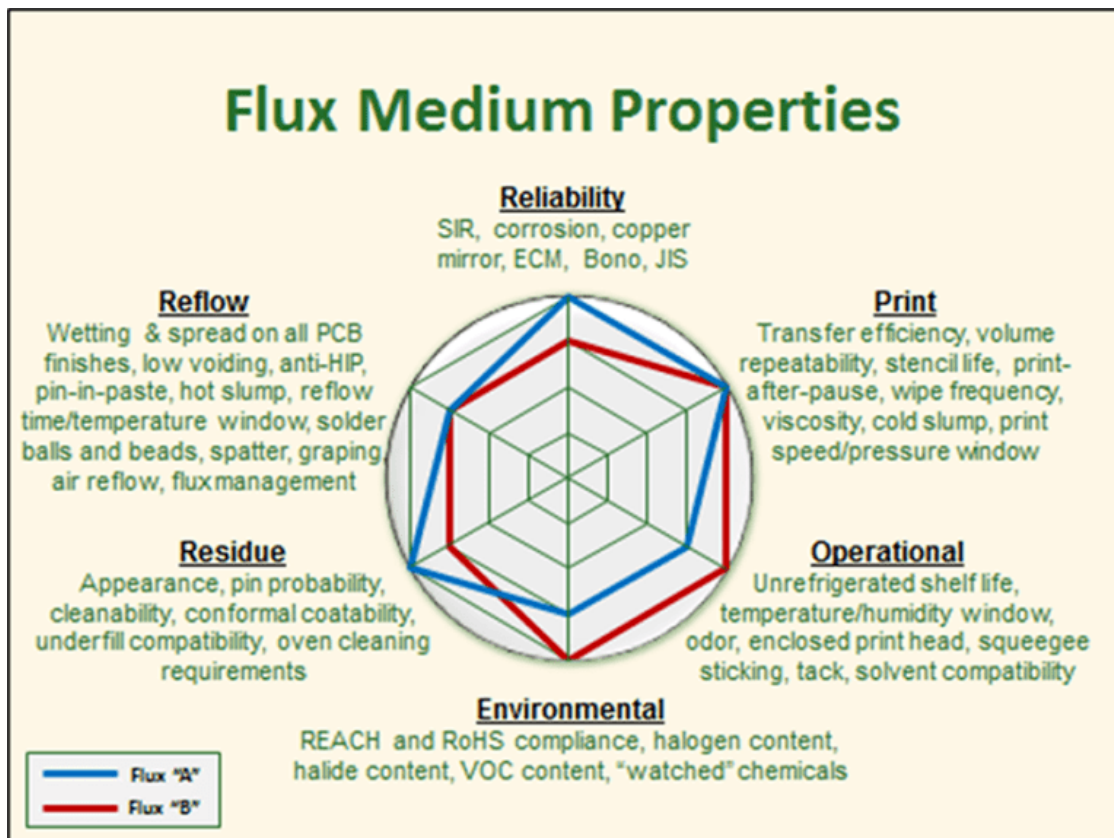



Figure 1. Radar chart of flux medium properties.

Staying Within the Assembly Process Window

The choice of substrate, components, solder paste, stencil, and more determines how wide or narrow a particular assembly process window is. While it is often a good idea to make choices that keep the window as wide as possible to account for variations, this must also be balanced with the constraints of the application. Steps to follow to navigate this crucial balancing act include:

1. **Develop a comprehensive understanding of requirements.** This includes the nature of the components, the types of PCB materials involved, and the environmental conditions in which the assembly will operate.
2. **Consider solder alloy options.** The melting point of the solder should align with the limits of the components and substrate. This includes accounting for extra heating that may be needed for regions of high thermal mass.
3. **Consider flux medium options.** A well-balanced flux can significantly impact the wetting behavior and the integrity of the solder joints. Consider the activity level, the residue characteristics, and the electrochemical reliability of the flux.
4. **Select the right solder paste.** After considering the alloy and the flux medium separately, it is important to dig a little deeper and ensure that the resulting solder paste is known for consistency and reliability. Variations in paste composition can lead to a wide range of assembly issues, making it crucial to choose products from reputable manufacturers known for maintaining high standards.
5. **Evaluate solder paste performance.** Because the final interaction of the paste with the process can lead to unanticipated outcomes, evaluate the paste's performance in your production environment. Measure the volume of solder paste deposits, assess the voiding percentage, and look for other defects after reflow. Examine any residue left by the flux to ensure it meets specifications and can be cleaned if necessary.
6. **Adjust as needed.** Finally, adjust process parameters until desired results are obtained.

Mastering the assembly process window helps optimize solder paste applications. By understanding the interplay between paste properties and the broader assembly environment, professionals can enhance flexibility, reduce defects, and maintain a high standard of efficiency and reliability. 

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Lean Philosophy and EMS Realities

Non-value activities are sometimes unavoidable.

ONE CHALLENGE FOR electronics manufacturing services (EMS) providers implementing Lean manufacturing practices can be customer buy-in. While an original equipment manufacturer (OEM) can design a process with minimal non-value-added activity, customer requirements may revive some necessary non-value-added activity and it is up to the EMS provider to find a compromise that satisfies the customer requirements while minimizing the cost of resources associated with the non-value activity.

A recent example of this occurred in SigmaTron International's Chihuahua, Mexico, facility. A consumer product customer added conformal coating to a product experiencing field failures related to operating environment issues. An automated selective coating machine is used that controls conformal coating deposition areas and application thickness. The customer wanted an automated visual inspection step added to ensure any overspray or missed coating was caught.


From a Lean perspective, the inspection step is a non-value-added process, particularly given the level of spray control associated with the selective coating machine. It was a customer requirement, however. The EMS provider's team evaluated available off-the-shelf automated optical inspection equipment and found that most had more inspection functions than the customer required and the process cost would exceed the customer's target price.

The compromise was to develop a proprietary automated visual inspection system that incorporated only the inspection functions the customer required. The cost of this system was less than one-tenth of the cost of an off-the-shelf system. While off-the-shelf systems were faster, the customer only required inspection based on a sampling plan consistent with IPC-A-610 workmanship requirements, thus only a portion of the 3,000 units per day would undergo inspection, making slower throughput an acceptable option, particularly given the cost differences.

The systems were validated using a measurement system analysis (MSA) which included a Gage repeatability & reproducibility (R&R) study. The goal of an MSA is to quantify measurement uncertainty and determine whether a system's accuracy, precision and stability is consistent with requirements. In this MSA, three appraisers performed three trials on a sample size of nine units. The characteristic evaluated was the percentage of conformal coating coverage on the studied samples.

To support the analysis, the team created a statistical process control (SPC) plan to determine whether the measurement data fell within control limits. The analysis looked at repeatability in terms of equipment variation to determine whether the machine consistently achieved the same results. It also looked at reproducibility in terms of

appraiser variation to determine if results changed if machine operators changed. Gage R&R studies were conducted to determine the amount of uncertainty within the measurement system. The impact of part variation was also studied. The data showed that the system's ability to discriminate among samples was acceptable across all samples and all appraisers.

The end-result of this example is a compromise that gives the customer exactly what they required at a cost aligned with acceptable pricing. While a non-value-added activity, it eliminates the variability found with manual inspection and requires minimal resources. It also helps ensure that any system variability found in the selective coating machine, such as issues driven by tooling wear or coating buildup, will be identified early. Consequently, the automated inspection step contributes to eliminating the waste of defects. 

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PCD&F

EASYLOGIX PCB-INVESTIGATOR V15.1 ECAD

PCB-Investigator V15.1 brings enhanced import/export functions, advanced analysis tools and a more user-friendly interface to streamline the PCB design process. Key features include enhanced import and export functions for various file formats and faster data handling, advanced thermal simulation and improved DfM checks, more UI options and improved reporting tools, and enhanced support for machine formats to streamline manufacturing processes.

EasyLogix

pcb-investigator.com



PASTERNAK IMPEDANCE-MATCHING PADS

Impedance-matching pads for 50Ω and 75Ω transmission lines are said to provide seamless transition between the two types of lines. Ensure optimal performance across a variety of RF applications and feature BNC, F-type, N-type, and SMA connectorized designs, making them versatile for integrating into existing systems with ease. Facilitate 50Ω to 75Ω impedance matching as well as 75Ω to 50Ω, catering to a broad spectrum of transmission requirements. Feature configurations including 50Ω BNC to 75Ω F-type among various gender setups, and combinations like 50Ω N-type male to 75Ω F-type male, and 50Ω SMA male to 75Ω F-type female to solve diverse connectivity challenges.

Pasternack

pasternack.com



STACKPOLE RNWA THIN FILM RESISTOR

Stackpole's RNWA is a thin -film chip resistor with wide terminations and is capable of tolerances to 0.1% and TCR as low as 25ppm. Is automotive grade, which provides an additional level of long-term stability and reliability as well as being resistant to sulfur.

Stackpole Electronics

seielect.com

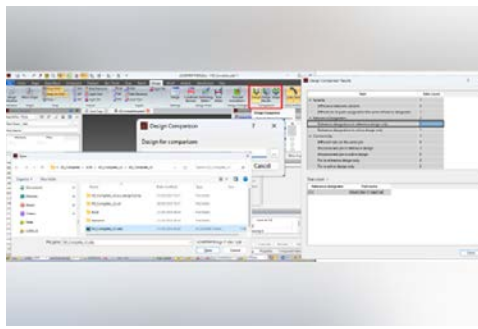


VISHAY DRALORIC AC05 WSZ AND AC05-AT WSZ RESISTORS

Vishay Intertechnology's Draloric AC05 WSZ and AC05-AT WSZ resistors feature a lead form permitting them to function as surface mount components. Serve as snubber and inrush current limiting resistors, and are said to be useful in automotive and industrial electronics, energy meters, and power supplies for white goods. Peak power capabilities up to 5kW for a 1 μ s pulse load and resistance range from 0.10 Ω to 10k Ω . Also feature a robust, nonflammable silicone cement coating that meets UL 94 V-0 standards. Operate within a temperature range of -55° to +250°C and are withstand mechanical stress and thermal shocks at high temperatures. Conform to RoHS compliance, are halogen-free, and feature tin-plated terminations, ensuring compatibility with lead-free and lead-containing soldering processes.

Vishay Intertechnology

vishay.com



ZUKEN ECADSTAR 2024.0 ECAD

eCADSTAR 2024.0 PCB design system includes improvements ranging from enhanced design reuse, simplified revision tracking and more robust schematic design. Introduces a comprehensive design comparison capability that allows designers to easily identify differences between two PCB or schematic designs, and a shape comparison tool to aid in reverse engineering efforts by highlighting discrepancies in copper and routing patterns. Also includes new "Copy Complete Part" feature that allows designers to transfer a component, along with its comprehensive set of data including PCB footprint, schematic symbol, padstacks, and 3-D model, from a customer-specific or prototype library to a central library directly to a customer-specific library in a single action. Schematic updates include support for variant text, optimized drawing of nets and buses, and the introduction of new design rule checks (DRCs) to help identify potential problems early on and streamline the design process, reduce overall design time, and minimize the need for revisions.

Zuken

[zuken.com](https://www.zuken.com)



CA



ASMPT SIPLACE CA2 PLACEMENT MACHINE

Siplace CA2 hybrid placement machine combines semiconductor and SMT production to integrate the production of SiPs (system-in-package modules) directly into the SMT line. Processes both SMDs from tapes and dies taken directly from the wafer in a single step at speeds of up to 50,000 dies or 76,000 SMT components per hour with a precision of up to 10µm at 3σ. Features a buffer storage module that works similar to a placement head and can hold

16 new dies (plus four on the flip unit) while the placement head itself is still placing SMDs. Also features full single-die-level traceability, which automatically logs for each die its pick-up and placement position on the board, as well as speedy program and product changeovers, placement program portability to any machine of the same type, and fast and comprehensive substrate mapping.

ASMPT

asmpt.com



AVEN HIGH-PERFORMANCE DIAGONAL CUTTERS

Aven's diagonal cutters are crafted for cutting and longevity for a range of industrial tasks. Titanium diagonal cutter is made with high-grade titanium. Features an overall length of 150mm and a semi-flush blade type, an oval head with a 22mm width, and cuts low carbon steel wire up to 1.6mm in diameter and soft copper wire up to 2mm. Features a lightweight design and a comfortable plastic grip to reduce hand fatigue for extended use without discomfort.

304 stainless steel cutter is designed for various cutting applications and offers a semi-flush cutting edge able to cut low carbon steel wire up to 1.6mm in diameter and soft copper wire up to 2mm. Features ergonomic PP+TPR grip to ensure comfort during use, and oval head style and 200mm overall length are said to provide control and leverage.

Aven

aventools.com



DYMAX UVCS V3.0 LED CONVEYOR

UVCS V3.0 LED conveyor is an enhanced version of the Dymax UVCS conveyor curing systems. Includes high-contrast 8" touchscreen for managing speed, operation modes, and LED emitters installed in the conveyor. Is fully programmable for belt speed and intensity and features a static curing oven mode in addition to high-speed conveying through the conveying tunnel, and a PLC can also be used to activate and operate the system. Features 12"-wide belt, automated part sensing and reversible operation. Fully enclosed design enhances safety with UV leak protection, and high-power exhaust system minimizes noise, light and heat emissions. Is said to reduce chamber temperature even with high-power curing systems, for temperature-sensitive parts, and includes stainless steel components near the belt to limit ESD.

Dymax

dymax.com



EMIL OTTO ZINNIN GREEN PASTES

Zinning Green pastes do not require zinc chloride, are not subject to hazard labeling, and can be used for soft soldering and tinning. Come in three variants with different alloys: Zinnin Green I with the alloy Sn100, Zinnin Green II with the alloy Sn96.5 Ag3.0 Cu0.5 (SAC305) and Zinnin Green III with the alloy Sn97Cu3. For use in both industrial and craft applications and come in various packaging sizes.

Emil Otto

emilotto.com



INDIUM DURAFUSE HR ALLOY

Indium's Durafuse HR solder paste alloy is said to deliver enhanced thermal cycling performance and superior voiding performance without vacuum reflow, especially for high-reliability automotive applications. Is engineered to withstand 3,000-plus thermal cycles at -40°/125°C across different PCB finishes and component types, and reportedly outperforms SAC 305 with bottom-terminated component voiding. Also offers reduced solder joint cracking and increased shear strength. Is compatible with most SAC 305 reflow profiles and standard PCB surface finishes, including ImSn, OSP, and ENIG.

Indium Corp.

indium.com



MASTER BOND UV15DC80-1MED EPOXY

UV15DC80-1Med is a one-component, no-mix epoxy that offers a dual cure mechanism utilizing UV light for initial fixation followed by heat for complete polymerization. Addresses limitations of traditional UV adhesives by effectively curing shadowed areas that wouldn't receive sufficient UV exposure, making it suitable for intricate parts and complex geometries, and meets ISO 10993-5 cytotoxicity standards, demonstrating biocompatibility for medical device applications. Is said to resist radiation, liquid sterilants and autoclaving. Has a moderate viscosity of 20,000-40,000cps for versatile dispensing and delivers strong bonds to various substrates, including metals, glass, ceramics, and many plastics, with a tensile strength exceeding 5,000psi at 75°F. Offers a wide service temperature range from -80° to +350°F (-62° to +177°C) and a glass transition temperature of 125°-135°C, and maintains optical clarity with a refractive index of 1.52 at 589nm. Exhibits minimal sensitivity to oxygen, and initial UV cure/tack can be achieved in seconds with UV light (325-365nm) at a minimum UV radiation intensity of 20-40mW/cm² while areas with limited UV access need to be subsequently cured with heat at 80°C within 40-60 min. Post-cure at 80°C for 2-4 hr. or 125°C for 30-60 min. is recommended for maximum performance.

Master Bond

masterbond.com



POLAR INSTRUMENTS GRS550 FLYING PROBE TESTER

GRS550 flying probe test system is designed for fault diagnosis in prototype construction, new product launches, small series and applications for which a traditional in-circuit test or multi-pin flying prober is too expensive. Offers extensive testing options with short preparation times and low costs through the extensive use of CAD data in combination with proven fault diagnosis technology. Is suitable for all component technologies and features a maximum fly height of 100mm. Includes two live video cameras, with one camera for programming and inspection and the second for live monitoring of the probing position, which enables diagnosis of faults in all component technologies such as SMT, PTH and BGA, with the system automatically positioning test points on accessible areas of the nets.

Polar Instruments

polarinstruments.eu



SHENMAO PF918-P250 SOLDER PASTE

PF918-P250 thermal fatigue-resistant solder paste is formulated with high-strength solder material, designed for long-service life electronic products with stringent reliability requirements. Incorporates high-reliability lead-free alloy PF918, which boasts a tensile strength performance 1.4 times greater than the typical SAC 305. Is said to reduce voids, have good printability and demonstrate thermal cycling reliability.

Shenmao

shenmao.com

TOPLINE BRAIDED SOLDER COLUMNS

Braided solder columns are designed to serve as a drop-in replacement for solder spheres used in BGA components. Are said to be suited for cryogenic environments and next-generation applications, and provide improved reliability and thermal properties over competing technologies. Are non-collapsible, RoHS compliant and lead-free, and designed to absorb destructive strain caused by differences in CTE of materials between large-sized heterogeneous 2.5-D packages and FR-4 PCBs.

TopLine

topline.tv



In Case You Missed It

Components

“How a Simple Circuit Could Offer an Alternative to Energy-Intensive GPUs”

Author: Sophia Chen

Abstract: On a table in his lab at the University of Pennsylvania, physicist Sam Dillavou has connected an array of breadboards via a web of brightly colored wires. The setup looks like a DIY home electronics project – and not a particularly elegant one. But this unassuming assembly, which contains 32 variable resistors, can learn to sort data like a machine-learning model. The potential energy savings works this way: Digital chips like GPUs expend energy per operation, so making a chip that can perform more operations per second just means a chip that uses more energy per second. In contrast, the energy usage of his analog computer is based on how long it is on. Should they make their computer twice as fast, it would also become twice as energy efficient. While its current capability is rudimentary, the hope is that the prototype will offer a low-power alternative to the energy-guzzling graphical processing unit (GPU) chips widely used in machine learning. (*MIT Technology Review*, Jun. 5, 2024, <https://technologyreview.ae/source/how-a-simple-circuit-could-offer-an-alternative-to-energy-intensive-gpus/>)

PCB Reliability

“Numerical Simulation Approach for Consideration of Ageing Effects in PCB Substrates by Modifying Viscoelastic Materials Properties”

Authors: Marius van Dijk, *et al.*

Abstract: During operating time of electronic systems, the materials used in such devices are potentially subjected to aging effects, which might limit the lifetime. Therefore, knowledge about the materials and the way they are affected by aging effects is of key importance to develop reliable products. This study discusses a simulation approach that can consider aging effects caused by oxidation at elevated temperature of a printed circuit board material, typically used for high-frequency applications. The material was characterized for its thermomechanical properties with state-of-the-art techniques for different aging durations. Aging was accelerated by storing the samples in an oven at 175°C for up to 1000 hr.

Within the simulation workflow, the thermomechanical properties of the different aged states are defined by modifying the pristine viscoelastic properties. Four exponential functions are derived modifying the initial modulus,

the characteristic time constants, the shift function and the coefficient of thermal expansion, all in dependency of aging time.

To demonstrate the approach, the soldered interconnection lifetime of a theoretical chip-size-package on a printed circuit board is studied. State-of-the-art lifetime predictions of such interconnections only include thermomechanical aging effects, for example by creep effects of the solder. By additionally considering the aging of the printed circuit board, thermal aging is combined with thermomechanical aging.

Results in the soldered interconnection are compared between either considering additional aging effects of the printed circuit board or neglecting this behavior. Thus, it is shown that thermal aging plays a significant role in the development of accumulated creep strain which becomes increasingly important with increasing expected lifetime. (*Microelectronics Reliability*, June 2024, <https://www.sciencedirect.com/science/article/pii/S0026271424000830>)

Recycling

“Efficient and Selective Gold Recovery using Amine-Laden Polymeric Fibers Synthesized by a Steric Hindrance Strategy”

Authors: Youngkyun Jung, *et al.*

Abstract: Various alkylamines are commonly used for efficient Au recovery; however, their high hydrophilicity can result in dissolution in water, hindering effective Au recovery and potentially causing environmental contamination. Currently, the forms in which alkylamines are immobilized on supports provide unsatisfactory Au recovery capabilities and exhibit low structural stability. This study proposes a pragmatic approach for synthesizing amine-laden polymeric fiber (ALPF) adsorbents with efficient Au recovery capabilities and superior structural stability. Polyacrylonitrile fibers (PANF) were employed as a supportive matrix to immobilize the alkylamine molecules chemically. The densely grafted amine groups on the ALPF adsorbed significant amounts of Au ions and reduced them to Au(0) crystals. This chelation–precipitation hybrid method achieved a Au recovery efficiency of nearly 100% over a wide pH range of 1–4. In addition, it demonstrated an exceptional Au adsorption capacity of 1463 mg/g, surpassing the values reported for other adsorbents categorized by size and shape. Even in the presence of 14 different coexisting metal ions, the ALPF showed a Au recovery efficiency above 99.9%. It also exhibited excellent reusability, maintaining a Au recovery rate of ~91% after 10 cycles. Furthermore, fibrous adsorbents alleviated the pressure drop in columns filled with adsorbents, thereby enabling energy-efficient and environment-friendly processes. (*Chemical Engineering Journal*, March 2024; <https://doi.org/10.1016/j.cej.2024.149602>)

Solder Materials

“Effect of Ce and Sb Doping on Microstructure and Thermal/Mechanical Properties of Sn-1.0Ag-0.5Cu Lead-Free Solder”

Authors: Fang Liu, *et al.*

Abstract: This study investigated effects of Ce and Sb doping on the microstructure and thermal mechanical properties of Sn-1.0Ag-0.5Cu lead-free solder. The effects of 0.5%Sb and 0.07%Ce doping on microstructure, thermal properties and mechanical properties of Sn-1.0Ag-0.5Cu lead-free solder were investigated. According to the mass ratio, the solder alloys were prepared from tin ingot, antimony ingot, silver ingot and copper ingot with purity of 99.99% at 400°C. X-ray diffractometer was adopted for phase analysis of the alloys. Optical microscopy, scanning electron microscopy and energy dispersive spectrometer were used to study the effect of the Sb and Ce doping on the microstructure of the solder. Then, the thermal characteristics of alloys were characterized by a differential scanning calorimeter (DSC). Finally, the ultimate tensile strength (UTS), elongation (EL.%) and yield strength (YS) of solder alloys were measured by tensile testing machine. With the addition of Sb and Ce, the β -Sn and intermetallic compounds of solders were refined and distributed more evenly. With the addition of Sb, the UTS, EL.% and YS of Sn-1.0Ag-0.5Cu increased 15.3%, 46.8% and 16.5%, respectively. The EL.% of Sn-1.0Ag-0.5Cu increased 56.5% due to Ce doping. When both Sb and Ce elements are added, the EL.% of Sn-1.0Ag-0.5Cu increased 93.3%. The addition of 0.5% Sb and 0.07% Ce can obtain better comprehensive performance, which provides a helpful reference for the development of SAC lead-free solder. (*Soldering & Surface Mount Technology*, May 2024,

<https://www.emerald.com/insight/content/doi/10.1108/SSMT-08-2023-0044/full/html>) 

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