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FEATURES

HIGH-SPEED DESIGN

Fundamentals of Signal Integrity at Various Frequencies

PCB designers use CAD tools or the internet to find best practice techniques for designing at different frequencies, but they may not understand the fundamentals behind signal integrity or miss lesser-known techniques. An exploration of board-level tips and a discussion of fundamentals from lower-speed designs to gigabit-level speeds.

by ANDREW GONZALES and JASON METZNER

SIR TESTING (COVER STORY)

Dendrite Growth Dynamics

With the growing prevalence of high-voltage electronics seeing daily use by consumers, the reliability of those electronics is increasingly important – including the question of whether they should be tested at those elevated voltages or whether the conventional 5V SIR test is adequate. To answer that question, a series of tests was conducted to understand how higher voltages and contamination affect dendrite growth on a SIR test coupon.

by ADAM KLETT, PH.D.

AQUEOUS CLEANING

Water Quality Matters

Aqueous cleaning in PCB assembly requires particular attention to water quality to minimize the risks of contamination of the board, with ion exchange being the technology of choice to purify and recover the water. Ion exchange systems typically require manual monitoring or timed changing of water tanks to maintain quality, and a case study is presented using an ion exchange system with remote monitoring capabilities to reduce water usage and minimize manual monitoring.

by CHRISTOPHER T. RILEY

BOARD QUALIFICATION

Identifying Solder Mask Problems with Simple Tests

Solder masks can face several issues that can lead to complications like micro solder balling, bridging and solder snail trails, which could compromise PCB quality and long-term reliability. To prevent significant production rework and increased costs, a few simple tests are presented that an engineer can perform on the shop floor.

by TIMOTHY O'NEILL

ON PCB CHAT (PCBCHAT.COM)

PCB Chat

SMTA INTERNATIONAL PREVIEW
with JASON KEEPING, JEFF KENNEDY and ROBERT BOGUSKI

SUPPLY CHAIN MANAGEMENT
with ZACHARY FEUERSTEIN

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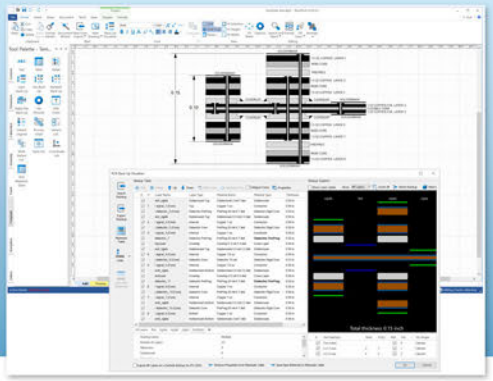
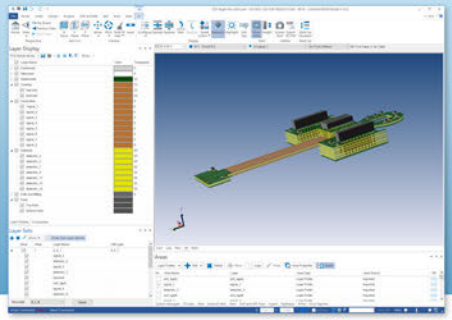
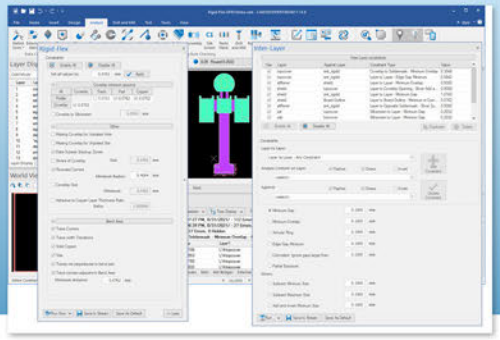


Use Stack Up Visualizer and Blueprint's Rigid-Flex Stackup template to easily manage and document rigid-flex stackups.



A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



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PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by Printed Circuit Engineering Association, Inc., PO Box 807 Amesbury, MA 01913. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

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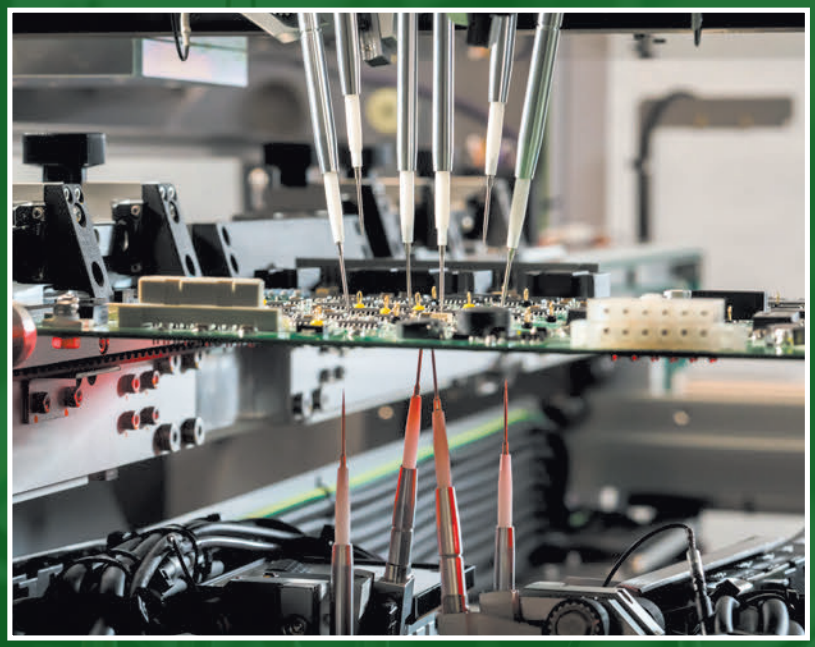

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Let's Get Small

ULTRA-HIGH-DENSITY INTERCONNECTS ARE more smoke than fire right now, but they won't be that way for long. Driven by high-density BGAs and RF products, UHDI is finding its way into the mainstream.

Given the number of conferences, webinars and the like, readers would be forgiven if they thought UHDI was already standard, however.

First, of course, means agreeing on what, exactly, UHDI is. The working definition of UHDI is product with line widths and spaces of fewer than 50 microns, dielectric thickness of less than 50 microns, and a microvia diameter of less than 75 microns. That's not a standard definition – yet – and the lower lever parameters have yet to be defined. At some point, there stands to be overlap with semiconductor technology. Stay tuned as the definition evolves.

I am reminded – to a degree – of the chaos surrounding UHDI's (slightly) larger cousin, high-density interconnects, which hit widespread production in the late 1990s (although the original concept dates much earlier). Then, the issues could be boiled down to two:

- Which process to use: etch or drill (and if drill, mechanical or laser)?
- The demand signal.

As to the former, some of the processes of the day included photovia, plasma etching and the eventual winner, laser. As to the latter, time will tell as to the ultimate market size, but orders are already coming.

It's mostly lost to history now, but not every company banked on laser at the start. Motorola, for instance, produced millions of boards using a sequential build HDI process that mated photoimageable dielectrics and semiadditive copper metallization on a PWB substrate.

And even fewer companies – or regions, really – saw the need. North America and Europe were all about big boards in those days. Japan controlled IC substrate production. Taiwan and especially China were still relatively marginal players. Still, the signs were ominous. Key industry observers were already piping up that investment in microvia formation, specifically in laser drills, was needed.

The West wasn't listening. Indeed, upon seeing the buoyant forecasts for the PCB industry in North America for the early 2000s, I recall Jack Fisher, then the CTO of the Interconnection Technology Research Institute, remarking that it would be years before Americans started pursuing HDI. How right he turned out to be. And when the major telecommunications and IT companies started canceling orders en masse for their so-called "surfboards," the Western

PCB shops weren't left with much to fall back on.

Asia, on the other hand, led by Taiwan and Japan, invested heavily on leading-edge drilling capacity. Today, we all know the Pacific Rim dominates high-end PCB fabrication.

Could the script be flipped? Unlike with HDI, additive fabrication processes look like they will have a significant role in UHDI. It's unlikely a single solution will dominate.

We have a long way to go to mainstream this technology. IPC task groups are working on various specifications for fabrication and qualification, among others. Designers need to understand component choices, signal integrity implications, impedance matching, and thermal management. Assemblers will have to master the use of smaller powder sizes, different stencils, and so forth.

According to John Johnson at American Standard Circuits, one of the handful of PCB fabricators in the US capable of UHDI production, when lines and spaces reach less than 25 microns, UHDI is needed. To be sure, that's really small. But while conventional technology will continue to have a long runway, those who master UHDI will be better-positioned to take advantage of the smaller, thinner, lighter products consumers of all stripes demand.

A special free panel on UHDI at PCB West this year will outline the basic various ways UHDI processing takes place, and to help designers and design engineers understand how their decisions might affect yield. Among the panelists are Michael Gleason of GreenSource Fabrication; Meredith Labeau of Calumet Electronics, Anaya Vardya of American Standard Circuits/Sunstone, and Jay Vyas of SigmaTron International.

The panel takes place at the Santa Clara Convention Center on Oct. 9 from 9-10 a.m. We invite all our readers to join us for this and several other free sessions that day, and to take in the more than 100 leading electronics design, fabrication and assembly companies on hand during the one-day exhibition.

See you at the show!

mike@pcea.net
@mikebuetow

P.S. The video from our forum on UHDI & Substrates: From Design to Package will be available at PCEA.net later this month. Also, a series of videos on printed circuit board design will be available on our YouTube channel.

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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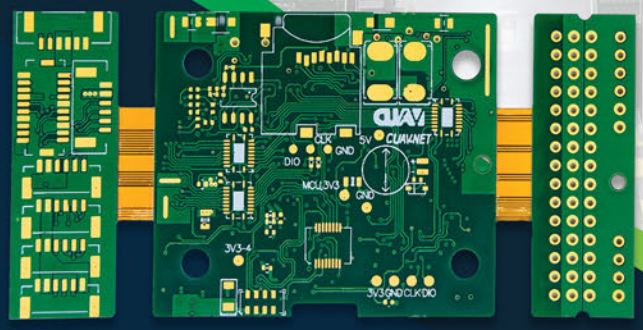

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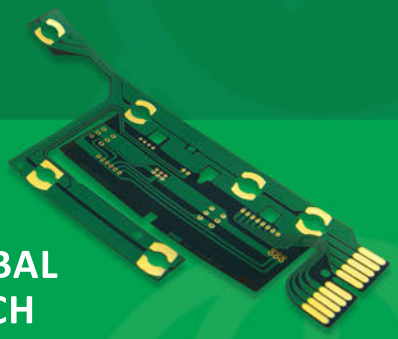

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Jedec Releases Plans for Memory Module Standards

ARLINGTON, VA – Jedec has announced upcoming standards for advanced memory modules designed to power the next generation of high-performance computing and AI applications.

The standards for DDR5 multiplexed rank dual inline memory modules (MRDIMM) and a next-generation compression-attached memory module (CAMM) for LPDDR6 are set to change the industry with unparalleled bandwidth and memory capacity.

DDR5 MRDIMMs offer an innovative, efficient new module design to enhance data transfer rates and overall system performance. Multiplexing permits multiple data signals to be combined and transmitted over a single channel, effectively increasing bandwidth without the need for additional physical connections and providing a seamless bandwidth upgrade to enable applications to exceed DDR5 RDIMM data rates. Other planned features include:

- Platform compatibility with RDIMM for flexible end-user bandwidth configuration
- Utilization of standard DDR5 DIMM components including DRAM, DIMM Form Factor & Pinout, SPD, PMIC, and TS for ease of adoption
- Efficient I/O scaling using RCD/DB logic process capability
- Leverage existing LRDIMM ecosystem for design and test infrastructure
- Support for multi-generational scaling to DDR5-EOL.

The Jedec MRDIMM standard is set to deliver up to twice the peak bandwidth of native DRAM, enabling applications to surpass current data rates and achieve new levels of performance. It maintains the same capacity, reliability, availability, serviceability (RAS) features as Jedec RDIMM. The committee aims to double the bandwidth to 12.8Gbps and increase the pin speed. MRDIMM is envisioned to support more than two ranks and is being designed to utilize standard DDR5 DIMM components ensuring compatibility with conventional RDIMM systems.

Plans are underway for a tall MRDIMM form factor to offer higher bandwidth and capacity without changes to the DRAM package. This taller form factor will enable twice the number of DRAM single-die packages to be mounted on the DIMM without the need for 3DS packaging.

As a follow-on to Jedec's JESD318 CAMM2 memory module standard, JC-45 is developing a next-generation CAMM module for LPDDR6 targeting a maximum speed greater than 14.4 GT/s. As planned, the module will also offer a 24-bit subchannel, a 48-bit channel and a connector array.

Both projects are in development in Jedec's JC-45 Committee for DRAM Modules. Jedec standards are subject to change during and after the development process.

Renesas Completes $5.9B Altium Acquisition

TOKYO – Renesas in August announced the successful completion of its $5.9 billion acquisition of Altium, which was first announced in February.

The combination sets the foundation for Renesas and Altium to create a common electronics system design and lifecycle management platform, Renesas said in a release. The platform will integrate and standardize various electronics design data and functions and enhance component lifecycle management, delivered in digital iterations.

"This is a historical milestone for both Renesas and Altium as we take another important step forward in bringing enhanced user experience for electronics system designers," said Hidetoshi Shibata, CEO, Renesas. "The integrated and open electronics system design and lifecycle management platform we aim to build together will make electronics accessible to broader market, for any enterprises regardless of their size or industry. I want to reaffirm that our commitment to upholding data security and compliance of the Altium customers will continue to be our top priority."

With the transaction now closed, Altium is now a wholly owned subsidiary of Renesas. Altium CEO Aram Mirkazemi has assumed the role of senior vice president and head of Renesas' Software & Digitalization. He concurrently serves as CEO of Altium.

"This is a pivotal moment for Altium and marks the beginning of an exciting future with Renesas," Mirkazemi said. "With Renesas' support and expertise, we are looking forward to accelerating the cloud-enablement of all industry processes associated with electronics design and development. This will make electronics accessible to a broader market and lay the foundation for software-defined products."

SIA Report Provides Recommendations for Domestic Semiconductor Growth

WASHINGTON – A new report from SIA and the Boston Consulting Group identifies five primary factors that impact investment decisions for semiconductor companies. "Attracting Chips Investment: Industry Recommendations for Policymakers" also lays out actionable recommendations for governments seeking to grow their domestic semiconductor industry.

Among the factors:

1. Investment and operational costs. Semiconductor development, in both design and manufacturing, is expensive. In evaluating site options, companies thoroughly analyze site-specific costs, including land, utilities, equipment, materials, labor, and taxes. Government support programs that are simple, flexible, and offset

construction and equipment costs are attractive to semiconductor investors.

2. Semiconductor companies require access to a large technical workforce. They seek countries where the education system and public-private partnerships coalesce to generate a rich talent pipeline—from technicians and skilled trades to Ph.D-level engineers and scientists. Governments that adopt comprehensive workforce development and labor policies to build an industry-ready talent pipeline will be well-placed to draw investment from the semiconductor industry and other strategic technology sectors.
3. Safe, reliable, and cost-efficient water, utilities, communications, and transportation infrastructure are critical for semiconductor operations. Small interruptions in operations can incur significant costs. Governments should invest in electricity grids that are able to maintain day-to-day stability, provide a portion of energy from green sources, and ensure communications and transportation networks are sufficient to support semiconductor industry needs.
4. Regulatory and trade environment. Semiconductor supply chains are concentrated in countries with market-friendly trade policies, and regulatory frameworks that respect intellectual property rights and trade compliance. Policymakers can facilitate semiconductor investments by implementing policies that minimize trade and permitting costs, streamline administrative processes, and facilitate the movement of semiconductor products and data.
5. Integrated ecosystems. Semiconductor companies thrive on vibrant ecosystems that cluster suppliers, customers, R&D partners, educational partners, and innovative talent.

Governments seeking to present their countries as a destination for semiconductor companies to invest must move quickly and deliberately to take advantage of this window of opportunity, mindful that other governments are competing for such investments, the report says.

The policy recommendations, if followed, can position countries to attract chip ecosystem investments that complement industry operations in the United States, and drive greater security, resilience, and diversification in global semiconductor supply chains, the report concludes.

Long Young to Build 2 Thai Factories

KUNSHAN, CHINA – Long Young Electronic has announced plans to invest CNY200 million ($28 million) to build two new factories in Thailand.

The Chinese supplier of electromagnetic interference shielding materials said it will spend up to CNY120 million ($16.8 million) on a composite copper foil plant and CNY80 million ($11.2 million) on an EMI shielding materials plant in Thailand's northern Chachoengsao province.

The company said the composite copper foil plant will take four years to construct and is designed to produce various types of products, targeting printed circuit board makers in Southeast Asia and other markets. The other factory will be built in three years with a production capacity of 62,400 sq. m. of conductive tape and 352 million EMI shielding and related materials a year.

To pay for the new facilities, Long Young said it will terminate a plan to build a new EMI shielding material plant and expand the capacity of an existing one in China and will suspend construction of a product research and development center.

Benchmark Expands Romanian Facility

TEMPE, AZ – Benchmark Electronics has opened an expansion at its Brasov, Romania, facility that more than doubles its manufacturing capacity in the region.

The EMS company said the expansion is intended to support customer-driven demand for access to high-technology manufacturing solutions, localized and global supply chains, and a customer-focused team committed to optimizing delivery, quality, cost, and manufacturing and engineering services. Key market sectors serviced include complex industrials, medical and semiconductor capital equipment.

"Benchmark Brasov, alongside Benchmark Almelo, serves as the heart and soul of our European operations and we are excited to expand our manufacturing footprint, add capacity to better serve our current customers, and support the high interest by new customers who are looking to regionalize their manufacturing in Europe," said Jeff Benck, president and CEO, Benchmark. "The new space will offer our manufacturing and engineering teams ample room to expand our operations in eastern Europe while also bringing more high-paying jobs to the Brasov community."

The expansion of Brasov is part of a broader company strategy to increase manufacturing capacity around the world by leveraging its current facilities and leadership as more customers look to diversify their manufacturing strategy and have products built closer to end-market consumption, the company said, and the new space not only provides new manufacturing space, but also improves system integration and workflow on the floor.

"It is an honor to welcome our partners, suppliers and the local community for the unveiling of our expanded Brasov facility," said Herman Bartelink, vice president of European operations, Benchmark. "We're looking forward to adding new capabilities and bringing more business and jobs to the region. This expansion has been a long time coming and I am very proud of the work of our European team in reaching this milestone."

Kimball Sells AT&M Unit to Averna

JASPER, IN – Kimball Electronics has completed the sale of its automation, test and measurement business to Averna, and said it plans to focus on its core EMS business.

The sale to Averna Technologies closed on Jul. 31, with proceeds from the transaction being used for support of organic growth, debt reduction and share repurchases, Kimball said in a release. Financial terms of the sale were not disclosed.

Kimball entered the automation, test, and measurement industry with the acquisition of Global Equipment Services in 2018, and in May 2024 announced that the unit was for sale. The AT&M business provides advanced testing and

inspection solutions for manufacturers in the industrial, medical, consumer electronics, and semiconductor sectors.

“While we have made significant strides enhancing our capabilities in AT since the acquisition of GES, we determined that it is not a good strategic fit for Kimball and that focusing on core EMS operations aligns best with strategic priorities and longer-term growth opportunities for the company,” said CEO Richard Phillips. “AT will be well-positioned under new ownership with expertise in testing and measurement, broad industry knowledge, and established client relationships. We thank the team for their contributions and wish them success moving forward.”

“The addition of the GES team, and its footprint in Silicon Valley and Asia, is a perfect fit for Averna,” said Francois Rainville, CEO, Averna. “This will further strengthen our position as one of the worldwide leaders focused in automation, test and measurement. Now with 1,200 professionals spanning across the Americas, Europe and Asia, we can better partner with our global customers in all aspects of their product test requirements, wherever they are. We welcome our new teammates and are looking forward to this new chapter in Averna’s story.”

Meiko to Open Vietnam PCB Factory in 2025, Partners with Aoshikang

AYASE, JAPAN – Meiko Electronics is planning to begin production at its $100 million PCB factory in Vietnam in the second quarter of 2025.

According to project’s latest report, the company aims to finish construction of the factory by the third quarter of this year, install equipment during the end of the year and early 2025, recruit and train staff during the first quarter and enter official operation in the second quarter.

When finished, the factory will have an annual production capacity of 80,000 sq. m. The company also plans to build a second factory on the site, upping its total investment to $500 million. The factories will produce PCBs for peripheral devices, computers, electronic home appliances, audio-visual equipment, solar cells, microprocessor chips and controllers.

Meiko also announced a strategic business alliance with Aoshikang Technology to boost PCB production capacity in the ASEAN region.

Through the partnership, Meiko will invest $20 million for a 14.9% stake in ASK’s subsidiary, Jiaruian, to manage a new production subsidiary in Thailand. Meiko said the collaboration aims to meet increasing demand and will have a negligible impact on its current fiscal year business results.

Bain Capital to Acquire Italian PCB Maker Somacis

LONDON – Private investment firm Bain Capital has announced the acquisition of a controlling stake in Somacis, an Italian PCB manufacturer, from Chequers Capital.

Chequers will reinvest into the company alongside the management team, led by CEO Giovanni Tridenti. Other terms of the deal were not disclosed.

Somacis was founded in 1972 and specializes in high-mix/low-volume, and mission-critical PCBs. The company serves various high-performance markets such as aerospace & defense, MedTech, and data centers/AI, among others, and operates across the full value chain, offering R&D prototyping, ramp-up and end-to-end production. The company has a global footprint composed of five facilities in Europe, North America and Asia.

"Given its strength in the market, Somacis is well-positioned to benefit from sustainable long-term reshoring tailwinds which increase the demand for PCBs manufactured in the US and EU," said Ivano Sessa, partner and co-head of European Industrials, Bain Capital. "We are pleased to back one of the leaders in its field."

"I would like to thank Chequers for their valuable partnership and outstanding work over the past years and am pleased that they will remain invested alongside our fully committed management team as we are joined by Bain Capital," said Tridenti. "We are excited for Bain Capital to bring its expertise in international development and operational capabilities to further enhance our global reach and help us fulfil our long-term ambitions, which are underpinned by a mix of organic and inorganic strategic growth initiatives, and on the strengthening of the value-add proposition to our customers."

"Over the past years, we have worked alongside the Somacis management team to strengthen the company's operations and positioning and to make strategic acquisitions," said Philippe Guérin, managing partner, Chequers Capital. "We are very pleased to reinvest alongside Bain Capital and such an excellent management team with the goal to become the number one global player in our segment."

SEMI Publishes Recommendations on Outbound Investments

BRUSSELS – SEMI has published recommendations to advance the European semiconductor industry in response to the European Economic Security Strategy.

The European Commission has outlined the nonbinding roadmap to monitor outward investment transactions with the goal of preventing technology and knowledge leakage in four critical technology areas tied to advanced semiconductor technologies.

The SEMI Europe Recommendations on Outbound Investments outline the association's position and strongly encourage all policymakers involved to carefully consider the following key recommendations:

- Ensure that European semiconductor companies are as free as possible in their investment decisions to avoid losing their agility and relevance across global markets.

- Adopt a pragmatic risk-based approach to comprehensively assess which outbound transactions related to advanced semiconductor technologies could result in technology leakage for dual-use purposes.
- Provide further clarification on how any potential measures would affect intra-company investments and relations with non-EU subsidiaries, given the international exposure of semiconductor companies.
- Develop an approach to outbound investments that effectively contributes to greater economic security through close consultations between European institutions, member states, and all relevant industry stakeholders.
- Maximize the synergies and positive feedback effects that the semiconductor supply chain has in increasing competition, cross-border investments and transnational collaboration.

The recommendations emphasize the need for the European Commission to adopt a positive approach to economic security that recognizes the crucial role of cross-border investments for the functioning and prosperity of the European semiconductor industry, to guarantee its companies have a high level of agility and market access at the global level.

"Within our industrial ecosystem, outbound investments are regarded by the vast majority of SEMI members as essential to scale production, expand capabilities, access emerging markets, and engage in innovative partnerships," said Laith Altimime, president of SEMI Europe.

SEMI will continue to engage with relevant stakeholders to contribute to the political debate and encourage a legislative framework that can enhance economic security across industrial supply chains while preserving Europe's technological competitiveness.

ECIA Guide Advises Approved Channel Buying

ATLANTA – An Electronics Component Industry Association (ECIA) committee in August released an advisory to use only the authorized channel to procure electronic components. With the double threat of a steep rise in bad actors with new tools to sell fake components, combined with more frequent supply chain disruptions, it is an especially critical time to be vigilant, the trade group's Global Industry Practices Committee (GIPC) said.

The GIPC Guideline, "The Risks of Buying Components Outside the Authorized Channel," is available from the trade group's website.

"These guidelines spell out the specific risks taken when going outside the safety of the authorized channel to buy electronic components," explained Don Elario, ECIA Vice President of Industry Practices. "We urge customers to seriously consider the consequences that can occur when a counterfeit component infiltrates their BOM: catastrophic failure, brand damage, liability, and so on. Our document contrasts those risks with the assurances that come from the authentic chain of custody from the component manufacturer through the authorized channel."

Bank Exits Welsh Electronics Manufacturer After Funding Buyout

TREDEGAR, UK – The Development Bank of Wales has exited Camtronics six years after funding a management buyout of the contract electronics manufacturer.

In 2018, the Development Bank's Wales Management Succession Fund Investment Fund invested £450,000 ($584,000) in the company to enable managing director Paul Macleur, alongside colleagues Chris Gulliford and Linda Sterry, to lead a management buyout from Photonstar, who had purchased the company in 2011.

The Development Bank also introduced non-executive director Mark Pulman to the company at the time, and since the buyout, Camtronics' turnover has doubled to £4 million ($5.2 million).

"As we embark on the next stage of our growth, the time was right to reflect on how the support of the Development Bank has enabled us to build a strong foundation for the future," said Macleur. "We have enjoyed the benefit of having an excellent working relationship with the team who have stood by us throughout, offering guidance and significant support in addition to funding. Together with Mark, they have helped with our strategic planning and long-term value creation which means that we are now in a position to buy them out. As the sole owners of the business, we are now well-placed to move forward and continue to grow our industry-leading services."

Camtronics offers a full range of electronics manufacturing services and has 38 employees. Services include SMT assembly, AOI, through-hole assembly, box build, programming and testing.

PCD&F

Altair signed a memorandum of understanding with the **University of Nottingham** for a digital twin project within the aerospace sector and worked with **LG Electronics Vehicle Component Solutions** to create analysis solutions aimed at increasing product lifespans using Altair's HyperWorks platform.

Bestec Group plans to invest INR200 crore ($24 million) in a new manufacturing unit near Bengaluru, India.

Brandner PCB, an Estonian PCB manufacturer, will shut down its operations at the end of November.

IEEE TryEngineering partnered with **Keysight Technologies** to develop lesson plans focused on electronics and power simulation.

Elite Material and **Zhen Ding** have signed a strategic cooperation agreement to collaborate research of copper-clad laminates.

ISU Petasys will invest KRW300 billion ($223 million) in Daegu, Korea, to build a PCB manufacturing plant.

Jingguo Thailand's PCB plant will be sold to Tongye Shenghong Technology Group for about $23 million.

OurPCB USA opened a new office in Sierra Madre, CA.

Siemens and **BAE Systems** announced a collaboration to accelerate digital innovation in engineering and manufacturing technologies.

Sumitomo Electric Industries will invest an additional $27.4 million in two projects for manufacturing flexible circuit boards in Vietnam's capital city of Hanoi.

TTM Technologies plans to start construction this year on a plant near Syracuse, NY.

Ultra Librarian announced a partnership with **Footprintku AI** to enhance DfM capabilities across its CAD library.

Yang Xuan Electronics began construction on a $120 million PCB plant in Vietnam with an expected opening by the end of 2025.

Zhen Ding Technology has been granted a patent for a covering film that includes a thermal conductive layer sandwiched between a covering layer and an adhesive layer.

CA

Anda Technologies appointed **Tech Gear Ltd.** distributor in Hungary.

Ascentron installed **Ersa** i-CON 1 MK2 hand soldering equipment.

Avalon Technologies announced the expansion of its PCB assembly and design services.

Axiom partnered with **Switchee** to create a platform of interconnected devices for social housing.

BTU International named **Repstronics** representative in Mexico and Central America.

Cofidur in August announced the acquisition of fellow French EMS **Seico.**

Dixon Technologies will open a new facility in Chennai for producing laptops for four leading notebook brands in India and is negotiating with several multinational electronics component companies to form joint ventures aimed at strengthening its position in component manufacturing.

Foxconn plans to invest CNY1 billion ($138 million) to construct a new business headquarters in Zhengzhou, China.

Havells India will invest INR800 crore ($95 million) for a new electronics manufacturing facility in the first phase of development for the first electronics manufacturing cluster in India's Uttar Pradesh state.

Hirose Electric added **Master Electronics** as an authorized dealer in the Americas.

India is hoping massive subsidies can help it establish a self-reliant semiconductor ecosystem.

Jabil will lay off 130 employees in Albuquerque later this year due to a "shift in customer demand" and completed the construction of a new production facility in Osijek, Croatia.

Jaltek is collaborating with **PP Control & Automation** to target new orders with UK organizations involved in indoor/vertical farming, automation, precision farming and remote sensing.

Kaynes Technologies in August inaugurated an advanced electronics manufacturing services unit near Hyderabad, India.

Nexperia installed **Essemtec's** Fox MFC pick-and-place system at its Stockport, UK, facility.

Nikon opened a 90,000 sq. ft. advanced manufacturing technology center in Long Beach, CA.

Nordson Electronics Solutions consolidated its European offices into one location in Valkenswaard, Netherlands.

Padget Electronics will start making **Google** Pixel smartphones in September.

Pico MES announced that all manufacturers will be able to use its digital work instruction suite of tools for free.

Plexus broke ground on its sixth manufacturing facility in Penang and said it is investing more than MYR1 billion ($215 million) in Malaysia over the next three years.

Poly Electronics is adding three AI-powered inspection machines to its manufacturing lines.

Rocka Solutions opened a new entity in Canada to better serve its customers and expedite the delivery of import products across the nation.

Semi-Kinetics installed three **Koh Young** Zenith 2 3-D AOI systems and an **Epilog** Fusion Pro laser machine at its California facility.

SK Hynix will receive up to $450 million in direct funding and a loan of up to $500 million from the Commerce Department to support high-bandwidth-memory production and advanced packaging R&D in the US.

Tata Electronics started the construction of its INR27,000 crore ($3.2 billion) chip assembly plant in India that will produce more than 48 million chips per day.

TPV Technology will implement **Blue Yonder's** supply planning solution to increase supply chain efficiency, visibility and responsiveness.

TSMC has taken targeted measures to boost its support for Taiwan's domestic supply chain, reduce costs, and reduce the risks associated with foreign monopolies.

Turkey announced $30 billion in incentive packages to boost high-tech investment in the country, including $5 billion to build a semiconductor factory.

VS Industry secured new orders in the Philippines with an aggregate value of MYR1.5 billion ($338.5 million) over the next two financial years.

Zetwerk Manufacturing Businesses has announced a strategic partnership with **SMILE Electronics** to establish three new factories dedicated to IT hardware production in India.

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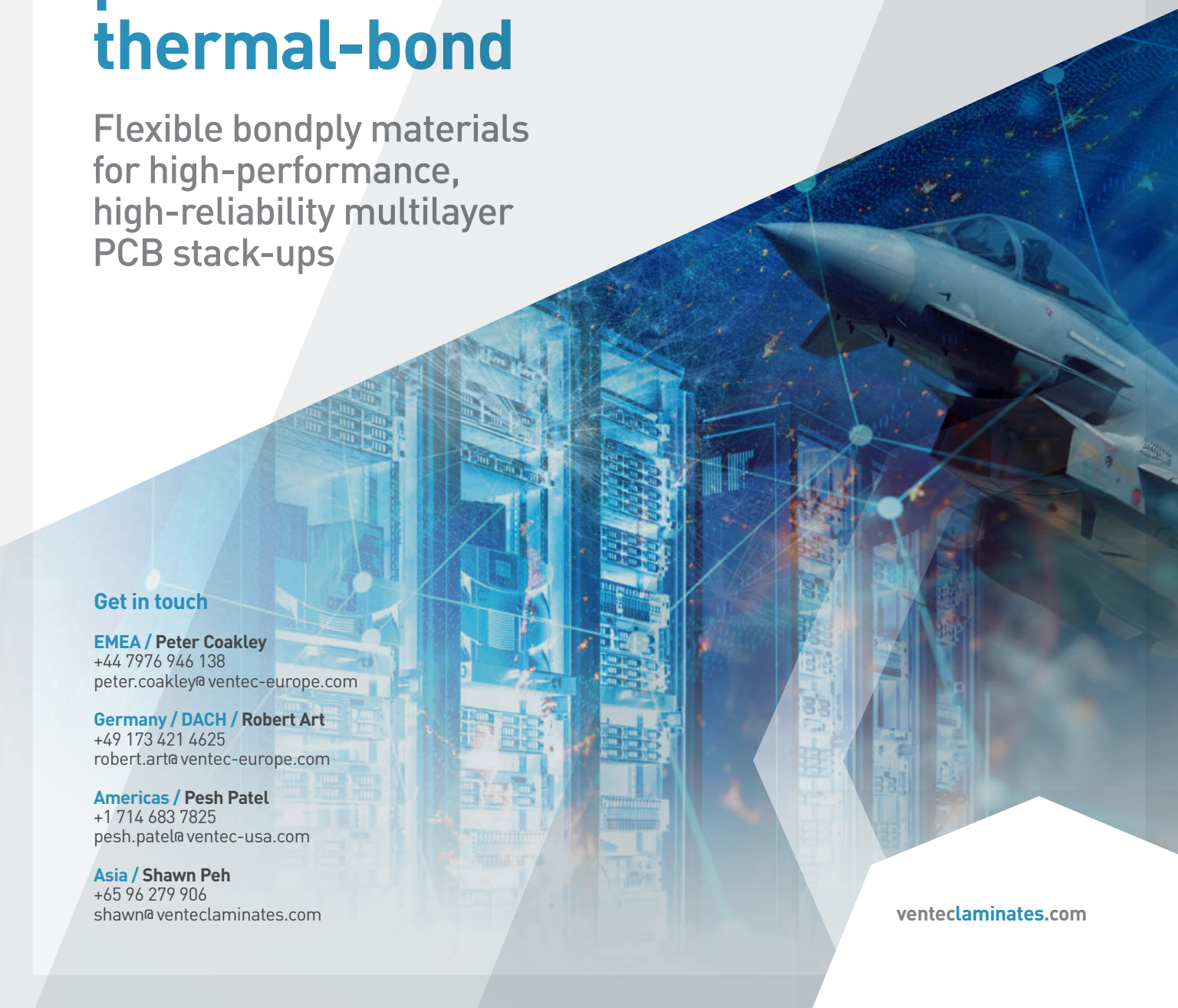

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PCDF


John Geerdes


Ram Mayampurath


Daniel Gamota


Rafael Padilla

All Flex Solutions appointed **Jamil Abdallah** manufacturing plant manager and promoted **John Geerdes** to senior process engineer.

MKS Instruments appointed **Ram Mayampurath** CFO.

NextFlex appointed **Daniel Gamota** executive director.

Shengyi Technology named **Rafael Padilla** VP of OEM marketing (North America).

CA


Greg Beck


Michael Bowden


Victor Madero


Bill Wentworth


Christopher Nash


Richard Burke


GayeLyn Bates


Bob Pearson


Rosie Medina


Matt Hansen

Jeff Gilbert

Absolute EMS named **Greg Beck** director of sales.

Altus Group appointed **Michael Bowden** service and applications engineer.

Count On Tools appointed **Victor Madero** of SMTVYS Technology partner and distributor for Mexico.

Data I/O named **Bill Wentworth** president and CEO.

Indium promoted **Christopher Nash** to senior sales and business development manager.

Kyzen named **Richard Burke** key account manager.

Libra Industries appointed **GayeLyn Bates** senior vice president of business development.

PDR Americas appointed **Bob Pearson** representative for the Central Texas region.

Promex Industries named **Rosie Medina** senior vice president of sales and marketing.

QP Technologies promoted **Matt Hansen** to VP of sales and marketing.

Spectrum Advanced Manufacturing Technologies announced the retirement of CEO **Jeff Riggs** and the appointment of **Jeff Gilbert** to the position.

Unigen named **John Burke** president and COO.

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PCB West Exhibition Floor Sold Out

PEACHTREE CITY, GA – The exhibition floor space is sold out for PCB West, the largest exhibition and conference for printed circuit board design, fabrication and assembly in the Silicon Valley. It is the tenth time in 11 years all booths have been sold for the popular exhibition, PCEA said.

"Coming off an outstanding PCB West 2023, booth sales for our 2024 event have been strong," said Frances Stewart, vice president of sales and marketing at PCEA. "We're looking forward to another great event."

PCB West will be held Oct. 8–11 at the Santa Clara (CA) Convention Center. The event includes a one-day exhibition on Oct. 9.

This year's show will feature more than 100 exhibitors showcasing the leading companies in the PCB industry, including the top CAD and CAM vendors and top names in printed circuit fabrication and electronics assembly. Attendees will be treated to a free lunch on the show floor during the exhibition on Oct. 9.

'Early Bird' Discount for PCB West Technical Conference Ends Sept. 7

PEACHTREE CITY, GA – The discounted price for the PCB West 2024 technical conference ends Sept. 7. From Sept. 8 through Oct. 8, registrants will pay the advanced conference price, which is $100 more than the "early bird" rate.

The technical program for PCB West 2024 features more than 115 hours of in-depth electronics engineering training from leading experts such as Rick Hartley, Lee Ritchey, Tomas Chester, Dan Beeker, Gerry Partida and Susy Webb.

The scope of classes ranges from designing all types of printed circuit boards to complex signal and power integrity and power delivery systems design. Foundational topics such as circuit grounding and PCB stackups are interspersed with advanced tutorials on DDR5, thermal management, analog measurements, system mechanical design, and more.

"This year's lineup of presenters is second to none," said Mike Buetow, president, PCEA. "It is literally the only place where you can meet Rick Hartley, Lee Ritchey, Susy Webb and Dan Beeker in one place. That's what makes PCB West the industry's leading event for technical information and professional networking."

Registration for the technical conference and the exhibition is open at pcbwest.com.

An exhibition featuring more than 100 leading suppliers to the electronics design, manufacturing and assembly

industry will be held Oct. 9.

PCEA Board Welcomes 2 New Members

PEACHTREE CITY, GA – PCEA in June welcomed two new board members, filling two vacated seats. The new directors both have long electronics industry experience across the design to assembly spectrum, as well as significant financial expertise.

Jim Barnes is corporate senior vice president, strategic global sourcing at Generac, a leading energy technology company. Prior to that, he spent more than 15 years in management at a publicly traded multinational EMS company. He is an expert in strategic planning, team building, finance, outsourcing, manufacturing operations best practices, supply chain, and business development, with experience in the US, Mexico and Asia.

Matthew Leary has been designing PCBs full-time since 1996. He is the founder and president of Newgrange Design, a Boston-area PCB design service bureau. His design work has included high-speed, high-voltage, high-power, high pin count, low-level signals, and more. He is a graduate of the University of Wisconsin-Madison with a degree in physics.

Jim Barnes

Matt Leary

CPCD Course to be Offered at Wayne State in 2025

PEACHTREE CITY, GA – Wayne State University will offer PCEA Training's Certified Printed Circuit Designer curriculum as part of a semester-long course on printed circuit board design starting in January.

The Detroit-based school, the third largest in Michigan, gained experience with the course last summer when it held a CPCD class of approximately 35 students in June.

Students will be taught the entirety of the CPCD course, which includes the *Printed Circuit Design Professional*

handbook, a 400-page guide of technical information that provides the knowledge base for making good decisions in the printed circuit engineering process. Wayne State plans to add lab work and talks from local manufacturers as part of its course, and will use the CPCD certification exam as its final exam.

PCB East 2025 Conference Task Group Named

PEACHTREE CITY, GA – The PCEA Conference Task Group named its PCB East 2025 members.

Troy Hopkins, a printed circuit design professional and consultant, leads the group as chairman alongside eight other printed circuit industry veterans.

Other industry experts in the task group include John Burkhert Jr., Stephen Chavez, Tomas Chester, James Jackson, Keith Kowal, Matt Leary, Matt McBride, and Susy Webb.

"Building off the continued growth of last year's conference, I am thrilled to bring together this exceptional group of industry experts," said Hopkins. "Their experience and collective wisdom will help ensure PCB East 2025 will showcase content that addresses the challenges facing PCB designers as well as showcasing the latest innovations and best practices in PCB design and manufacturing.

"With this group I am confident this conference will continue to provide massive value, empower PCB designers, and bring our industry together."

PCB East is the largest technical conference and exhibition for the electronics design, fabrication and assembly industry in New England.

The four-day technical conference takes place Apr. 29 – May 2 at the Boxboro Regency in Boxborough, MA, with a one-day exhibition on Apr. 30. For details, visit pcbeast.com.

PCEA CURRENT EVENTS

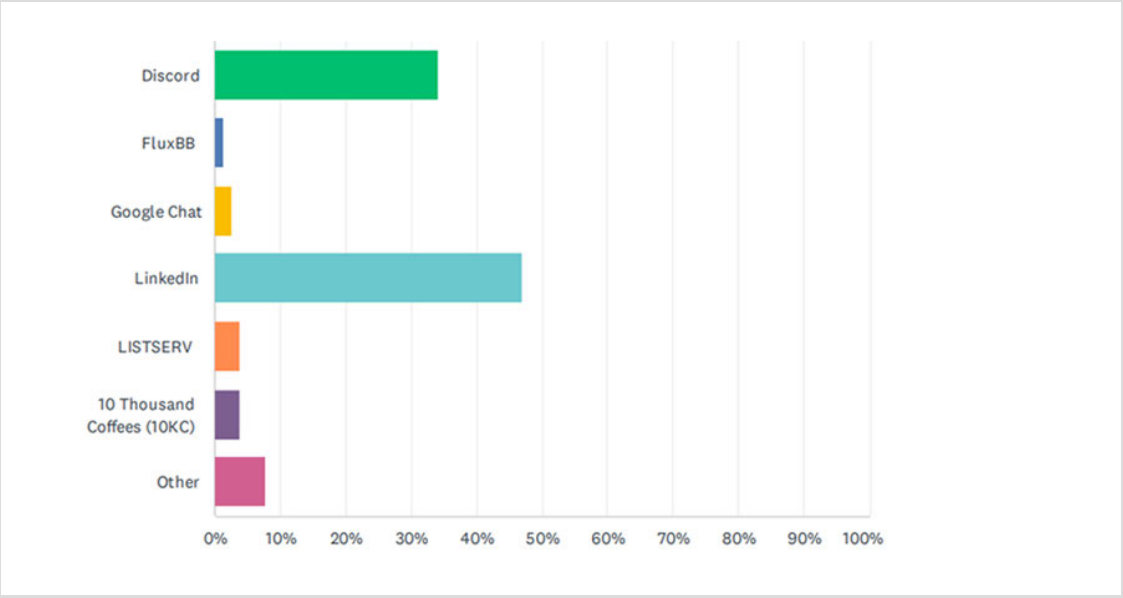
CHAPTER NEWS

General. The annual PCEA meeting will be held Oct. 8 from 9 – 10 a.m. during PCB West at the Santa Clara (CA) Convention Center. An update on all association programs, plus the annual awards, will be presented.

Abstracts for next year's PCB East technical conference are due Sept. 6. The conference, the largest of its kind in New England, will take place Apr. 29 – May 2, 2025, in Boxborough, MA. The event includes a one-day exhibition on April 30. Submit abstracts here.

Some 78% of respondents to PCD&F's annual Salary Survey said they would find value in an online

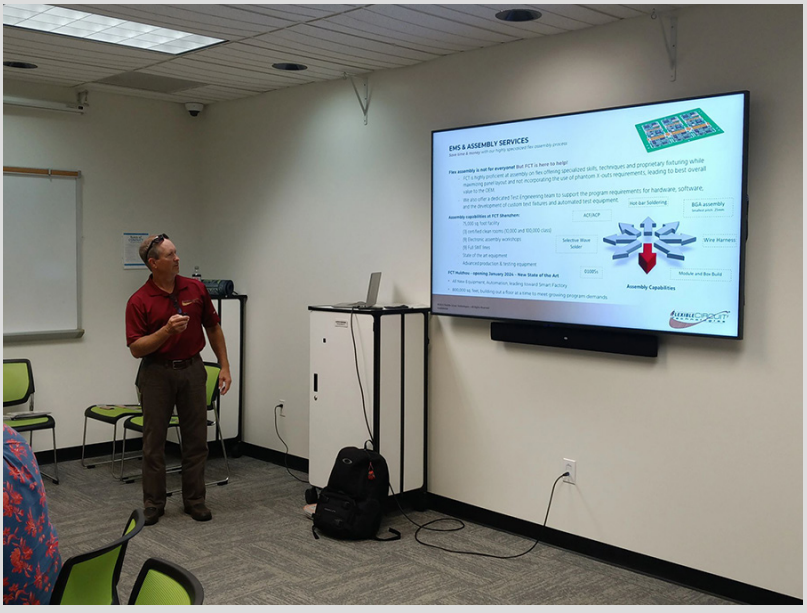
networking forum dedicated to printed circuit board design and engineering. When it comes to the type of forum, however, the responses were varied. LinkedIn was the top choice, at 47% of respondents. Discord was second, at 34%. No other option received more than 5% of the votes cast.



LinkedIn and Discord are the preferred forums for designers/design engineers to network online.

Portland, OR. In August we welcomed Bill Loving of ScanCAD International for a discussion about PCB reverse engineering. We will hold a live meeting at Axiom Electronics in October. Those interested should email sschmidt@pcea.net.

San Diego. Our meeting on Aug. 20 featured Mark Finstad, director of engineering at Flexible Circuits Technologies. Chapter members enjoyed a presentation on flex circuit design and manufacturing over lunch.



Mark Finstad talks at the San Diego chapter meeting in August.

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MARKET **WATCH**

Electronics Industry Sentiment Rose at end of July

BANNOCKBURN, IL – Sentiment in the electronics industry saw a modest uptick in August, though it remains below the peak observed in April, IPC said in a report released in mid-August. The results are based on a survey conducted Jul. 18-31.

Regarding current supply chain conditions, half (50%) of electronics manufacturers responding said they are currently experiencing rising labor costs, with 46% reporting increased material costs. At the same time, ease of recruitment, profit margins and backlogs are presently declining. Over the next six months, electronics manufacturers expect labor and material costs to remain high, although relatively stable. Profit margins and backlogs are expected to rise, with recruitment challenges continuing to persist.

Some 42% of respondents are very or extremely concerned about geopolitical risks and 44% are concerned with trade policies and tariffs, with no significant differences by geographical regions.

Additional survey data show:

- The demand index increased 3.3% in August, fueled by better, albeit still contracting, backlog, capacity utilization that shifted to expansion, and heightened order sentiment.
- Cost pressures eased slightly in August, with indices for labor costs and material costs each dropping one point. Despite the declines, both indices remain in expansion territory, indicating a majority of businesses continue to face cost challenges. Notably, the labor costs index hit a new low for the year.
- The overall industry outlook remained robust in August, although demand sentiment has cooled from earlier highs this year.

Search Party

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	APR.	MAY[r]	JUN.[p]	YTD
Computers and electronics products	0.0	-0.4	-0.3	1.2
Computers	3.8	-1.1	-2.3	23.7
Storage devices	1.7	0.0	-6.4	6.5
Other peripheral equipment	5.4	0.5	0.2	4.5
Nondefense communications equipment	0.0	-2.2	2.2	-0.2
Defense communications equipment	1.5	-2.0	-2.0	-2.1
A/V equipment	-7.1	-3.9	-1.3	15.3
Components[1]	1.0	0.9	-1.3	6.3
Nondefense search and navigation equipment	2.2	-0.9	0.2	1.9
Defense search and navigation equipment	0.4	0.4	-0.9	5.8
Electromedical, measurement and control	-0.3	-1.0	0.1	-1.2

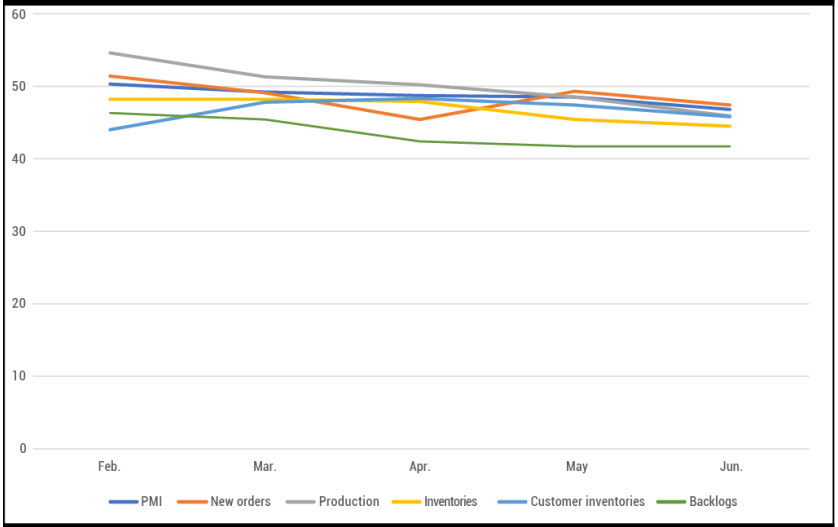
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, August 2, 2024

Key Components

	FEB.	MAR.	APR.	MAY	JUN.
EMS book-to-bill[1,3]	1.31	1.42	1.36	1.32	1.21
Semiconductors[2,3]	15.2%	15.8%	19.3%	18.3%	
PCB book-to-bill[1,3]	1.13	1.06	0.96	0.95	0.99
Component sales sentiment[4]	106.9%	124.1%	112.3%	98.9%	103.4%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA

US Manufacturing Indices



Source: Institute for Supply Management, August 1, 2024

Hot Takes

Sales of **PCB materials** (excluding flex) dropped 16% year-over-year to $57 billion in 2023. Copper-clad laminate sales made up about $13 billion, including prepreg but excluding mass laminate. Some 650 million sq. m. of rigid

laminate materials, including paper, composite, FR-4, and specialty laminates were sold, down slightly from 2022. (Prismark)

The global **flex PCB market** will gradually recover from its 2023 downturn, with the market size expected to reach $19.7 billion in 2024, representing a 7.3% year-on-year growth. (TPCA).

Japan's PCB output has shrunk for 19 consecutive months through May, but the decline has only been in the single digits for the past three months. (JPCA)

North American PCB shipments in July fell 21.2% versus a year ago and sank 14% sequentially. Bookings were down 25.4% and 17.3%, respectively. (IPC)

The **European PCB industry** saw a year-over-year decline in billings of 6.5% during the first half of 2024. (Data4PCB)

North American EMS shipments in July rose 1.9% over July 2023 and were up 1.9% over June. Year-over-year bookings increased 0.2% and quarter-over-quarter bookings rose 0.1%.

Packages using **chiplet architectures** will grow at 69% compounded annually from 2023 to 2029. (TechSearch International)

Worldwide **silicon wafer shipments** in the second quarter declined 8.9% year-over-year, but rose 7.1% quarter-over-quarter. (SEMI)

Major **PCB and IC substrate manufacturers** from Taiwan are expanding operations in Southeast Asia but face sustainability challenges amid uncertainties of electricity and water supply. (DigiTimes)

Three **EMS transactions** were recorded in the second quarter, down from five recorded in 2023's second quarter. (Lincoln International)

Global **semiconductor sales** totaled $149.9 billion during the second quarter, an increase of 18.3% compared to 2023 and 6.5% more than the first quarter of 2024. (SIA)

Taiwan's export orders rose more than expected in July as **demand for chips used in artificial intelligence applications** continued to soar and the government said it expects the momentum to extend into August. (Taiwan Ministry of Economic Affairs)

Taiwan-based ODMs are cautiously optimistic about **consumer electronics product demand** in the second half of this year, according to industry sources. (DigiTimes)

DRAM sales saw revenue growth of $22.9 billion in the second quarter, a sequential rise of 24.8%, on higher shipments of mainstream products. (TrendForce)

The amount of **data center supply** under construction in North America's top markets jumped by about 70% compared to a year ago to a record 3.9GW. (CBRE Group)

Worldwide spending on **artificial intelligence**, including AI-enabled applications, infrastructure and related IT and business services, will more than double by 2028 to $632 billion. (IDC)

North American **EMS shipments** in July were up 1.9% compared to 2023 and increased 1.9% sequentially. Bookings increased 0.2% year-over-year and 0.1% from the previous month. (IPC)

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ROI

From Microns to Nano

PCB designs will soon enter a new dimension in miniaturization.

OUR INDUSTRY HAS always been about creating cutting-edge, next-generation technology. Over decades this has been accomplished by striving to pack more capability in less space. The electronics industry, and printed circuits in particular, has accomplished this more often than not without specific definitions to either strive for, or be hindered by.

Such examples can be found by looking at the definitions, per Oxford Languages, for five simple words that have been used over the decades in our technologically driven businesses:

- Normal – defined as "usual, typical or expected"
- Small – defined as "of a size that is less than normal"
- Compact – defined as "closely and neatly packaged together; dense"
- Miniature – defined as "if a much smaller size than normal"
- Dense – "closely compacted in substance."

Clearly, the definition of each word has, shall we say, an open interpretation as it relates to technology, dimensions and tolerances! And yet, over the decades, engineers speaking and working on next-generation projects have had more than a good idea of what, at that point in time, each word meant.

In the early 1990s, if you were fabricating printed circuit boards, "normal" was defined as a board with 7-mil lines and spaces. "Small" referred to something along the lines of 5-mil lines and spaces. "Compact" would have included a panel of circuit boards that were V-scored to get as many as possible on the panel. "Miniature" was a dream: lines and spaces of less than 5 mils. And "dense" referred to how thin the combined layers on a multilayer circuit board can be.

That was then, now is now. New words are entering the vocabulary of designers and fabricators. The days of using terms with open-ended interpretations when defining the goal of getting more capability into less space has finally given way to the use of words with more specific dimensional definitions.

"Micron" has been used for years in the discussion of dimensions and tolerances sought when designing and fabricating circuit boards. Micron is a metric unit of length equal to one *millionth* of a meter. Developing the processes and materials to support micron technologies' ultra-minute dimensions is a formidable task that is still underway, but it has yielded highly successful results.

Today, micron plating thicknesses and the ability to plate in microns is common. IPC standards define acceptable plating thicknesses in microns. Suppliers of PCB materials use microns in their specifications. Imagining the ability to plate or image in microns was once a dream. Today, while still cutting-edge, holding dimensions and tolerances in microns is commonplace, and micron technologies are standard in the greater electronics industry.

Another word gaining traction in our industry is "nano." "Nano" is a short for "nanotechnology," which is a metric unit of length equal to one *billionth* of a meter. If producing printed circuit boards with dimensions in microns is cutting-edge, producing circuit boards with nano dimensions is nothing less than bleeding edge! But as intimidating as the thought of nano dimensions may be, developing processes and materials is how our industry, over and over, has been able to develop bleeding-edge technologies that eventually become industry standard.

If micron is today considered "normal," then new processes and materials necessary to establish nanotechnology within the printed circuit board industry will undoubtedly go through various iterations and phases of research, development and refinement. These combined efforts will be more interesting, as well as more challenging, than those of the past, in large part because the size – the actual dimensions – have far exceeded the ability for the unaided human eye to observe.

Equally, some of the products in which nanotechnologies will be utilized may also be too small for the human eye to see unaided. As dimensions shrink, so can the packages they go into.

So here we are again, as we have been countless times over the decades; an industry working on the next challenge. This time it is taking the current "normal" of micron technology, and by diligently working to transition processes and materials, moving from "small" to "compact," "miniature" to "dense," until we achieve the next baseline for "normal," which will shortly be nanotechnologies. Onto the next great challenge, and repeat.

PETER BIGELOW is president of FTG Circuits Haverhill; (imipcb.com); pbigelow@imipcb.com. His column appears monthly.

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Disruptive people, technologies or real advancements in our society are so few, it seems we now must minimize these people or events when they actually occur due to the overuse of this term. For most of us, success is a byproduct of very hard work, learning from failures, collaboration with the people we are surrounded by, an ability to see the real issues affecting our businesses with a focus on solving the critical few, a strong competitive drive for "winning," and yes, a little good luck.

Winning deals or awards is both an exhilarating and a humbling experience, but not something to dwell long on as the next challenge is always right around the corner. Outstanding business results simply gave us the right to wake up and fight a new fight the next day; it's our job and people are counting on us to perform. Those people counting on us are our families, customers, shareholders, stakeholders and vendor base.

I feel that a degree of "working scared" has driven excellent results for the successful EMS professionals I know. Selling scared wasn't a fear of being successful or entering a challenging opportunity; it was the fear of "losing" and not doing your best to outplan and outperform the competition. It's a fear to deliver less than the desired outcome you have been tasked to do. It was a fear of not meeting a deadline that people were counting on or the fear of taking too long to respond to someone who reached out to you earlier in your busy day.

The defining competitive spirit to enter a contested deal, maybe with the weaker team solution but driven to outsell the competition, has resulted in many wins in our work history. Writing the best technical response to an RFI, taking time to really understand the needs of a prospect and offering solutions, getting to your factory before an audit to run a mini-audit yourself, preparing the factory on roles and responsibilities for every audit, managing the arduous task of getting a quote just right, producing marcom content that can be used at the right time from a sales tool kit that defines who you are and who you aren't … these are the moves that separate the EMS sales professional from the sales hobbyist.

The difference between self-confidence and self-idolization is big. To me, self-confidence is earned over time after numerous failures where you learn lessons that stay with you forever. At some point in our lives, we should realize we now know what we know, and work to fill gaps of what we don't.

Self-idolization, on the other hand, can be hatched overnight with a post, a self-described title or the simple claim you have arrived and the world should take notice.

With a good sense of who you are and over time, the wins are a little less celebratory and the losses don't drive you into a depression. You simply look forward to the next opportunity to compete and try to outperform your competition.

Once you have achieved years of successes, the world you want to compete in will take notice and will want you on their team. Empty or exaggerated claims of superiority support no purpose other than stroking an overinflated ego. Those who start to believe a self-idolizing status tend to lose whatever edge they once had and spill into mediocrity.

Still inclined to describe yourself in these terms? Perhaps you should adopt the funniest title I've seen: "President of Awesomeness."

JAKE KULP is founder of JHK Technical Solutions, where he assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc. He can be reached at jkulp@cox.net.

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Is Thailand the World's Next PCB Manufacturing Base?

The country's growing industry could prove a viable alternative to China.

I HAVE BEEN involved in the electronics manufacturing industry for over 20 years, with much of that time based out of Hong Kong. China is a manufacturing powerhouse, supplying not only the world but its own large population with electronic products ranging from home appliances to ultra-modern electric vehicles. China is well beyond being called a "developing nation." It is a very mature economy – especially when it comes to any kind of manufacturing.

Recent geopolitical tensions from past and present US administrations, however, as well as supply chain concerns that came about during the Covid pandemic, have forced many OEMs and EMS companies to look elsewhere for their PCB needs – a task that is easier said than done.

In response to industry demands, I have traveled to several countries in southeast Asia over the past 18 months to learn as much as I can about the printed circuit board industry outside of China.

It was during my third and most recent trip to Thailand last July that I attended Thailand Electronics Circuit Asia 2024 (THECA), the electronics circuits and services showcase event in Bangkok.

The event did mark a milestone, as interest in Thailand's future in PCB manufacturing is booming. In fact, from January 2023 to June 2024, investment applications for PCBs totaled over $3.9 billion compared to an average of $420 million for the same period in 2021 to 2022, according to the Thailand Board of Investment.

The Board of Investment is expecting more than $1.4 billion in investments from Chinese EV OEMs to set up manufacturing hubs to supply Asia, which has presented many opportunities for these new factories. BYD, one of the largest EV car manufacturers in the world, opened its first factory in Thailand in July.

Interestingly, most of the PCB manufacturers exhibiting at the show were from China or have factories being built in Thailand that are owned by Chinese PCB manufacturers or their investors.

Thailand has always had a strong PCB manufacturing base when it comes to low-mix and high-volume manufacturing. Like most other countries trying to mimic China's success, however, it falls short when it comes to higher-mix, lower-volume, and higher-technology PCB manufacturing. That said, since early 2022, over 20 prominent PCB manufacturing companies from China, Hong Kong and Taiwan are planning or are currently building PCB manufacturing facilities in Thailand to expand the globalizing of their manufacturing capacity.

It is hoped this expansion brings opportunities. But it will also bring challenges as this is the first time some of these PCB manufacturing companies have invested heavily outside China.

During the show, I was able to talk to several general managers from different factories that are being built one to two hours outside Bangkok. These China-based managers have plenty of industry experience and were sent to Thailand to oversee the construction of their respective new facilities.

While they originally anticipated starting production earlier this year, the shortage of construction workers, the global economic slowdown and the uncertainty of incoming orders has forced these factories to most likely start operations later this year.

The output of these facilities will be gradual, with their first phase expected to produce 40,000-50,000 sq. m. per month, using upwards of 300 employees each. Several of these new factories plan to cater to customers that require high-mix, low- to high-volume and higher technology. This capability is very important as Thailand has generally catered to low-mix, mid- to higher-volume orders that are not as conducive to the US market.

These managers are facing cultural and operational obstacles, including finding enough technical operators and engineers for their factories. With over 20 large PCB facilities currently manufacturing or about to begin operations in Thailand, machine operators, engineers and chemists are in high demand.

High demand means short supply and many established domestic factories have had technicians and engineers hired away by these manufacturing newcomers. The need for experienced personnel and PCB engineering training cannot keep up with Thailand's high demand.

Language is another barrier among the Chinese and local Thai workers, as some managers say it takes upwards of a year for a factory to become a cohesive operation.

To help increase the employee supply base, several of these new facilities plan to send their Chinese employees to Thailand to train local hires, as well as source labor from outside Thailand.

Factories not only need employees but also need a supply chain to support their operations. While Thailand does manufacture raw materials, a major Chinese laminate supplier intends to open a new facility by Q4 2025.

The pricing for PCBs manufactured in Thailand is 10-15% higher than China. For now, the 25% US-imposed tariff does not apply to PCBs manufactured in Thailand. That is good news, but the average time to ship orders is much longer, averaging six to eight weeks. In comparison, China ships most product in three to four weeks or less.

The next 18-24 months will determine how successful Thailand will become as a PCB manufacturing powerhouse. The strength of the world economy and the politics that are put into play will determine the outcome.

CLEMENT YUEN has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com) and can be reached at clement@directpcb.com.

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Metal Health

Whether in wire or trace form, keep copper thickness in mind for your design.

ONCE UPON A time, about eight decades back, we didn't have printed circuit boards. We had copper wires that came in various diameters. Carrying a larger amount of current requires conductors of a larger diameter. These various diameters were identified by the American Wire Gauge (AWG) where smaller numbers indicated thicker wires. There is a metric equivalent where the opposite is true – a higher number for a thicker conductor. Set that aside for this discussion.

Heavy gauge wire for power. A 12- to 14-gauge wire is about the diameter of a cooked spaghetti noodle (~2mm) and is commonly found in power cords for smaller electronics such as a table lamp or a fan. An electric dryer running on 220V will require something between 10- and 6-gauge wire depending on the amperage of the appliance. Again, smaller numbers refer to larger cross-sections.

For the sake of flexibility, these thicker wires are typically constructed of several smaller wires twisted like a candy cane prior to adding the insulation coating. The coating itself is not part of the gauge, only the conductor matters in that regard.

Connection wire for signals. Then you have a 30-gauge wire, which is more like angel hair pasta. The diameter is 0.25mm, yielding a cross-section of roughly 0.05mm. This will be a single strand of wire and is typical of the "white wire" used to rework/repair a printed circuit board. The maximum current rating for 30-gauge wire is 500mA, which is fine for the intended signals.

General purpose wire. Between the 12 and 30 AWG conductors is 18-gauge, which can be used for general connections such as speaker wire. At 1mm of diameter, this gauge is rated at 7A when using polyvinyl chloride (PVC) for insulation. Teflon-coated wire has a higher operating temperature, so the same wire bundle can handle a bit more current without going up in smoke. This is analogous to using high-performance dielectrics on a printed circuit board.

As a factory worker in the mid to late '80s, I was soldering 12-, 18- and 30-gauge wires to assemble telecom racks. Those 7' to 11' tall units permitted a single T1 phone line to carry from 384 up to 528 separate signals through digitization. This was much better than the 24 analog signals (12 actual conversations) that the T1 line originally supported. The antitrust breakup of AT&T meant that all of the Baby Bells had to pay up to get the enabling equipment. So-called rack wire and test was my entry into high tech – 40 years ago!

Coaxial wire: One step beyond a twisted pair. Credited to Oliver Heavyside in an 1880 patent, a special type of wire known as coax features a non-stranded conductor inside an insulator that is then wrapped by a weave of copper with another layer of insulation around the weave. The woven shield is used as the ground path for the transmission line.

Figure 1. A coaxial cable creates a Faraday cage around the central conductor. The isolation and controlled impedance permit much longer runs without signal degradation. (Source: BHPhotoVideo)

This wire within a wire provides a controlled impedance environment of 75Ω for the central strand, with the weave also acting to mitigate electromagnetic interference between the inner wire and any outside sources. The coaxial arrangement protects the outside world from the noise inside the cable as well as isolating the inside from the environmental effects beyond.

Wire compared to PCB traces. All the ratings for hook-up wire have a corresponding cross-section to the traces on a PCB. The primary difference is the wire is round while the traces are more of a trapezoid that tapers toward the top. The average thickness and width of the trace determine the current capacity, while the type of dielectric material governs how much temperature rise is acceptable. The advantage of wires is in the connection flexibility, where the traces shine in terms of handling more complex circuits in less space.

Copper thickness is measured by weight. One of the oddities related to plating has to do with the way the thickness of copper is specified. You may have heard of 1 oz. copper or some other number like that. The unit of measure is based on 1 sq. ft. of copper. Whatever that square foot weighed would be the value of that thickness.

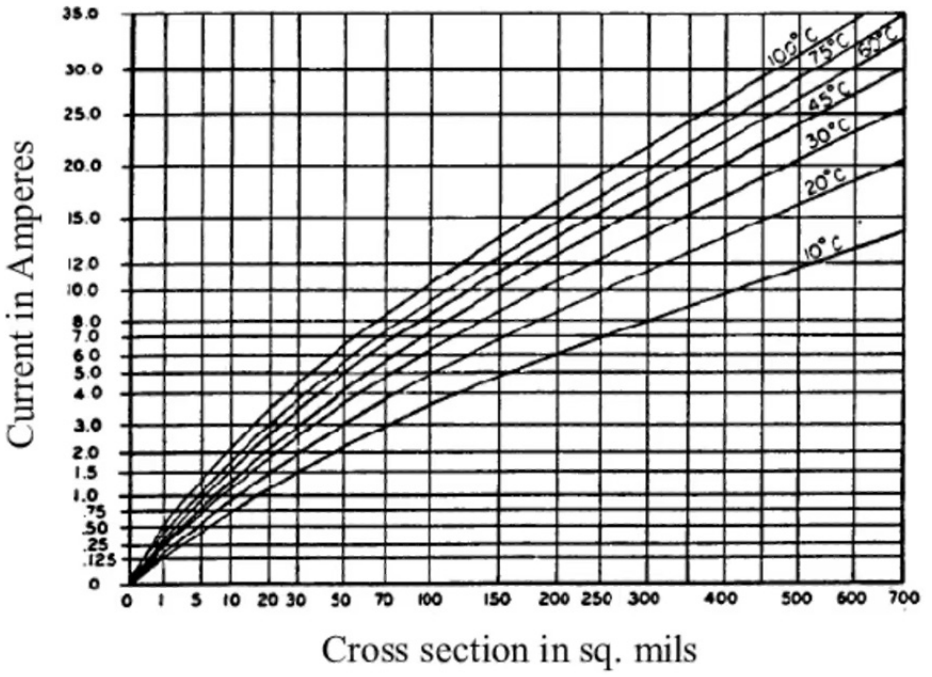

Figure 2. Before tools or apps could solve metallization requirements, these current carrying capacity charts were used to determine conductor width. This chart shows how much of cross-section is required for a given temperature rise. The lower, more conservative numbers of 30° of rise or less are preferred. A current of 5A with an expected temperature rise of 20°C require a cross-section of 100 mils. (Source: IPC)

Starting plating vs. finished plating. Fabrication drawings refer to finished copper thickness. The reason for this is that 1 oz. copper is only the beginning. A full PCB panel with copper on both sides is drilled for all the plated through-holes in the design prior to any etch process. In simple two-layer terms, this is all one core. For a four-layer stackup, innerlayers have been etched with a circuit pattern prior to lamination.

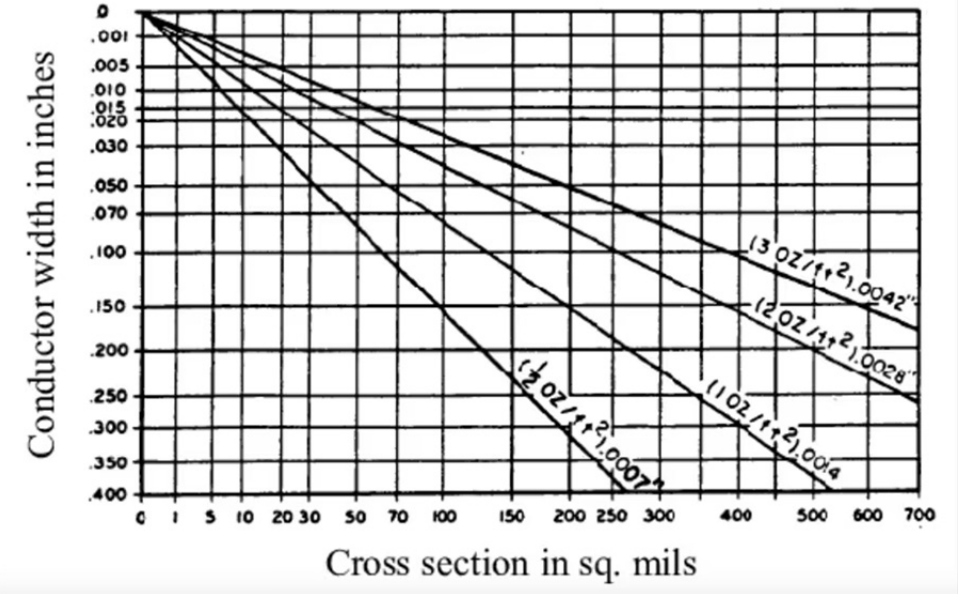

Figure 3. Sticking with the 5A current estimate and 20°C allowable temperature rise, the 100-square-mil target is found using 1 oz. copper that is about 75 mils (1.9mm) wide. Using 0.5 oz. copper would require double the width for the same outcome. (Source: IPC)

Now you have a board where the outer layers are still solid copper. This is the point when the drilling operation takes place. The whole board is still shorted out at this stage. The board is seeded with an electroless copper deposition process that lays down a very thin layer of copper inside the holes. After that, electrodes are attached to the outer plating layers and the whole thing is run through various processes that add more copper and finally some tin to the "barrel" of the holes. For this reason, the copper in the barrel will always be thinner than the copper on the outer layers that have the advantage of starting out with the original plating.

Considerations for high-density interconnect. High-density interconnect (HDI) uses a sequential lamination process where each layer that has microvias will also have plate up beyond the original copper. Much like the four-layer board in the above example, the layers that do not get plated up are in-between the first and last layers of any core vias that may be present. For example, the 14-layer stack-up in Figure 2 with a core via from layer 3 to layer 11 would plate up all layers except those between layer 4 and layer 10.

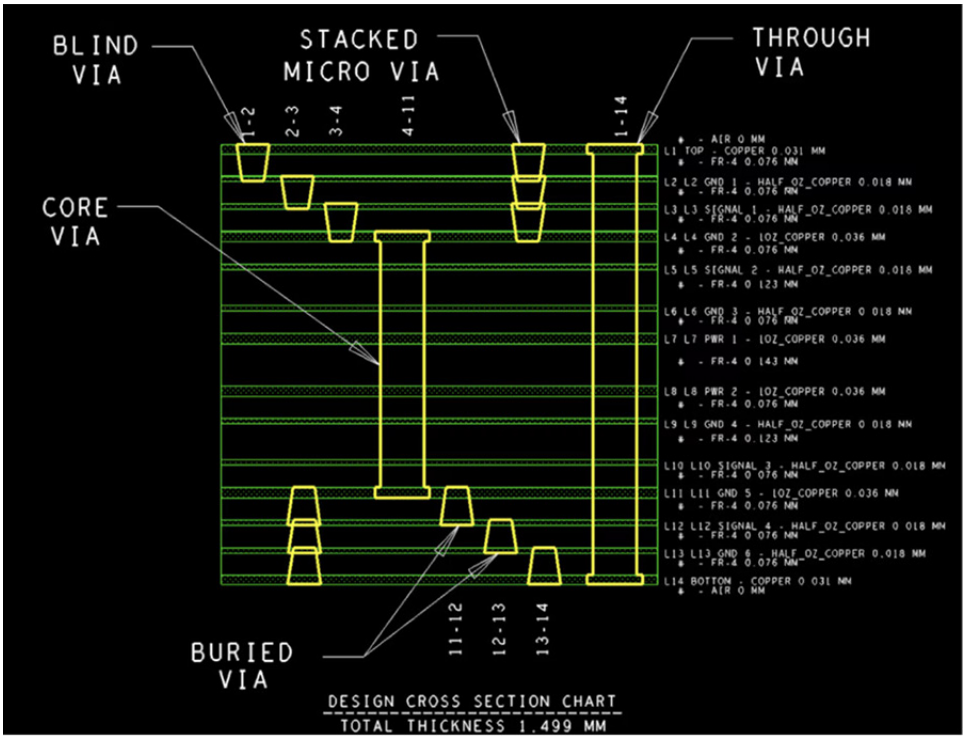

Figure 4. A diagram labeling the classes of vias in a typical HDI stackup. Plating-up via connections is one of the considerations for overall board thickness as the process adds material to the metal layers. (Source: Author)

Ultra-high density (MSAP). The significance of not plating up is that the layers that didn't terminate a normal blind or buried via (L4-L10) would be the only layers where modified semi-additive process (MSAP) could be used. The starting copper for MSAP is only a fraction of the usual copper thickness. A mask is put over the areas to be removed and the rest is plated up. This creates high and low areas. The high areas are retained by another mask where we want a circuit pattern, and the low areas are subsequently microetched away to reveal the circuit pattern. The initial plating has a lot in common with the first step of chemically plating the vias. They use a very thin layer of copper and electroplate up to the required finished thickness.

Metal core PCB. Let's finish up with one of my favorite examples. Known as "The Stick," it's for a CDMA (3G)

multi-carrier RF amplifier to be used inside the little hut at the bottom of every cellular tower. The first time I was listed as a contributor on a patent was for the innovative via structure with a "backdrill" that started from the top. Notice **Figure 5** where you can see the black dots along the edges of the device cavities. They are effectively used as ground vias from layers 2-4. The leads of the amplifier chips solder right over the top of the drilled and filled counterbores.

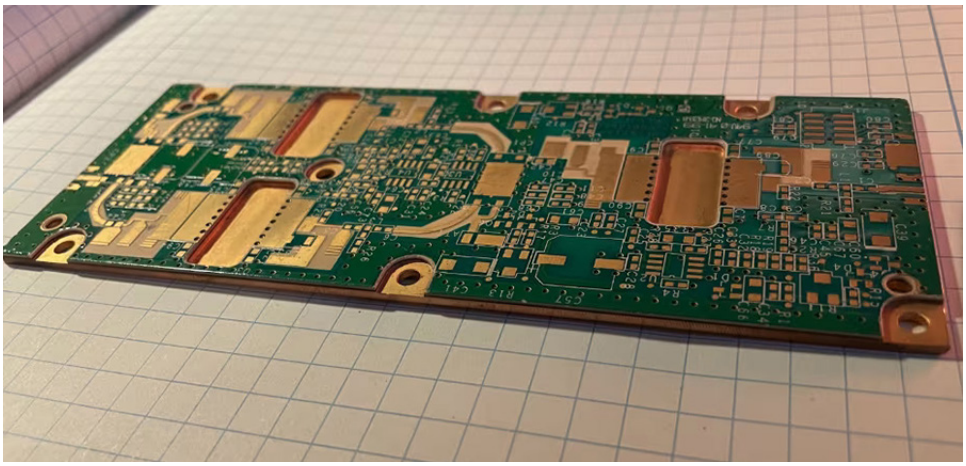

Figure 5. A metal core board that uses 32 oz. copper for layer 4. The copper pallet makes up about 75% of the board's overall thickness. (Source: Author)

This is only four layers, but the solid copper bottom could have had another three layers below the copper slug for a total of seven. It's surprisingly heavy for its size. The stiffness and flatness are better than average with this much copper. This isn't very common, noting that the IPC charts only go as far as 3 oz. copper.

There is no circuit pattern at this metal thickness, but you can see where the board is relieved to expose the mounting holes. Meanwhile, the device cavities go deeper with cutouts that hog out some of the copper slug. That is done to permit the device pins to align with the top surface. This is a board with two outlines and three thicknesses. Layer 4 is rectangular with the other layers having cut-outs and slots. This is a different way of thinking beyond heavy copper.

The funny thing is that you can still find these 13cm, 75W amplifiers being sold online decades after the company, Spectrian, went under. This may be the most reliable piece of equipment I've designed – provided you get the ones with the Motorola chips rather than our homespun LDMOS devices.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

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The Drive for Innovation

On the cusp of 6G, are we also on the verge of a materials breakthrough?

THE WORLD HAS barely experienced a fraction of the services 5G mobile promised to deliver, and already the drive toward 6G is gathering momentum. The standardization process begins this year, and the final specifications are expected to be released in 2028, with rollout beginning in 2030. It's proof, if more were needed, that we are an impatient and ambitious species.

Ericsson has helpfully described the 6G standardization process, which is expected to permit a much cleaner transition than we have seen in the move from 4G to 5G. Although 6G will leverage some 5G infrastructure, particularly in the core, connectivity will be standalone from the start and should perform better as a result. It's hard to grasp, but 6G data rates and latency are expected to be about 1000 times faster than those of 5G.

The bigger picture is working toward a pervasively connected world that supports our lives and adapts to our needs, wherever we are and however those needs change in real-time. Wireless is the only connectivity that can do this for us. Realizing the necessary connections is extremely challenging at every level, from the standards-setting efforts undertaken by the 3GPP, the global body managing mobile standards, to the subcomponent level – including the new materials we must develop to build the systems that can realize the performance promised in the specifications.

As so many of the instruments and devices we connect have become highly digitized and software-defined, it can be easy to forget that the natural world around us is analog and always will be. Our digital systems must interact with this physical world, and this has fascinating implications for the antennas that will make this border traversable.

6G will take our perception of the multiple-input multiple-output (MIMO) antenna array to new levels, in pursuit of the data speeds and response times we are expecting. Configuring and tuning these large arrays will have a critical impact on efficiency and power consumption, while circuit size and system reliability will be key concerns. Switched capacitor arrays are a tried and tested solution to antenna tuning issues, but their bulk makes them unsuitable, whether in infrastructure equipment or mobile devices. These capacitor arrays also need a separate controller chip, which adds to the overall size of the system.

A clever reimagining of the switched-capacitor concept now proposes digitally tunable capacitors, realized with on-chip MEMS structures. This MEMS-within-CMOS technology also enhances reliability compared to traditional solid-state switches. The technology permits combination chips that integrate these MEMS structures with multiple sensors or switches on a single die, delivering a further boost to miniaturization, cost-efficiency and performance. This is shown to be even more impressive when you learn that the scale of these structures is about one-tenth that of

conventional MEMS devices.

These are exciting developments at the component and material levels, driven by the necessity to create the real, tangible hardware we need to provide the foundation for tomorrow's virtual and mixed-reality worlds. We can also consider some of the latest adhesive systems from the PCB industry, such as resin-coated copper (RCC) and resin-coated film (RCF), and their likely impact in this emerging world.

One application for RCC/RCF is in the construction of tiny anti-shake inductors. Manufactured at micron-scale, these devices leverage RCC or RCF's properties to maintain their mechanical stability and ensure consistent resonance parameters when used in conjunction with miniature antenna systems. Working with materials like these to produce complex components in highly miniaturized form factors, at scale, will likely drive the development of new expertise in disciplines like microfluidics to dispense minuscule and tightly controlled volumes of adhesive.

Working at the cutting edge of materials technologies for high-performing PCBs, I'm intrigued at the change in mindset that's happening in this field. Generally we tend to view reliability and longevity as virtues, and place value on building things that last. But this is now changing, driven by today's emphasis on sustainability and our concerns about the long-term impact our creations are having on the environment.

A U-turn is happening, shown in developments like the biodegradable materials I mentioned last month. Made from natural fibers, instead of conventional glass fiber, this material is easy to recycle and eliminates chemicals that are hazardous to the environment. The boards break down in boiling water, permitting fibers to be reclaimed and reused, and enabling components to be easily extracted. In contrast, very little from a conventional electronic assembly based on a PCB can be salvaged or repurposed.

Long-term reliability and resilience will always be a requirement in some applications, but plenty of application areas are either single use or have low life expectancy where a biodegradable PCB would make sense. We should all admire the ingenuity that devised this new substrate class and draw inspiration as we consider the way forward for our industry and the world.

If we can imagine it, we should have faith in our ability to build it.

ALUN MORGAN is technology ambassador at Ventec International Group (venteclaminates.com); alun.morgan@ventec-europe.com. His column runs monthly.

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ROUGHLY SPEAKING

For the Love of Learning

> Exploring new hobbies and earning new certifications can stimulate the mind – and your career.

I LIKE TO think that my hobby is learning new things, or maybe it's just an instinct for engineers. If you ask my wife, maybe that is just a mask for the adage that my hobby is collecting hobbies, which frequently necessitates learning new things. Some hobbies have significant barriers to entry, such as the financial obligations for equestrian activities, while others have more intellectual requirements, like amateur radio, also known as ham radio.

Recently I jumped into ham radio, getting my technician license – also called a ticket – and a handheld radio. For years friends in the PCB industry asked me if I was into amateur radio before I finally looked at it seriously. A few months ago, a friend and coworker got really excited about it, and he assured me that given my electrical engineering background and understanding of signal integrity, the test would be a breeze. In short, it was.

As an electrical engineer, with a significant understanding of transmission lines and electromagnetic fields, the hardest part of the technician license was learning the regulations. This truly seems like a hobby geared for electrical engineers to be able to apply technical knowledge outside of a work environment. While some of those I have already met in my local club are EEs, however, others have gotten into it for other reasons. One of the common reasons is for individual and community emergency preparedness. Various organizations in ham radio provide emergency communication services, such as Radio Amateur Civil Emergency Service (RACES) and Amateur Radio Emergency Service (ARES). Others do it for the sake of connecting and communicating with people all over the world. In modern times, we can meet and talk on the internet through voice over IP (VoIP), which is now ubiquitous in business and everyday life.

Just as I had several within the PCB industry poke me about getting into ham radio, let me be one for you. Check it out: you might like it!

On the topic of continued learning and education, it was only a few months ago that I took the PCEA Training course and passed the exam to become a Certified Printed Circuit Designer, adding the CPCD letters after my name. The PCEA integrated this training material last year, and a growing number of graduates are passing the exam to demonstrate their knowledge and understanding of a solid engineering-based process for designing and laying out a printed circuit board.

At PCB East, I was discussing the curriculum with another electrical engineer who shared a background in silicon design, and it dawned on me that the core of the training material is similar to the education I received about silicon

design – a top-down design, bottom-up implementation! If you understood that, great! If not, sign up for the class! Tongue in cheek! Or maybe do sign up! It is a proven methodology for large and difficult projects to break down the design process into manageable chunks to make methodical decisions while resolving localized issues, followed by integrating the design elements together at various stages and repeating the process.

The course offers a plethora of information ranging from basic electronics and schematics (early design) all the way through fabrication, assembly and test. Any engineer, even those who have spent their entire career in the PCB industry, will learn something in this course. It has the added benefit of allowing you to show others that you know what you are talking about in a practical sense. Some tests/certifications in the PCB industry are rote memorization-based; e.g. What are the plating requirement differences between a Class 2 and Class 3 board? But knowing information like that doesn't help you understand why and when you would need to have a 10-layer board instead of an eight-layer board before doing layout. The CPCD course passes on the higher-level problem-solving and critical-thinking skills that are necessary to be successful as a designer.

Having completed the CPCD course and successfully passed the examination, one of the unexpected takeaways was the connections and friendships I made with my fellow classmates. We were only in class together for a few days, but I felt that I built good connections with those in my cohort, such that for at least some of them, I have continued to build friendships in which we aspire to fulfill the ethos of the training and of PCEA itself: Collaborate, educate and inspire.

Finally, I would encourage everyone who takes the CPCD course to take the exam. After all, that is the evidence that you understood the material and aligned with it enough to be able to demonstrate your understanding and ability to apply it.

Let me know if you want to try connecting with me on amateur radio or to talk more about the value of the CPCD course by emailing me at geoffrey@pcea.net.

GEOFFREY HAZELETT is a contributing editor to PCD&F/CIRCUITS ASSEMBLY. He is a technical sales specialist with more than 10 years' experience in software quality engineering and sales of signal integrity software. He has a bachelor's degree in electrical engineering; geoffrey@pcea.net.

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HIGH-SPEED **DESIGN**

Fundamentals of Signal Integrity at Various Frequencies

Tips and tricks for applications of all speeds, from 1MHz to gigabit level.

by ANDREW GONZALES and JASON METZNER

How do you know a high-speed design application from an ordinary one? What qualifies as high speed and when does design rigor need ramping?

With CAD tools available to help enforce design rules and the internet at one's fingertips, PCB designers may implement "best practice" techniques without truly understanding their importance. They may also be missing some less common, powerful and effective techniques as well.

Here we target a broad range of designers and discuss the gamut of lower-speed designs up to gigabit-level speeds. We cover board-level tips and tricks and explain why these tips are important and the nature of the physics behind them. Whether you're designing with simple I^2C or gigabit ethernet, there's something to be gained by considering even the simplest additions to a design.

Throughout, we explore the common themes throughout all speed applications and the best practices that could extend beyond board-level traces and planes.

Let's start on the slower end and work our way up.

Low-Medium Speeds (1MHz to 100Mhz)

A competent PCB designer understands the relationship that clock and data frequencies have with a PCB's physical characteristics, which includes when to increase design rigor. Simple serial interfaces (including single-ended and differential) can produce signal integrity issues if laid out incorrectly, so it's important to understand the fundamentals of signal integrity, even at these lower speeds.

Table 1 features a list of common, industry-standard interfaces that warrant special consideration when performing PCB layout. Note that the clock or bus frequency is what we are looking at here, not necessarily the data rate. The table should indicate where a given design sensitivity might sit concerning these rising and falling edges for lower speeds.

Table 1. Industry-Standard Interfaces for Low-Medium Speeds

1MHz or less	1-50MHz	50-100MHz
12C	USB Full Speed	Octo-SPI
UART (typical)	SD (default/high speed)	SD Ultra High Speed (UHS)
I2S (depending on sampling rate)		
	CAN	
	Ethernet (10BASE-T)	
	SPI	
	Ethernet (100BASE-T)	
	LVDS	
	PCI	
	RS485	

Some of the protocols described have good protocol-layer protection and can help improve data integrity (not necessarily signal integrity). CAN is a good example of this, given its failure detection mechanisms.

But let's look at some of the physical signal integrity issues we might encounter at these lower speeds.

Transmission line effects and propagation delays. For circuit boards including a serial or parallel bus, there is a typical minimum speed (threshold frequency) at which a designer should consider transmission line effects such as reflections, EMI crosstalk and other issues, based on the physical length of the signal path (and a few other things). A widely accepted general rule of thumb is $1/10^{th}$ of the signal wavelength. Let's explore that a bit.

Consider the equation

$$\lambda = wv / f$$

where signal wavelength (λ) = signal propagation speed (wv or wave velocity) / frequency (f)

On a PCB, propagation speed is impacted by many things, including parasitic capacitances, impedance mismatches and reflections. But assuming our example contains a well laid-out circuit with minimal issues, the dielectric material effect can be approximated by:

$$wv = c / \sqrt{(\varepsilon)}$$

where propagation speed (wv) = speed of light (c) / square root of the relative permittivity of FR-4 dielectric material (around 4.5).

This equates to

$$wv = 3\times10^{8}m/s / \sqrt{(4.5)} = 1.42\times10^{8}m/s.$$

Let's say we're staying within a rather large, 10″x10″ PCB design. Consider 20cm (~8″) as a typical trace length of an

I^{2}C or UART bus. If we're estimating the frequency associated with a 1/10th wavelength, then we end up with:

$\lambda = wv / (f*10) \rightarrow f = wv / (\lambda*10)$

$f = (1.42\times10^8 m/s / 10*0.2m) = \underline{71MHz}$

Figure 1 shows a design containing an I^{2}C bus and a total signal length of over 17". A designer might run a sanity check on this to make sure they're still within a reasonable margin of seeing reflections and crosstalk.

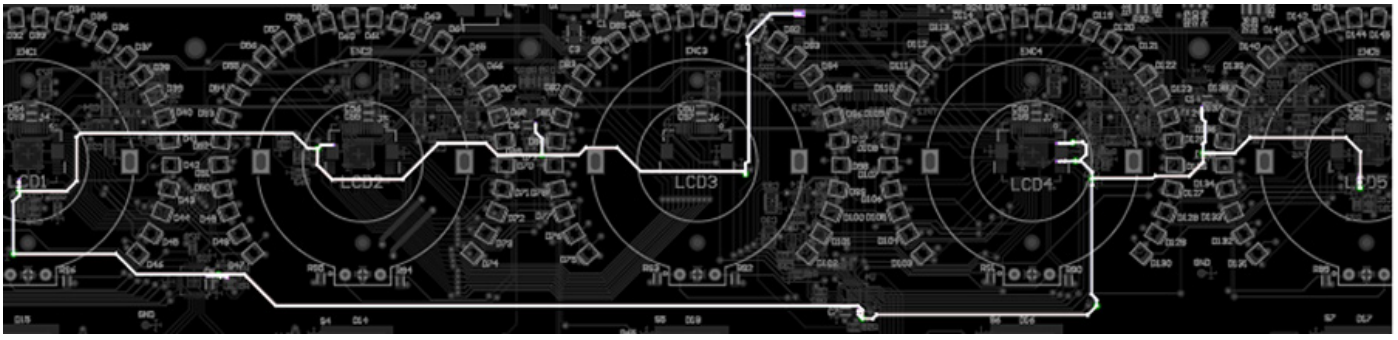


Figure 1. A circuit board design highlighting the "SCK" signal. Calculating frequency limitations for I^{2}C bus stretching over 17" (f = (1.42×10^{8}m/s / 10*0.43m) = 33MHz)). This is much higher than the expected data frequency, which may be up to 1MHz.

These 33MHz and 71MHz estimated threshold values fall within our 1-100MHz table including SPI, SD and RS485 applications operating at higher speeds and are well out of reach from slower protocols such as I^{2}C. As pointed out in the walkthrough above, other parameters can impact propagation speeds and greatly impact this threshold frequency if best practice is not followed. That includes impedance matching and some other tips included in this article.

Implementing the following design choices to applications, including the slower speeds (1-50MHz), can help keep propagation delays to a minimum as well as avoid crosstalk and typical EMI issues:

- Using the "star" topology in an I^{2}C application (and slower SPI speeds) is a myth and shouldn't have any major impact on signal integrity, as shown in the calculations above. If the bus isn't operating above the 50MHz range, then bus reflections likely won't occur. At some point, it *does* matter, and you'll want to avoid a "star" topology when laying out a communication interface. It's better to "snake" a bus around a PCB starting with the master or host at one end and the slave devices connected along the path rather than branching out in many different locations **(Figure 2)**.

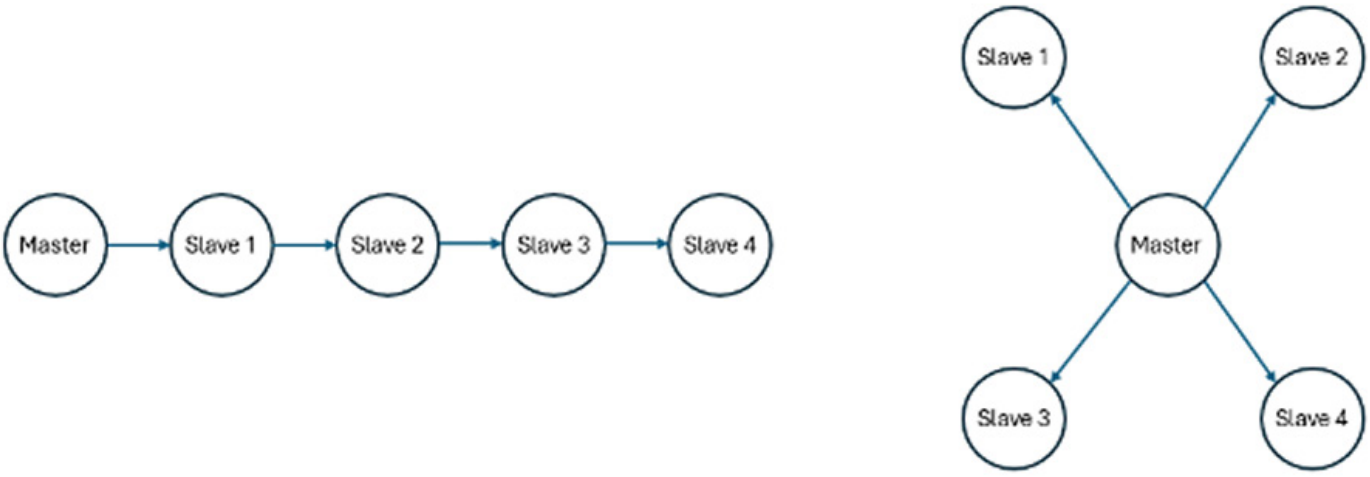


Figure 2. Daisy-chain (left) and star (right) topologies.

- Routing traces alongside a PCB edge increases the chances of EMI susceptibility from nearby, off-board radiators. Keep buses protected and if needed, establish a grounding barrier with vias to help keep EMI off board edges **(Figure 3)**.

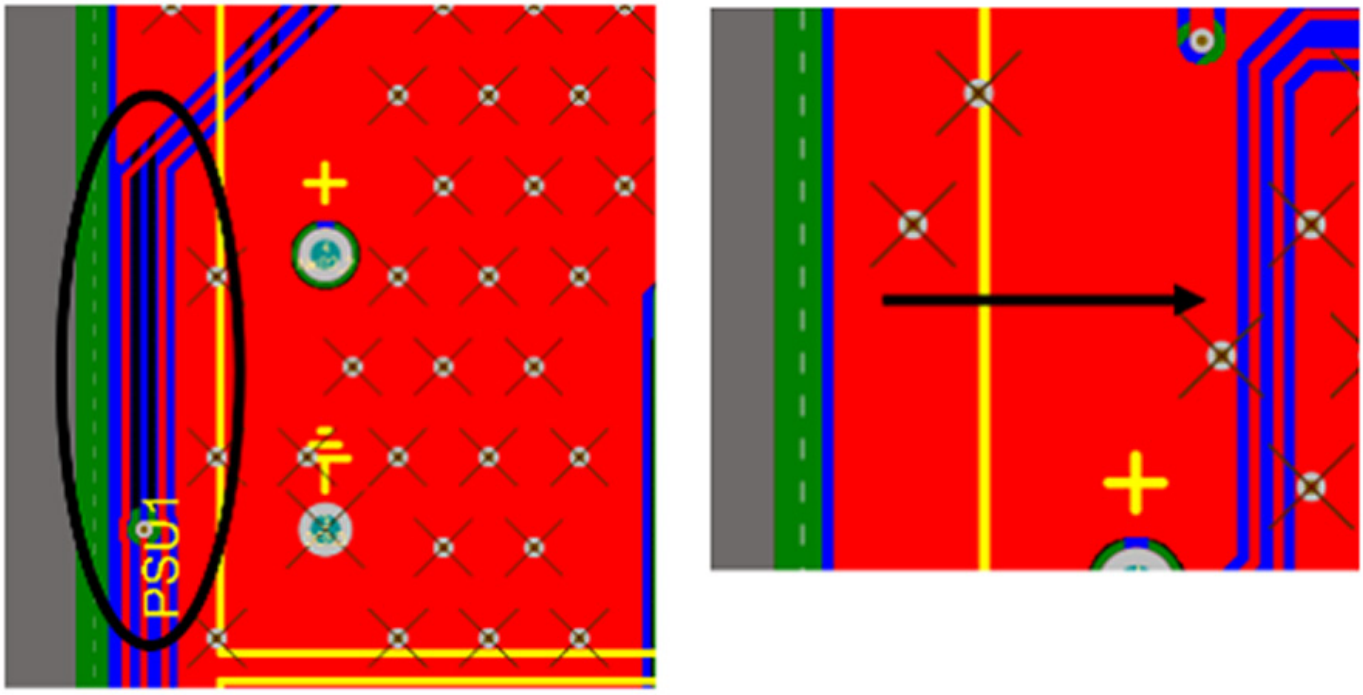


Figure 3. An example of an EMI-sensitive design containing a signal routed on the outer edge of a PCB. This should be moved off of the board edge and routed through the polygon pour.

- Limit the amount of vias used when routing signals from one layer to the next. In this speed range, it's best to limit the amount of vias (per signal) to no more than three.
- Pull-up and pull-down resistors typically have a positive effect on signals and help accelerate rise times or fall times while preventing stray signals, though depending on the driving circuit, they may require some tuning.

This improved propagation timing helps keep delays to a minimum and out of the danger zone with respect to transmission line effects **(Figure 4)**. The value of the pull-up/pull-down resistor is usually specific to the signal and its conditions, and often is recommended by a chip manufacturer or even an IEEE standard.

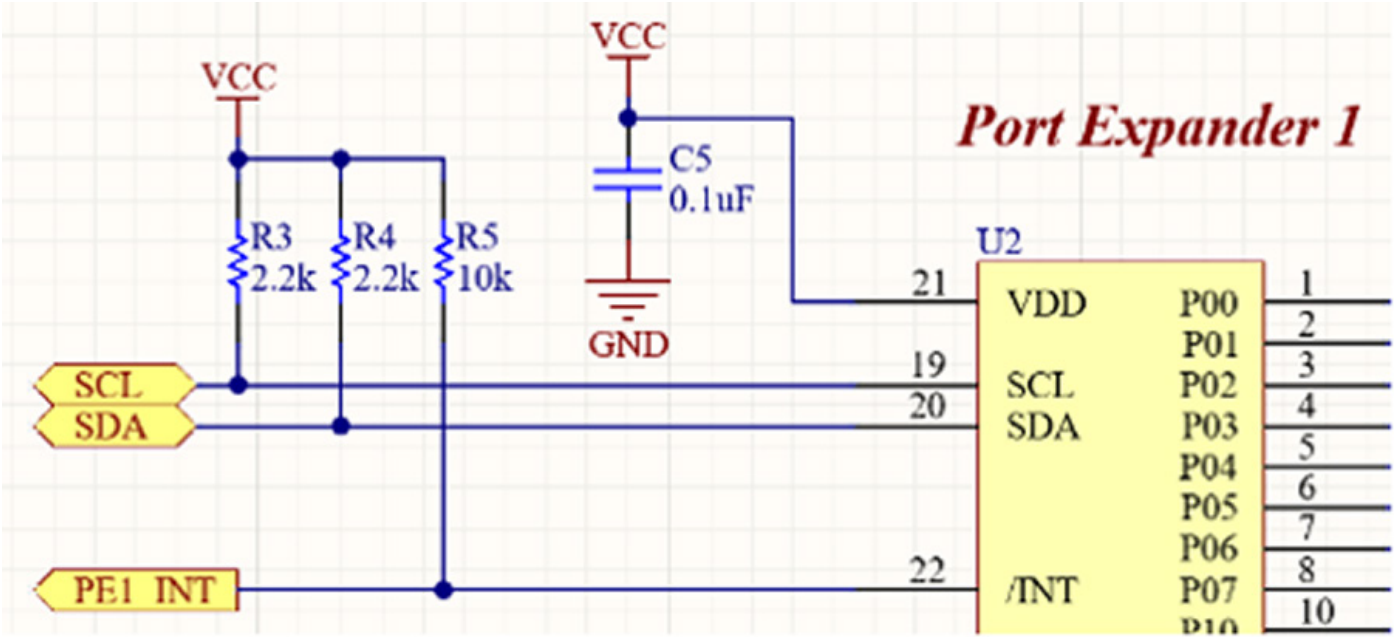
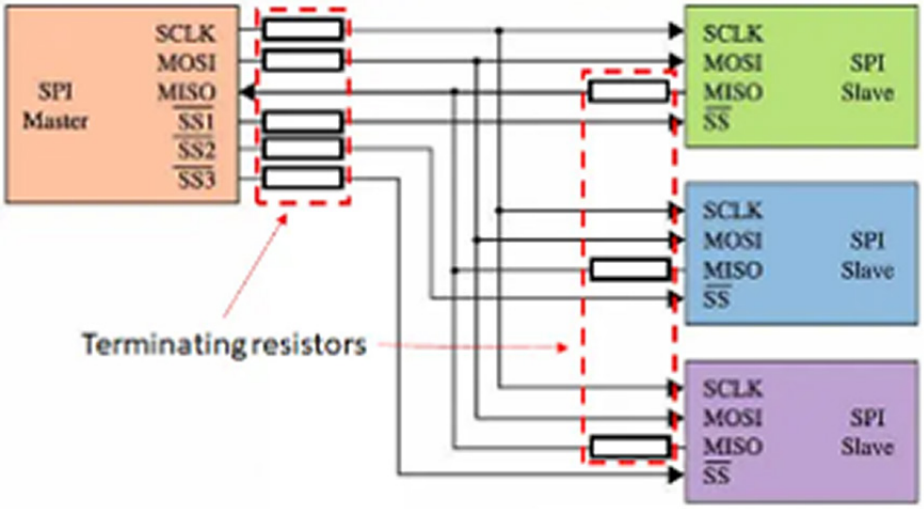


Figure 4. An example of a port expander's I2C bus containing a very typical 2.2kΩ pull-up resistance, while its interrupt signal contains another very standard 10kΩ pull-up resistance.

- For applications in the 50-100MHz domain that may experience some transmission line reflections, it's common to slow down the driving signal and dampen the ringing with the placement of a series resistor **(Figure 5)**. This can be done for longer SPI bus layouts where you place a resistor (typically 22-33Ω, which typically helps achieve a 50Ω target line impedance) in line with each source. Place these resistors near the MOSI, SCLK and CS pins at the master end and the MISO pin at each slave's end.



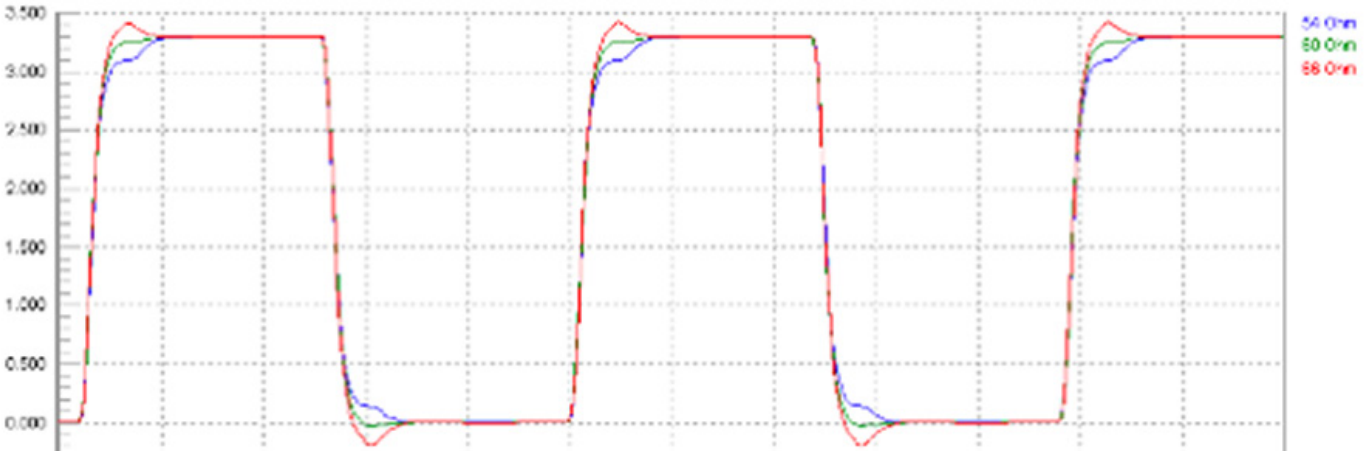


Figure 5. A schematic description of SPI bus termination resistors (top) and the impact of source termination resistors on a high-speed signal waveform (bottom)

High Speeds (100MHz to 1Ghz)

Now that we've discussed some of the basic details to consider at lower speeds, let's kick it up a notch.

Table 2 is another list of common, industry-standard interfaces that require closer consideration during PCB layout for higher speeds. Here we will focus a bit more on rise and fall time considerations.

Table 2. Industry-Standard Interfaces for Medium-High Speeds

100-500MHz	500MHz to 1GHz
DDR1 RAM	DDR2 RAM
PCI-e 1.0	DDR3 RAM
USB (high-speed)	
Ethernet (1000BASE-T)	
MIPI	
HDMI	
DisplayPort	

With clock and data frequencies operating above 100MHz, a designer must pay close attention to the relationship between rise time and frequency **(Figure 6)**.

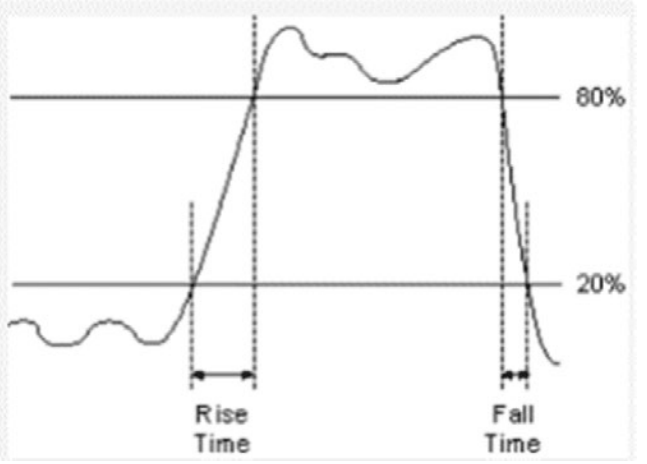


Figure 6. Rise and fall time visual indication of a signal.

In general, a rise or fall time is defined as the transitional period of a signal's edge, typically making up 10-90% of the edge, and ruling out the first and final 10% zones due to anomalies and differences seen in switching patterns from one device to the next (some have slow roll-off, etc.). A circuit can never support zero rise or fall time; it's impossible. This transition will always have some sort of delay. But the key is that it must support fast enough transitions to not lose valuable information at higher frequencies.

Going *too* fast may cause undesired effects as well. So, these rise and fall times must be characterized and controlled.

A good rule of thumb here when relating expected rise or fall times to frequency is:

$$T_{R/F} = 1 / (f * \pi)$$

For a frequency of 100MHz, a designer should expect (or strive for) a rise or fall time on the order of 3-4ns. 500MHz should be more in the 0.5-1ns range. We can use this to determine what an acceptable trace length would be for a given signal, and we'll see here that they are proportional to each other.

Another general rule of thumb: the critical or maximum trace length for a given signal should permit a propagation time of no longer than half the rise or fall time. This can be written as

$$\text{Critical trace length} = wv * \tfrac{1}{2} T_{R/F}$$

Let's apply this to an example. Say that we have a 100MHz signal, which is estimated to have around a 3ns rise time. Incorporating our previously calculated propagation speed of 1.42×10^{8}m/s, we get the following

$$\text{Critical trace length} = (1.42\times10^{8}\text{m/s} * 3\times10^{-9}\text{s}) / 2 = 21\text{cm } (\sim8'')$$

Applying this same formula to something operating at 500MHz produces a much shorter critical trace length:

$$\text{Critical trace length} = (1.42\times10^{8}\text{m/s} * 0.6\times10^{-9}\text{s}) / 2 = 4\text{cm } (\sim1.6'')$$

These calculations assume (as was done before) that our propagation delays are minimal. Any negative impacts to this propagation timing or the rise and fall times (such as parasitic capacitance, inductance due to ground bounce, reflections, etc.) greatly impact this critical length, and it's why we must incorporate more rigorous tips/tricks with the PCB layout.

Here is a list of higher-speed tips and tricks for the 100MHz to 1GHz range:

- At these speeds, a clean power source needs to be used for all digital ICs involved. This includes using higher-quality ceramic capacitors like MLCCs that are good at reducing local EMI, decoupling noise and reducing voltage ripples. Use linear regulators whenever possible, but if incorporating a switching supply, make sure to source a quality, low-noise supply and implement a good practice layout for the switching paths to minimize board parasitics and transients **(Figure 7)**. Also, be generous with ferrite beads, especially if a power source is coming from an off-board source.

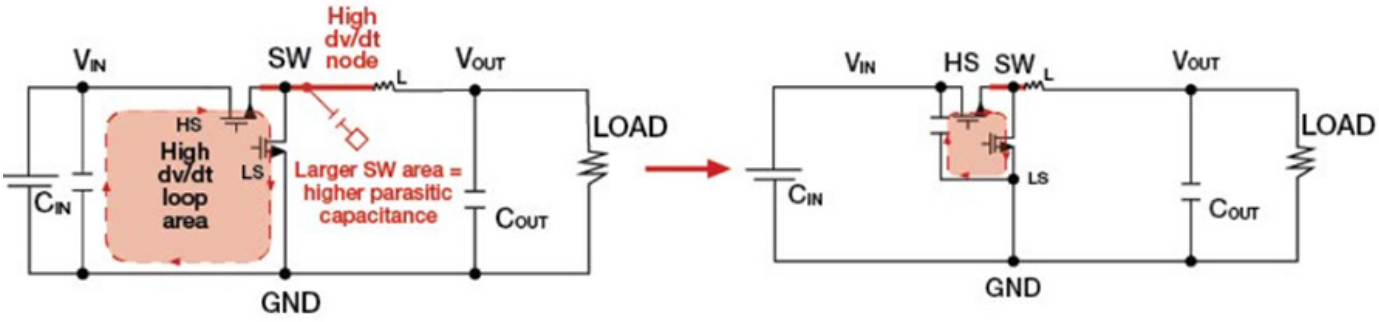


Figure 7. Effects of a larger SW area/trace length, resulting in more parasitic capacitance and unstable regulation.

- Impedance control greatly helps reduce reflections, crosstalk and inductive coupling. Impedance control involves many factors, including PCB stackup materials and their dielectric constants, trace width, thickness and spacing. PCB materials and controlled-build specifications become much more crucial beyond 1Ghz, as we'll see in the next section. Length tuning is part of this impedance-matching activity and ensures minimal differences in propagation delay between signal pairs. Serpentine routing on differential pairs is the ideal form of length tuning for interfaces that contain several lanes of differential pairs (all of which need to be tuned together) **(Figure 8)**.

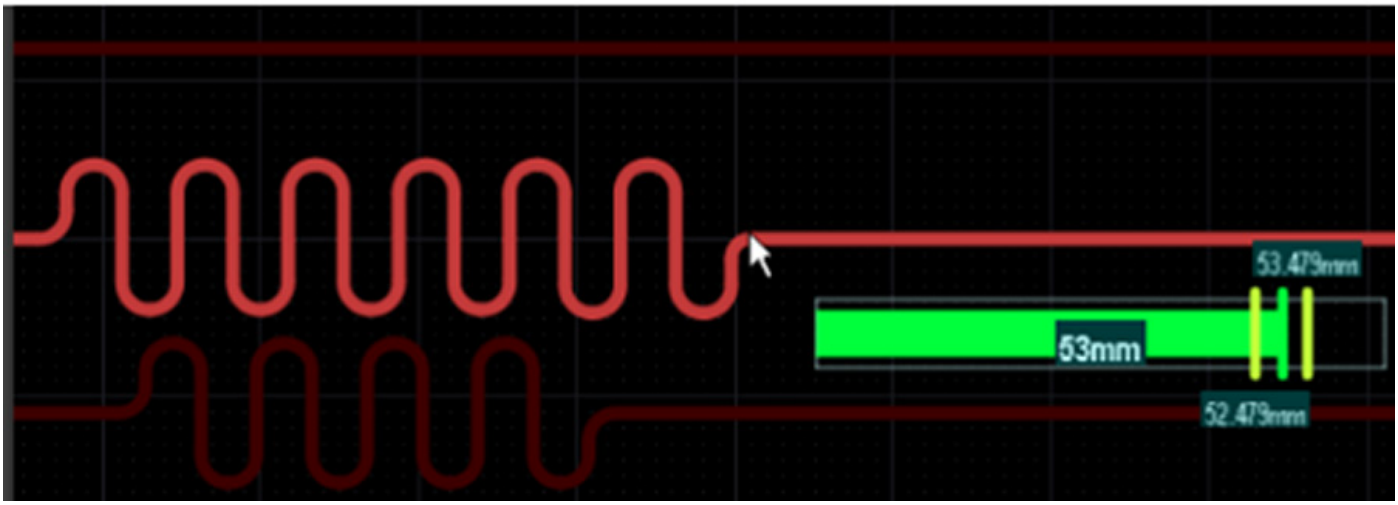
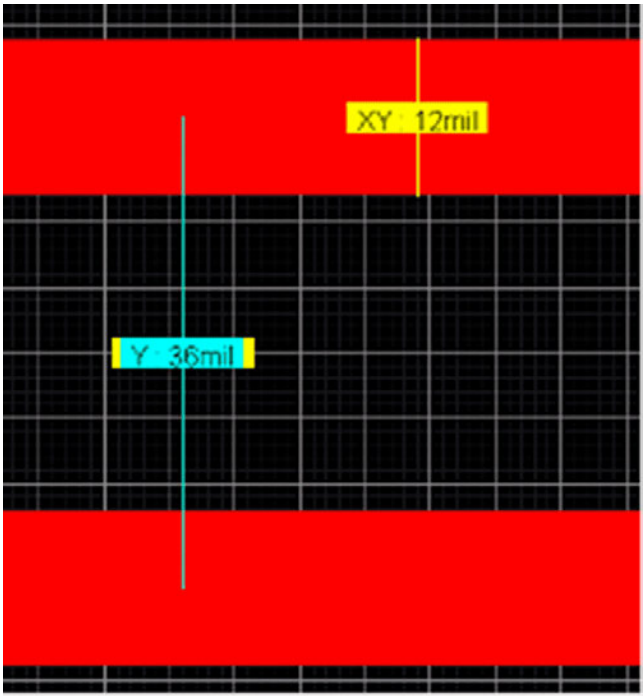


Figure 8. An example of serpentine length tuning.

- The well-known "3W" rule for impedance control states that, to minimize crosstalk between two traces, the designer should permit a minimum spacing between the differential pairs equal to three times the width of the track (measured from center to center of the trace) **(Figure 9)**.



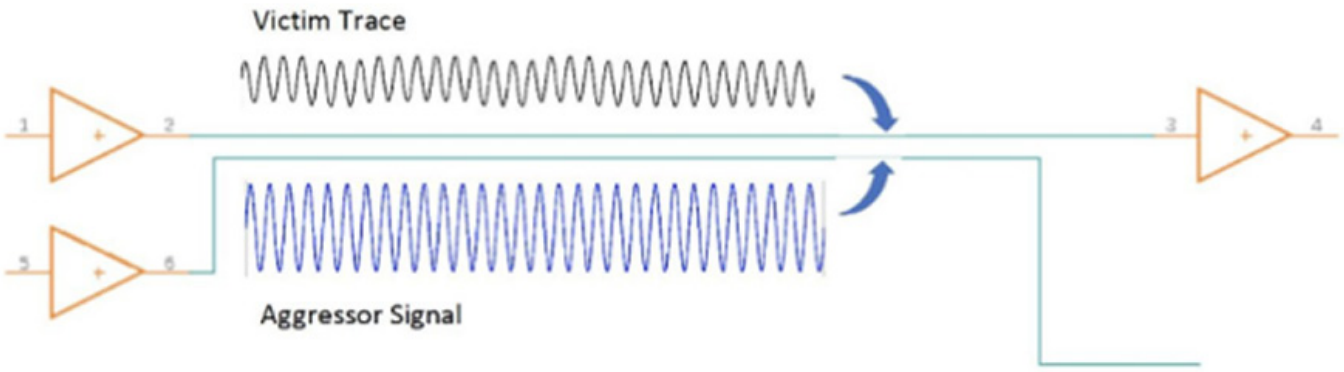
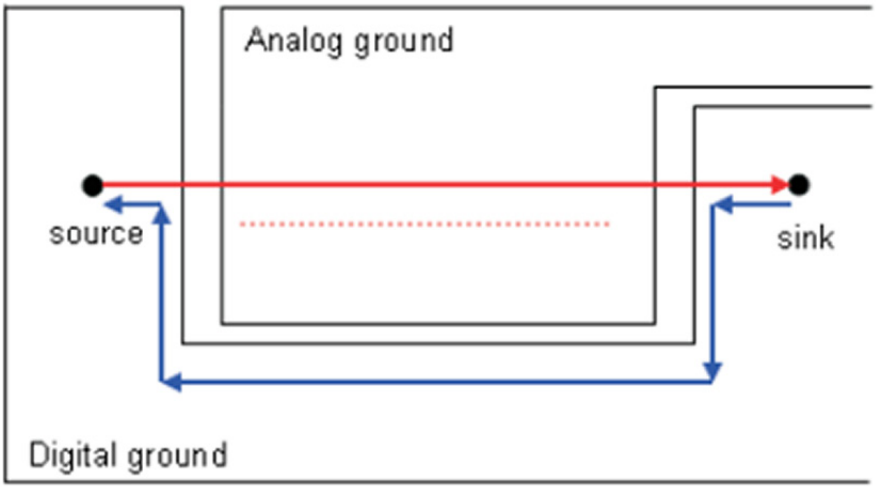


Figure 9. An example of a differential pair including 12-mil traces, separated by three times the width of the track (36 mils).

- Implement shielding wherever possible, including the use of ground planes, stitched vias and off-board connections.
- Layer stackup is important, especially if internal layers are used for routing sensitive signals. Ground planes can be used as shields for applications involving several layers and can also be used to minimize crosstalk by maintaining sufficient spacing between signals and planes. A designer can implement "plane pairing," which is similar to having adjacent power planes and signal planes reduce current loops and lower EMI radiation.
- Avoid using vias on data and clock signals in general. Using vias on high-speed signals extends their length and exposes them to innerlayers, increasing opportunities for inductive coupling and EMI impacts. If vias must be used, avoid stubs (use blind and buried vias) as these can cause reflections.
- Avoid routing sensitive signals across two different planes or over top of other (unshielded) nearby signals on different layers **(Figure 10)**. If you must, route the traces such that they cross in a perpendicular direction rather than parallel.



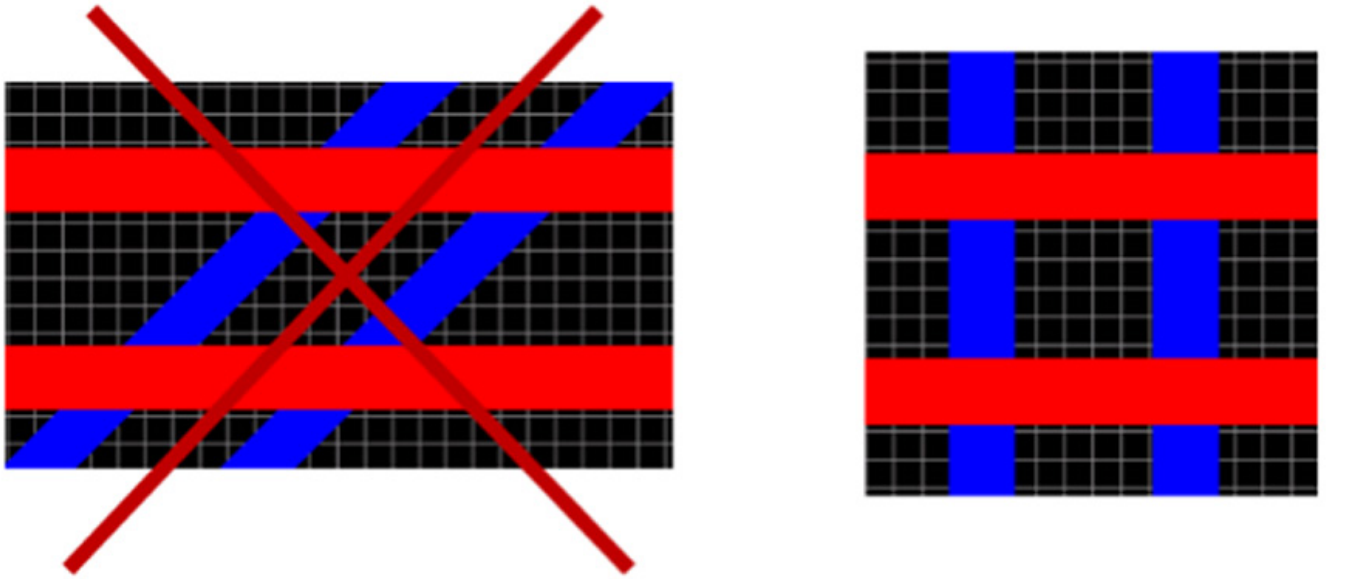


Figure 10. Route a sensitive signal overtop its reference ground and not across other ground reference planes (top), and route high-speed signals in a more perpendicular fashion with respect to traces on other layers (bottom).

Super Speeds (1Ghz to 10GHz)

Finally, we arrive at super speeds. These are the fast digital interfaces used today and require the utmost attention to detail during PCB layout. Rise and fall times will be in the picoseconds so the associated trace lengths and EMI protections are critical.

At this level, it is crucial to understand the fabrication and layer stackup specifications, as well as communicate those to the PCB vendor for DfM feedback.

Table 3. Industry-Standard Interfaces for High-Super Speeds

1GHz – 10GHz
DDR4 RAM
DDR5 RAM (up to 8.4GHz!)
PCI-e
USB 3.x
Thunderbolt

Here are some considerations for these super-speed applications:

- Use PCB materials with a low dielectric constant to minimize timing delays. Higher-performance materials such as PTFE may drive cost but provide lower losses at higher frequencies. Work with your PCB vendor on recommended materials and cost/benefit tradeoffs and utilize layer stackup tools.
- Understand when to use microstrip (outer layers) and stripline (innerlayers) for routing data and clock signals,

and how to configure ground planes associated with the signals. Impedance control will be different for outer layers versus innerlayers and should be calculated using CAD. Also, be sure to understand the source and load characteristics of these traces.

- Be generous with ground planes in designs featuring several layers. Each digital interface may require its own designated innerlayer with ground planes above and below to shield from EMI as well as provide minimized ground loops and clean return paths. Try to keep all byte lanes on the same layer if possible, but if needed, then alternate the byte lanes across two different layers. **Figure 11** shows several layers containing high-speed signals. Some layers are paired with others and are part of the same bus, such as orange and purple.

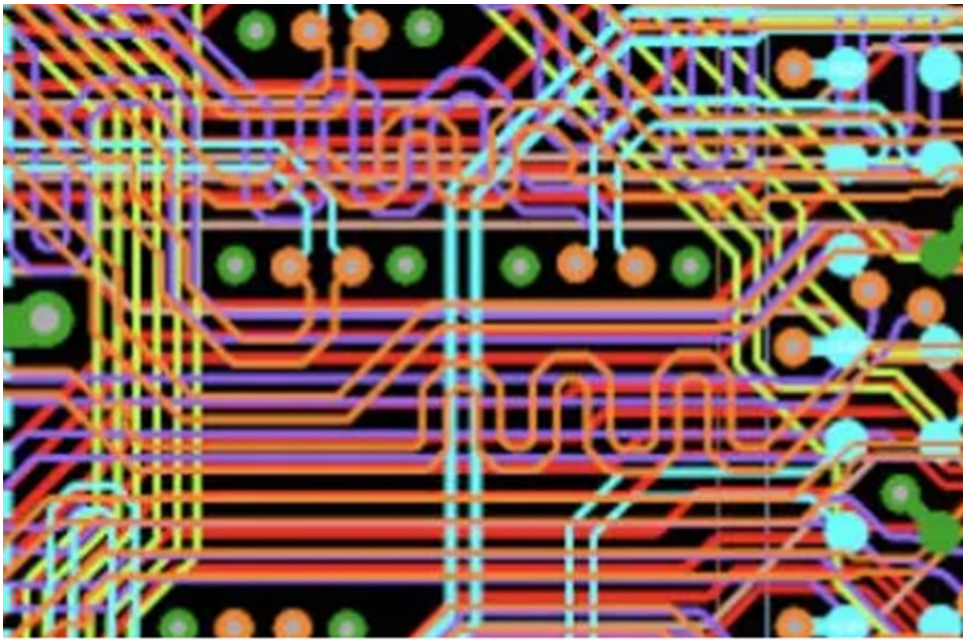


Figure 11. An example of multiple high-speed lanes routed on several inner layers, some of which are part of the same bus.

- While adding layers to a design, keep an eye on layer stackup symmetry to provide mechanical stability. This includes evenly distributed copper across the stackup, which should prevent warping.
- When routing clock and data traces, maintain the critical length rule described in the previous section. It's also ideal to avoid any corners at all (even 45° bends), and keep all traces serpentine if possible. Right angle traces can act as antennas and cause radiation due to added capacitance in the corner. Minimize this by rounding off the corners of sensitive signals **(Figure 12)**.

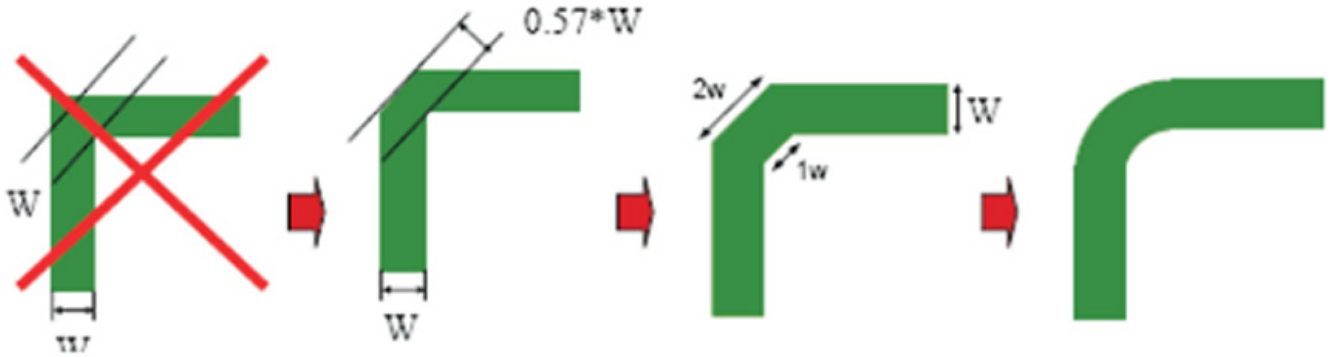
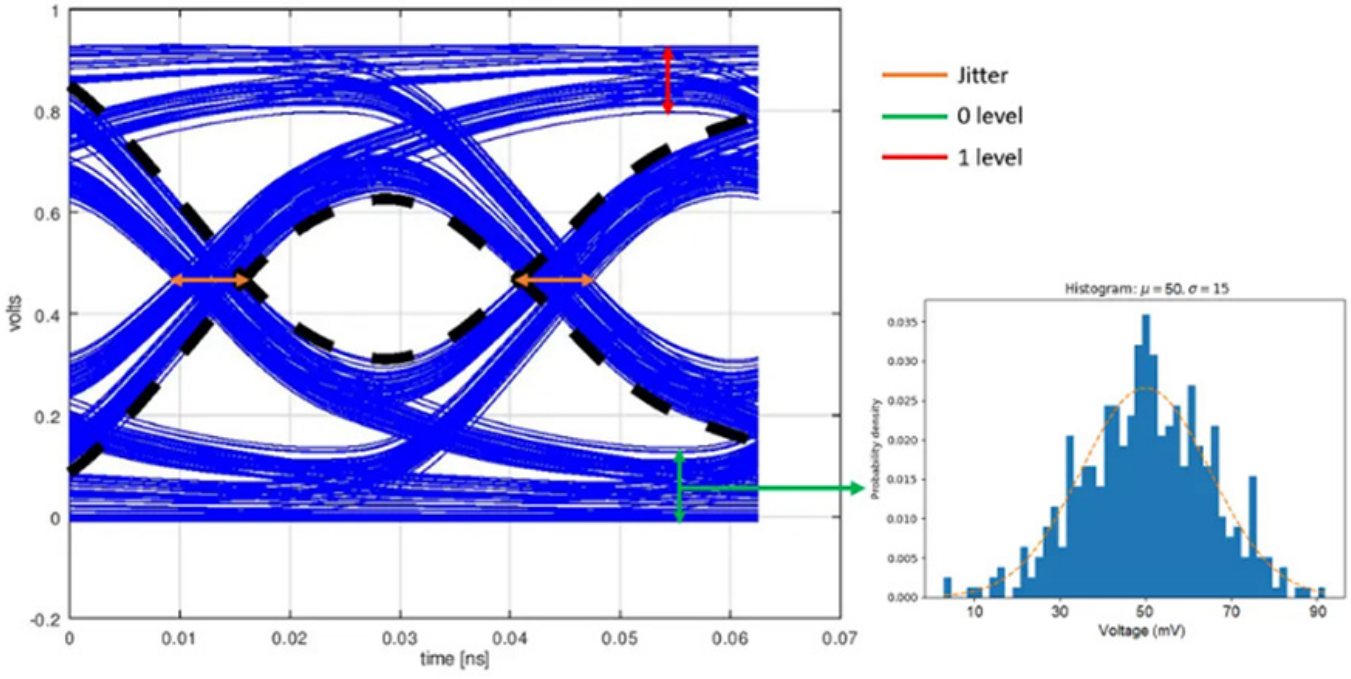


Figure 12. An indication of poor and good right-angle bends

- High frequency typically translates to high heat. Make sure to plan on thermal management and proper heat dissipation including thermal vias, heat sinks and polygon pours.
- Simulate and test your designs as much as possible. This includes eye diagrams, thermal management, insertion/return loss and voltage ripple on associated power rails. Eye diagrams (which can be both modeled and tested) provide a great metric for jitter and timing as well as ensuring that data and clock signals fall within the acceptable limits of a standard **(Figure 13)**. Thermal management can typically be modeled and reveal potential hotspots, but should be measured on prototype designs. S-parameters are used to characterize high-frequency behavior and include analysis of expected losses and transmission efficiencies. Depending on the manufacturer, low-noise power supplies can typically simulate voltage ripple and loading effects.



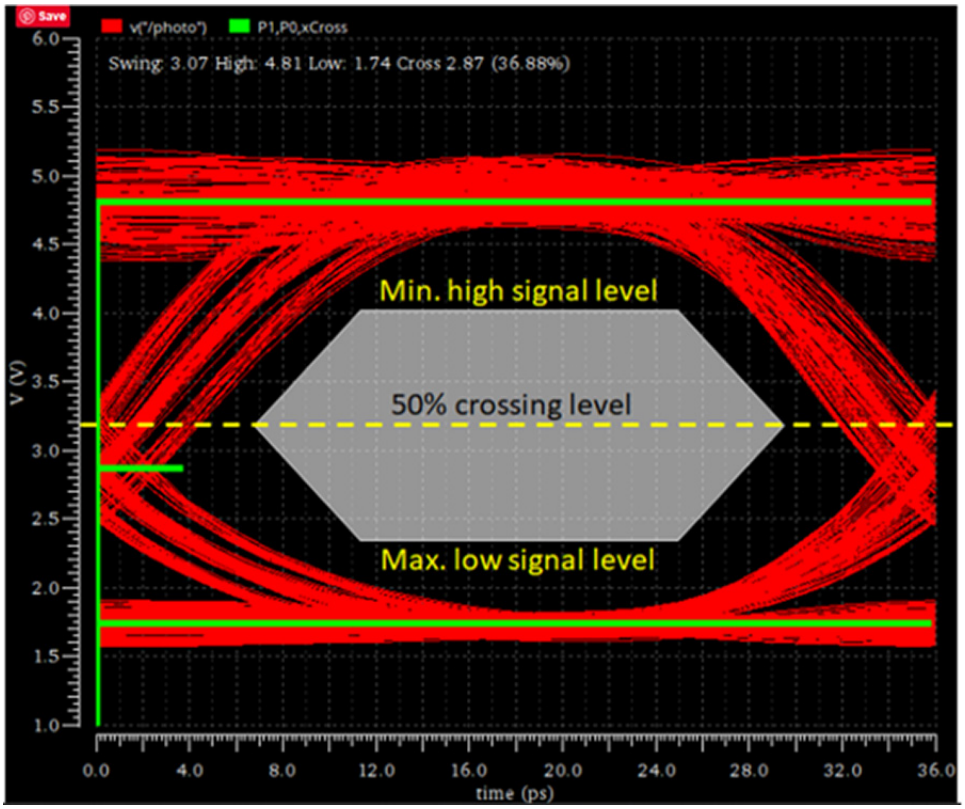


Figure 13. An eye diagram indicating jitter and normal distribution of 0-level (top), and a demonstration of how to interpret an eye diagram and ensure that all signal traces stay out of the mask area (bottom).

- Finally, it is always ideal to build a good relationship with the board supplier and ensure that proper DfM feedback is provided, as well as guidance in many aspects such as material selection, clearances and tolerances, and layer stackup. Begin by basing your design on vendor design rules. Don't wait to check to learn you're following a reasonable set of specifications.

Ultimately, it helps to know when to incorporate the proper rigor for PCB layout and it's important to understand the physics involved with these widely accepted rules of thumb.

By understanding the fundamentals behind signal integrity at higher frequencies, you're less likely to end up with a design with reliability problems during both initial board bring-up and system integration. And there will always be a tradeoff between cost and complexity.

By consulting with your PCB vendor regularly and performing due diligence upfront, a designer can find an ideal balance that is both cost effective and high performing.

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ENGINEERING *TOMORROW'S* ELECTRONICS

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Registration Details Coming Soon!

Dendrite Growth Dynamics

Are industry standards sufficient for characterizing the effects of cleanliness at high voltages?

by ADAM KLETT, PH.D.

The increasing popularity of high-voltage electronics, particularly in electric vehicles, underscores the need to address the quality assurance and reliability challenges linked to these technologies. Standards, such as those published by IPC, are a great way to accomplish this. A crucial step to ensure the proper application of standards is to tailor them accordingly. For high-voltage electronics, an initial part of this process involves defining high voltage. Different organizations have already put forth their definitions.

For instance, the International Electrotechnical Commission (IEC) and British standards stipulate that anything above 1kV AC or 1.5kV DC constitutes high voltage. On the other hand, the American National Standards Institute (ANSI) categorizes high voltage as ranging from 115-230kV, extra-high voltage as 345-765kV, and ultra-high voltage as exceeding 1,100kV. When referring to IPC standards, however, which are more pertinent to the electronics domain, a provision in IPC-J-STD-001H states that the definition of high voltage hinges on the specific application.

For the scope of the arguments presented here, as the focus is on SIR testing and most SIR is conducted at 5V, it is reasonable to define anything above 5V as “high.”

High-voltage electronics are not new. Humans have been engineering products with high voltages for many decades including power transmission, scientific equipment like plasma treatment or MRI equipment, and even older CRT TVs found in many households a few decades ago. But if this is the case, why are high-voltage electronics still at the center of discussions at many industry meetings?

Considering the examples, they all have a few things in common. First, except for power transmission equipment, most high-voltage equipment lived in temperature- and humidity-controlled environments; if they didn’t, the cost of failure was relatively minimal. Second, although the instrument price might have been high, there was very little to no risk to human life.

To restate the answer, it’s all about reliability. With the advent of software-defined vehicles, which are essentially cars built around electronics, we are quite literally putting high voltage into the hands of the consumer. I am not necessarily referring to the charging adapters, but all the electronics inside of the car, which, if they fail, could cause serious injury or death. Imagine a dendrite being the cause of a car crash.

Given that high-voltage electronics have been produced for so long, one would think that there would be a well-

established set of standards for manufacturing these high-reliability electronics. There is no argument that some electronic assemblies are deployed in harsh environments. Pick your favorite summer beach destination and imagine the stress those electric vehicle charging stations undergo. Huge temperature swings between direct sunlight and a cool, breezy night, rain every afternoon, salt spray from the ocean, and insect infestations that love to nest inside. Unfortunately, these are the environments to which these electronics are deployed, yet they are not being built to the standards required to ensure reliability. Things like good manufacturing processes (cleaning and coating) and, most importantly, testing of the assemblies, are key to reliability.

Is Elevated Voltage Testing Needed?

This work focuses on testing, specifically for dendrites in high-voltage applications. IPC has established performance classes to reflect the functional performance requirements, testing rigor and frequency. Class 1 electronics are those general electronic products where cosmetics are unimportant and failure is not impactful: devices like toasters or a light-up chew toy for a pet. Class 2 electronics are those dedicated service electronic products where high performance is required, and while uninterrupted service is desired, it is not critical. This classification includes equipment like an MRI machine. Class 3 electronics are those destined for high-reliability or harsh operating environments where continued performance is critical, downtime cannot be tolerated, and failure could mean the loss of human life. Among other requirements for Class 3, thorough cleaning and testing are essential.

The concern arises as to whether electronics operating at high voltages should be subject to testing at those elevated voltages or whether the conventional 5V test is deemed adequate. To navigate this question effectively, it may be helpful to review the current industry standards. IPC-J-STD-001, Section 8 on cleaning and residue requirements mandates the provision of objective evidence to demonstrate that a cleaning process results in an acceptable level of flux and other residues. This can include historical evidence, while surface insulation resistance (SIR) testing is recognized as a suitable measure to establish cleanliness for those lacking historical data.

To understand how SIR can be useful in providing the objective evidence needed to qualify a cleaning process, it is first necessary to understand that SIR is a measurement of the electrical resistance across two conductors on the surface of a circuit board. The idea is that the higher this resistance, the lower the level of contamination and the higher the reliability. In **Figure 1**, we see an example of a SIR coupon, which contains a BGA, a QFP, some QFNs, and a bank of capacitors; however, these can be designed to contain any number of various components to be representative of a specific assembly.

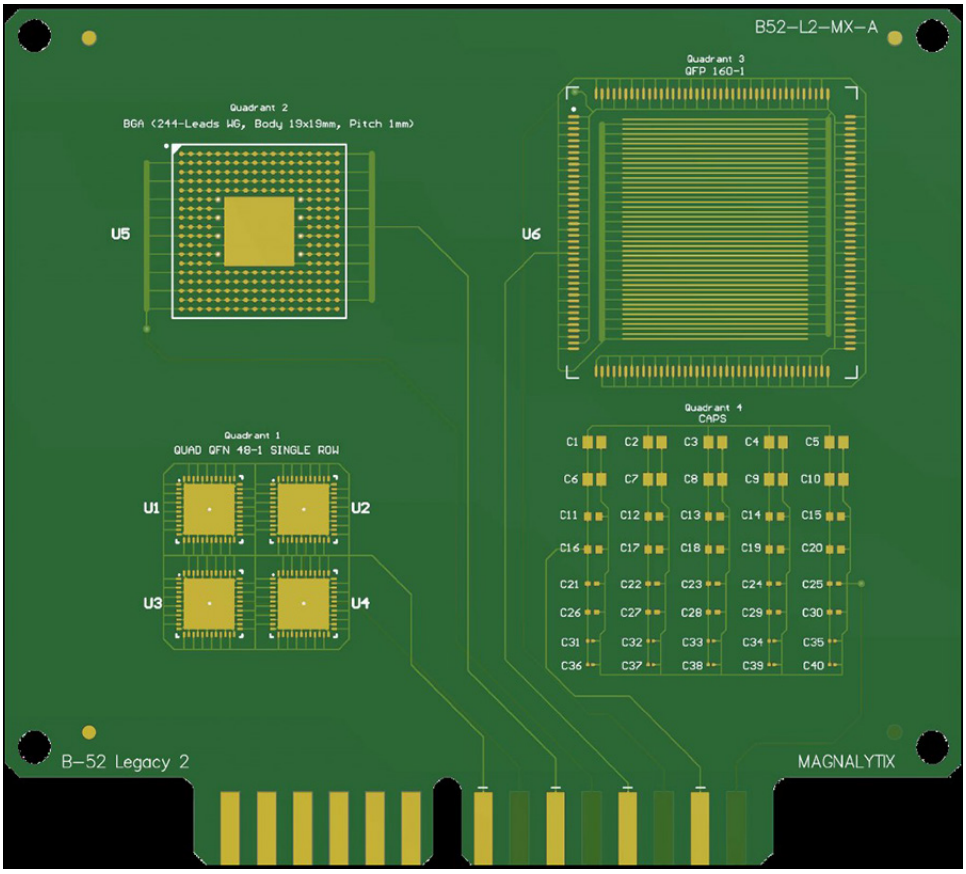

Figure 1. The SIR coupon was assembled with aBGA, QFP, QFNs and capacitors.

An SIR measurement is taken by first letting the representative coupon equilibrate in an environmental chamber. Typical conditions are 40°C and 90% relative humidity (RH), although other conditions can be used. A bias voltage of 5V DC is applied across the pattern, and the resulting current is measured. This current is then converted into a resistance using Ohm's law. Measurements are then taken over the course of seven days. If, at any point during that time, the resistance value drops below a certain threshold value, then the test is considered a failure.

One aspect of this measurement that is commonly overlooked is the part about using Ohm's law to calculate the resistance. Ohm's law states that the current in a conductor is directly proportional to the applied voltage, which most people know as V=IR. However, the argument can be made that this is not the correct model for an SIR coupon. On an SIR coupon in an environmental chamber, many mechanisms contribute to current flow between the conductors, including electrolysis and reduction/oxidation reactions that may or may not be linear in nature (i.e., obey Ohm's law). As seen in **Figure 2**, this is not a simple conductor.

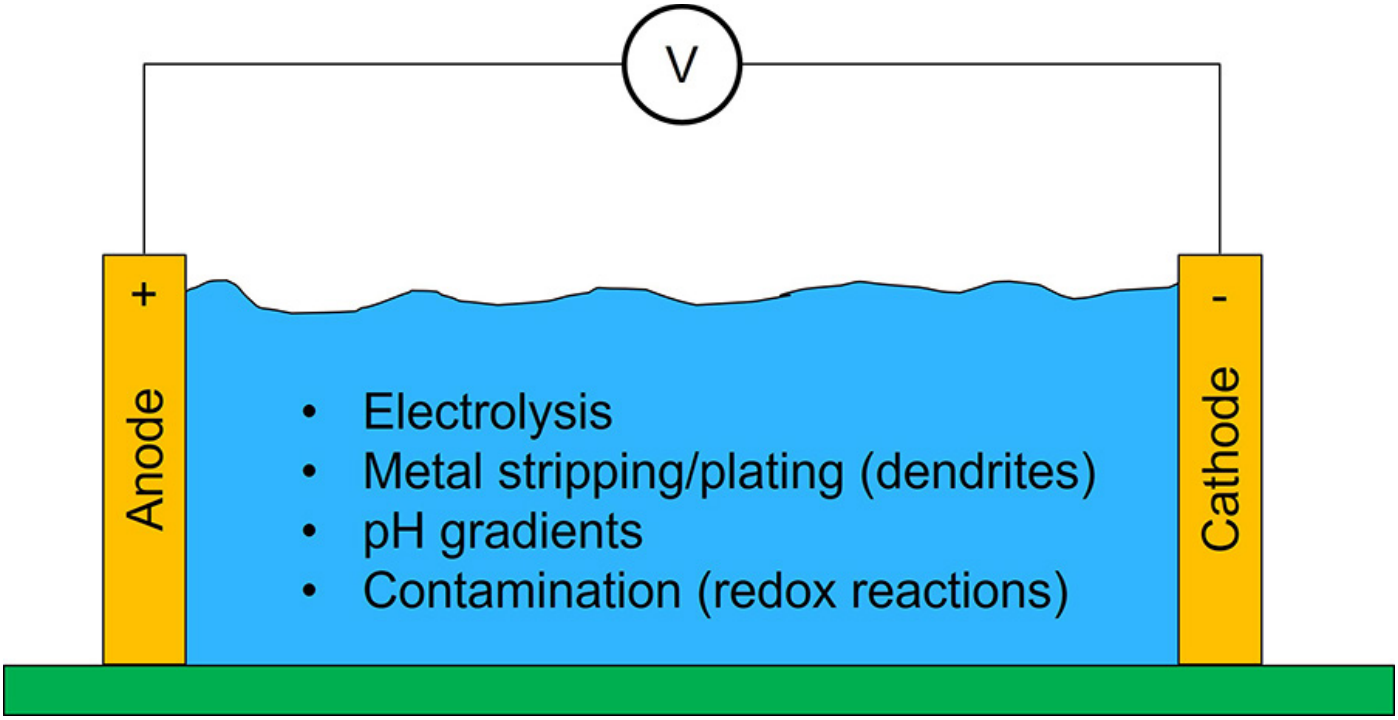

Figure 2. A visualization of some of the many mechanisms that contribute to current flow between the conductors.

Given these arguments, the question remains whether the current standards and test methods are applicable to these samples. Specifically, the time, temperature, RH, and pass/fail criteria. High voltages can affect materials by aging them, or if the voltage is high enough, it can experience dielectric breakdown. Also, the dynamics of dendrite growth at these higher voltages are under question. Do they grow faster or slower, and what role does contamination play in this?

Current IPC testing standards – IPC-J-STD-004C, 3.3.1.4 – state the SIR requirements for fluxes shall be determined in accordance with IPC-TM-650, Test Method 2.6.3.7, except that the test duration shall be 168 hr. The requirements for passing the SIR test are that all SIR measurements on all test patterns shall exceed the 100MΩ requirements after 24 hr. of exposure. That is the extent of the guidance given, unfortunately. There is no discussion about how higher voltages may affect the measurement.

SIR Test Protocol

Among the issues, dendrite growth dynamics is in question. A series of tests were carried out to understand how higher voltages affect dendrite growth. SIR test coupons were used to measure dendrite growth speed. One set of coupons was left clean, while another was contaminated with a commercial off-the-shelf no-clean wave solder flux. A droplet of DI water was placed on the surface to bridge two conductors. Various test voltages were applied up to 50V DC, and the time for a dendrite to grow across the 20-mil gap was measured.

Although applying bulk water droplets across the SIR pattern may not represent the adsorbed water layers on the surface during an SIR test, it can be argued that the mechanisms for ion diffusion through the water layer are similar. The tortuosity of the diffusion path in a thin layer will significantly affect the speed, and the results from this work will be orders of magnitude faster than would occur on a humidified board. The relative speeds of dendrite growth are

of interest here to illustrate the effects of voltage and contamination, however.

Test Results

Figure 3 shows dendrites growing on clean substrates after 150 sec. at the stated voltages. Compared to dendrites grown on the contaminated boards after only 60 sec., a significant difference is seen **(Figure 4)**.

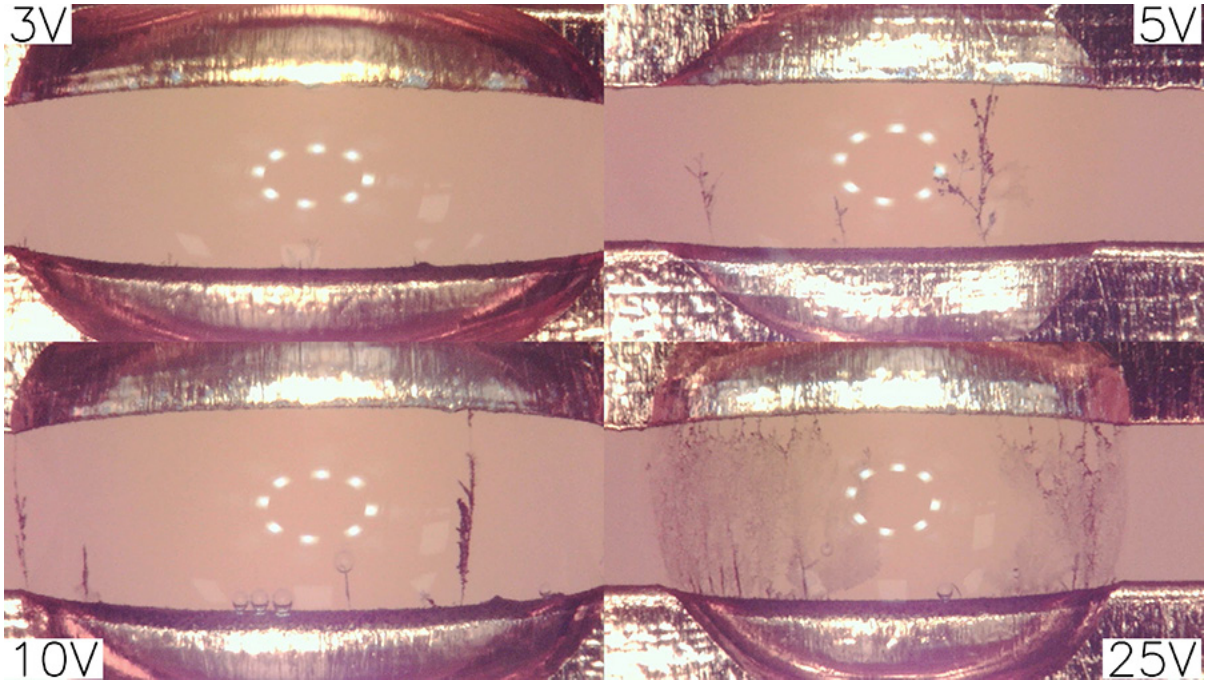

Figure 3. Dendrites growing on clean substrates after 150 sec. at the stated voltages.

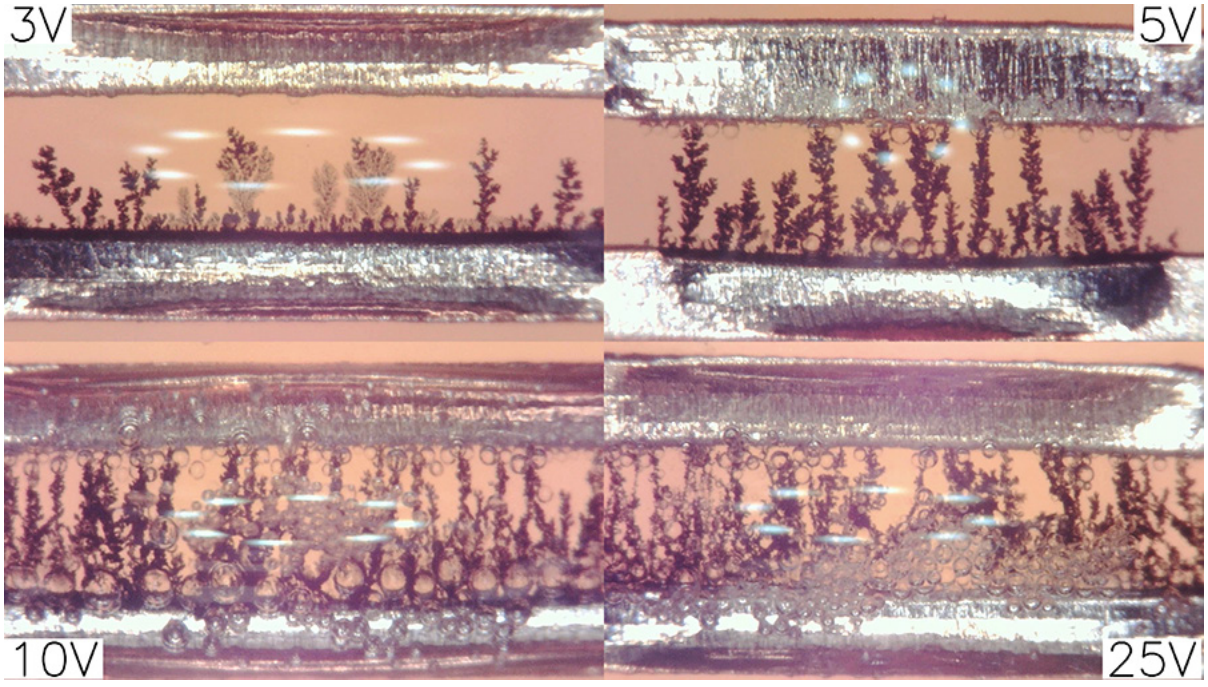

Figure 4. Dendrites growing on the contaminated boards after only 60 sec.

Qualitatively, the dendrites grow faster at higher voltages, regardless of contamination. However, they do grow significantly faster if the surface is contaminated. Another important observation is that more dendrites formed on the board in the contaminated samples. In the clean samples, only around five to 10 dendrites formed, whereas significantly more formed in the contaminated samples. Also interesting to note is that different dendrite morphologies exist. For example, the dendrites that formed at 25V on the clean sample are more ornate and coral-like, whereas the dendrites grown at the lower voltages look more like tree roots with only a few branches. At this point, the root cause of this difference is unknown.

Time measurements at each applied voltage were plotted and can be seen in **Figure 5**. The first thing to note is that the data was repeatable over the entire voltage range of 3-50V illustrated by the relatively small error bars. At 50V, the time to failure was less than one second and not measurable with the experimental setup. For this reason, voltages above 50V were not examined.

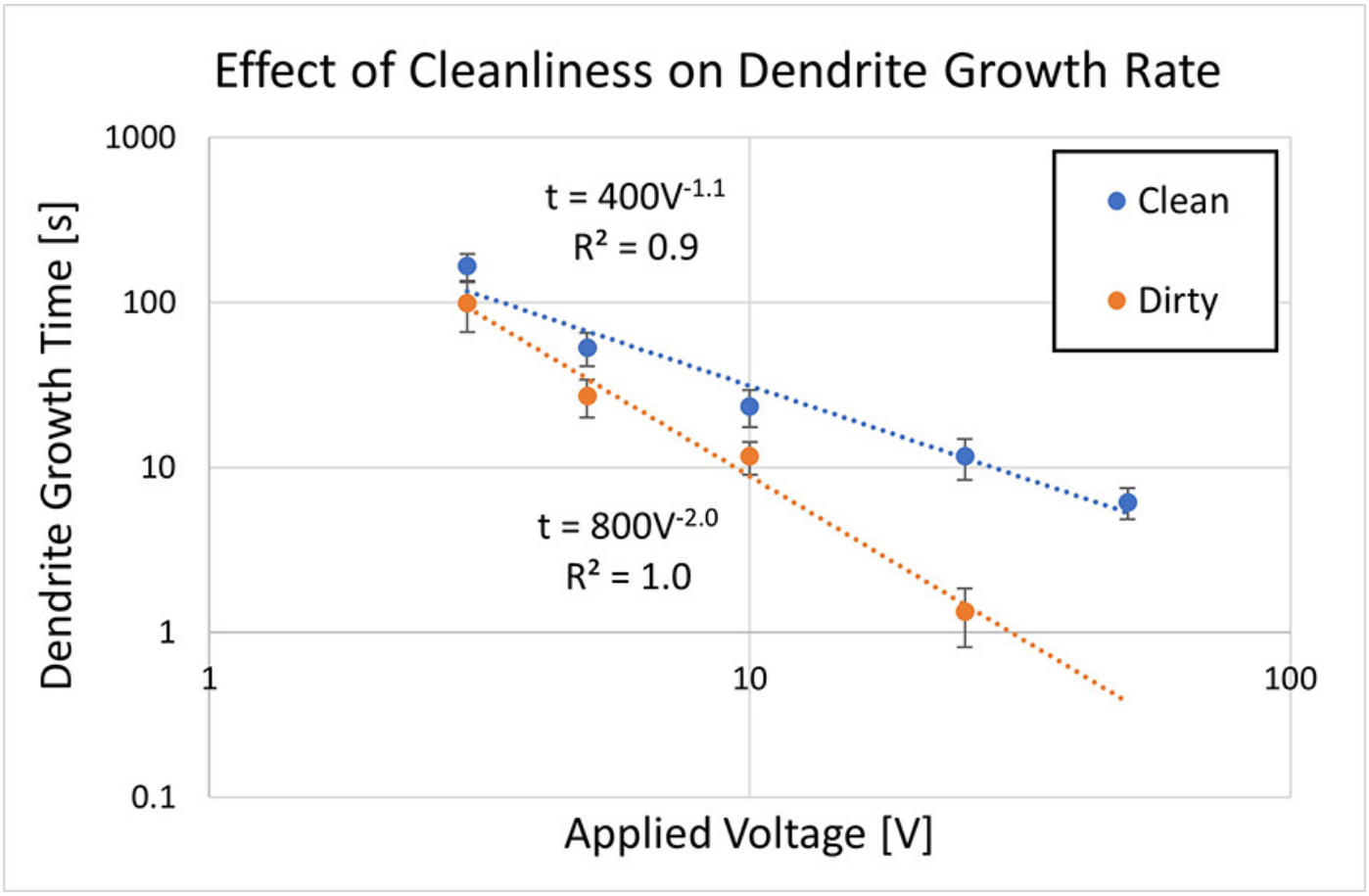

Figure 5. A plot of dendrite growth time and voltages on clean and contaminated boards.

What was observed in the videos can be seen quantitatively in the data. That is, higher voltages produced dendrites faster, regardless of cleanliness. This can be seen by the downward slope of the best-fit line (i.e., higher voltages took less time to grow a dendrite). Also, the dirty samples were faster across the board than the corresponding clean samples. The data also fit well to a power law relationship; the dendrite growth time of the clean samples was seen to be proportional to the inverse of the applied voltage while that of the contaminated samples was seen to be proportional to the inverse of the applied voltage squared. This suggests, not surprisingly, that other mechanisms are contributing to dendrite growth.

To visualize some of these mechanisms, a pH indicator was added to the water droplet, and the experiment was repeated. In **Figure 6**, a water droplet with phenolphthalein spanning three conductors can be seen approximately one minute after applying a 15V DC bias. PH gradients can be seen forming, as evidenced by the pink areas. Convection currents establish themselves within the droplet, and the pH gradient does not travel uniformly across the gap but ends up traveling in distinct lines. This further illustrates that the conditions on the surface of the board are not simple and homogeneous.

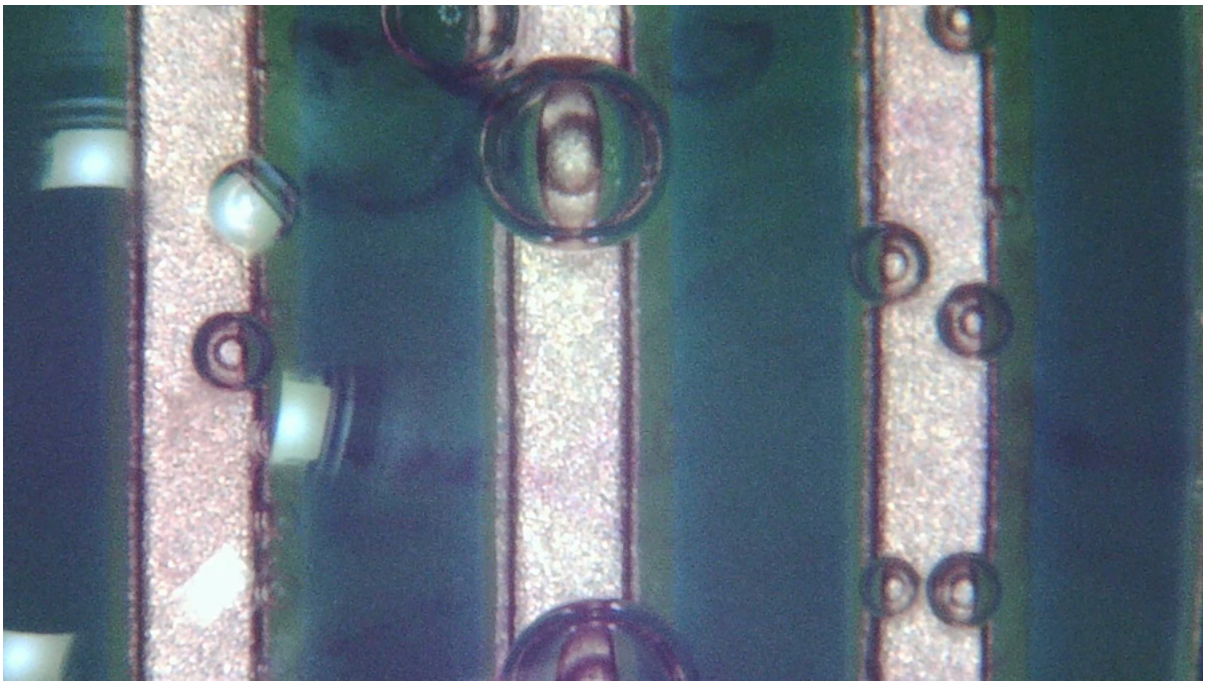

Figure 6. A water droplet and pH gradients can be seen on the board, demonstrating other mechanisms contributing to the dendrite growth.

Based on the results of this work, we can conclude that dendrites grow faster at higher voltages, and contamination exacerbates that growth. We also see that the dendrites are much more prevalent when contaminated. This is somewhat relieving as it suggests that the current SIR testing parameters, namely time under test, will bound potential failures. In other words, what would have failed during a standard 5V test will fail sooner at higher voltages and can be detected using current methods.

Conclusion

In conclusion, the chemical mechanisms occurring on an SIR coupon that contribute to the measurement are not linear, and blindly applying current standards when testing at higher voltages may be detrimental. Understanding these mechanisms with various contaminants will be key to determining applicable test parameters; however, it is important to note that although they might not be applicable, the current parameters do appear to bound the failures. For improved testing at shorter times, voltage-dependent testing will be required.

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Water Quality Matters

A novel approach leverages ion exchange technology with continuous monitoring for superior tank management.

by CHRISTOPHER T. RILEY

Aqueous cleaning operations in printed circuit board population require particular attention to water quality. Various soils – internal and external to the population processes – need to be removed to a very high degree to ensure trouble-free operation of the circuit board. The water used for the makeup of the cleaning solutions and rinsing must also be of very high quality to minimize the potential for contamination of the circuit board, with ion exchange technology being the technology of choice to purify and recover the water.

The quality of printed circuit boards, their operating characteristics, and ultimately, their lifespan depend on several factors, with one of the more important factors being the cleanliness of the boards. Several soils, if not removed, can negatively impact the operation of circuit boards. Incomplete removal of solder flux residue, for example, can lead to corrosion and potential short circuits. Aqueous cleaning chemicals may contain various additives (such as saponifiers, surfactants, etc.) that aid in soil removal but must also be completely removed from the PCB, as failure to remove these cleaning chemicals can lead to the formation of residual spotting on the board.

Water, used for aqueous cleaning chemical makeup, as the cleaner itself, or for rinsing, is a critical component of the circuit board cleaning process. The water must be clean enough so that it does not leave any residue on the board after the cleaning process. City water typically contains background ions, such as calcium, magnesium, sodium and potassium that, if not removed (along with corresponding ions such as chloride, nitrate, phosphate and sulfate), can deposit and cause spotting or otherwise leave residue on a board after drying. Removal of these background ions before using the water in the PCB cleaning process is imperative to obtaining a contamination-free (or as close as possible) product.

Water Quality

Water quality for board cleaning operations is typically expressed in terms of conductivity, resistivity or total dissolved solids. Conductivity is the ability of the water to conduct electricity and is usually expressed as "microsiemens/centimeter" or "ìS/cm." Resistivity, or the ability of the water to resist conducting electricity (and the inverse of conductivity), is typically expressed as "Megaohm-centimeter" or "MΩ-cm" – commonly abbreviated as "megohms." Total dissolved solids (TDS) is a measure of the total number of ions in solution and is normally expressed as "milligrams per liter" or "mg/L" or "parts per million," or "ppm." To relate these terms to the measurement of water quality, quality increases (contaminant concentrations decrease) as conductivity and TDS

decrease and as resistivity increases; an example of this is shown in **Table 1**.

Table 1. Water Quality Comparison

Parameter	Units	Measurement			
TDS	mg/L	50	5	0.5	0.028
Conductivity	µS/cm	100	10	1	0.056
Resistivity	MΩ-cm	0.01	0.1	1	18
		→ Water Quality Increases →			

Since the purpose of cleaning and rinsing PCBs is to remove soils and minimize residual contaminants – including those from the water itself – it makes sense that higher-quality water is required. Water quality requirements vary – sometimes greatly – for board cleaning applications, typically ranging from 1MΩ-cm to 18MΩ-cm.

Water Treatment Processes

Several common treatment processes are employed to increase the quality of water used to clean PCBs. These processes include filtration (removing particulate or suspended solids), softening (removing hardness from calcium and magnesium), carbon treatment (to remove organic compounds), reverse osmosis (removing virtually all divalent and most monovalent cations) and deionization (removing all ionic components). Which processes are employed depends on the characteristics of the water requiring treatment as well as, typically, the size of the required water treatment system.

Of the treatment technologies listed, only deionization, most often achieved using ion exchange technology, can achieve the required water quality of greater than 1MΩ-cm. Neither filtration nor softening reduce the TDS, and reverse osmosis (RO) can only partially remove TDS – but not to the level typically required for RO alone to be used as a means of deionization. Filtration, carbon adsorption and RO are, however, often used as pretreatment for ion exchange treatment.

Ion Exchange Technology

Ion exchange technology uses polymeric beads that have been functionalized to remove either cations (positively charged ions such as calcium or Ca^{+2}) or anions (negatively charged ions such as sulfate or SO_4^{-2}). Processing water through a bed of mixed cation exchange resin and anion exchange resin (a "mixed bed") results in the removal of essentially all the charged species in the water and can produce water quality up to 18MΩ-cm.

Ion exchange is a mass-loading-limited technology in that the resin has a finite exchange/loading capacity that, when reached, must be replenished through regeneration or replacement. This finite capacity also means that the throughput – how long the resin lasts in the service cycle – is directly related to the concentration of ions in the feed water. The lower the ionic concentration (lower TDS) in the feed water, the longer the resin lasts in service.

Ion exchange technology is deployed either through a service or as a fixed system at the end user's site. In the service

deployment, tanks of ion exchange resin and activated carbon are leased by the end-user and, when depleted, returned to the supplier for regeneration and processing. In the fixed system, tanks of ion exchange resin are fixed in place at the end user's facility and regenerated in place, necessitating the storage, use and treatment/disposal of acid and caustic chemicals.

Ion Exchange Treatment for PCB Wastewater

PCB cleaning may generate two types of wastewaters – a dilute rinsewater and a more concentrated cleaning waste. Ion exchange technology is well suited to the treatment of the dilute circuit board cleaning rinsewater, either for removing regulated metals (such as lead) to meet discharge limits or to recover the water for use back in the process or elsewhere in the facility.

PCB cleaning rinsewaters are especially attractive for recovery/reuse given their typically low TDS levels. One also must be cognizant of the organic content of the rinsewater (typically measured as total organic carbon, or TOC), as well as the suspended solids (typically measured as total suspended solids, or TSS) as both types of contaminants can greatly impact the successful recovery of rinsewater to the required quality.

A typical ion exchange system used to recover circuit board cleaning rinsewaters consists of:

- Cartridge filtration to remove TSS (dirt, dust, debris, solid flux residue)
- Activated carbon to remove dissolved TOC (cleaner and flux components)
- Mixed bed ion exchange resin to remove TDS (cationic and anionic elements).

An example of a typical ion exchange water recovery system is represented in **Figure 1**.

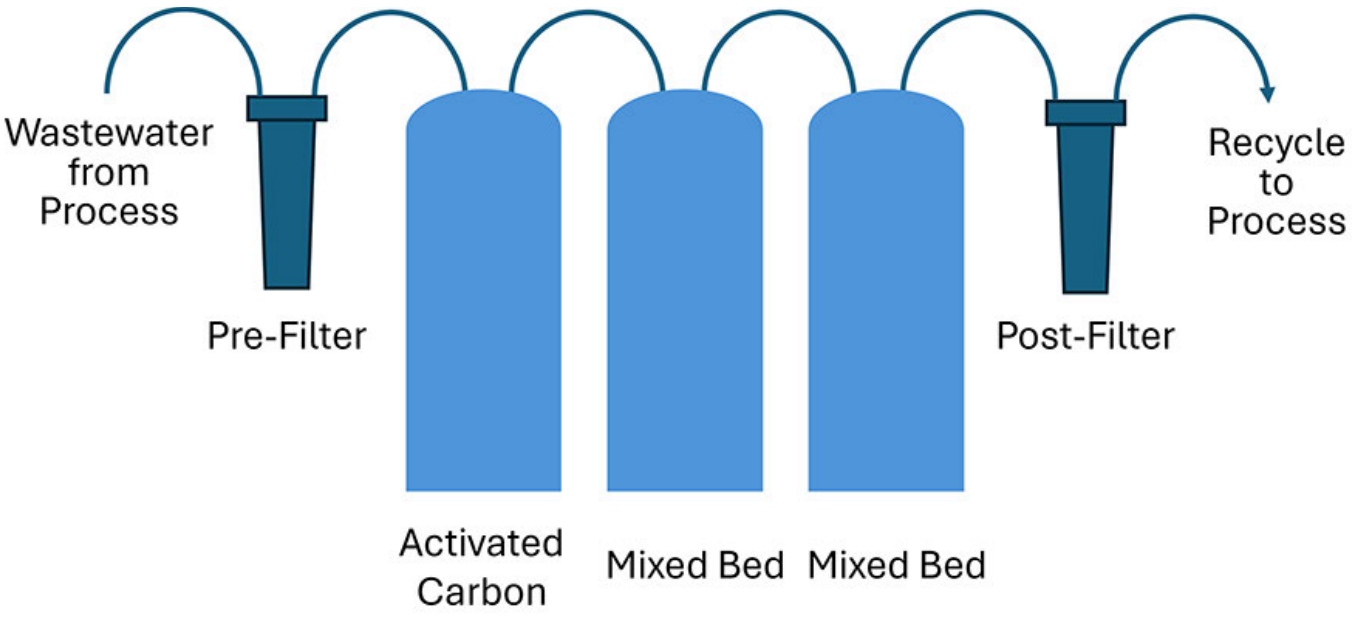

Figure 1. A typical ion exchange treatment system.

Smart Technology to Maintain Recovered Water Quality

Typical ion exchange wastewater recovery systems are set up in a worker-polisher (two mixed bed tanks in series) configuration and monitored manually, with treated water quality being measured with either in-line resistivity monitors or "quality lights." The resistivity monitors provide a resistivity number directly (or convert mathematically to TDS) while the quality lights show "green" if the resistivity is above the light's setpoint or "red" if it is below the light's setpoint. Based on these readings, in a service exchange system, tank changes are initiated by the user notifying the supplier that a tank change is required. Another option typically employed is to change tanks on a timed basis, before they are spent, regardless of the monitoring results – the assumption being that maintaining recovered water quality outweighs the cost of changing tanks before they are spent or exhausted.

A novel process, called Water One WX, combines traditional service wastewater ion exchange with remote monitoring and data logging capabilities. The system, monitored 24 hours per day by a centralized control center, measures several key wastewater performance parameters including flowrate, feed water conductivity and resistivities from both the worker- and polisher-mixed bed exchange tanks. When the worker-mixed bed quality drops below the specified setpoint, an alarm is sent to the control center who then initiates an exchange of the mixed bed tank with the supplier's service network. Before the tank exchange, the "polisher" tank ensures that the ion exchange system is providing the necessary water quality required for the cleaning process while relieving the end user of routine monitoring activities and responsibility to initiate tank exchanges.

The novel system, shown in **Figure 2**, does more than track ion exchange effluent quality. In addition to the water quality parameters previously noted, the system also measures and logs feed water temperature and differential pressure across cartridge filters while also monitoring the system for leaks. Alarms are also sent for negative deviations from these parameters which will trigger service events.

Figure 2. A Water One WX unit.

The novel unit compiles the water quality data collected, and the predictive analytics estimate the consumption of the worker mixed bed and forecast the remaining tank capacity. The historical data, including the performance cycles of previous mixed bed tanks, are stored and can be retrieved for evaluation and comparison to support user facility audits and to assist any troubleshooting efforts. All the relevant operating data are accessed via the unit's dashboard, with a typical dashboard view shown in **Figure 3**.

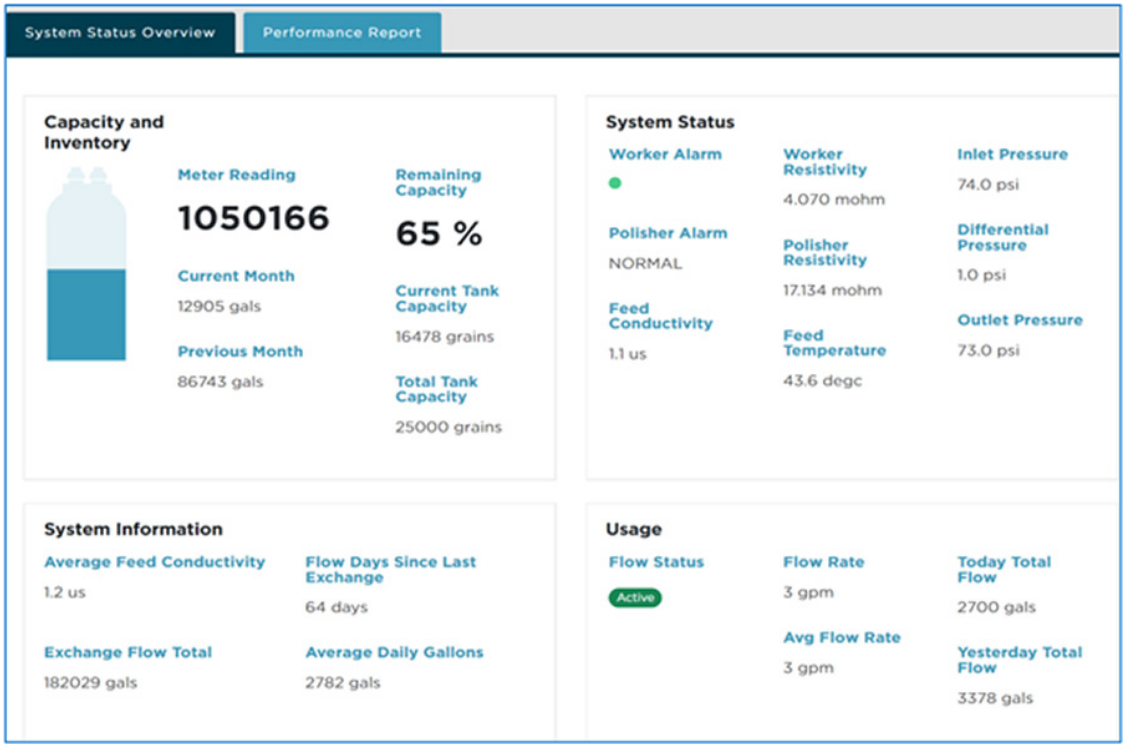

Figure 3. A typical dashboard view.

Case Study Examples

A microelectronics components manufacturer required high-quality rinsewater, greater than 16MΩ-cm, for cleaning its flexible circuit boards. A service-based ion exchange system was installed consisting of cartridge filtration, activated carbon and mixed bed ion exchange resin. The system was monitored manually, using a system of quality lights, with tank changes initiated by the customer when the quality lights indicated that a change was necessary. The system was converted to the novel system, which relieved the customer from both monitoring tank effluent quality and calling in for required tank changes. Between the remote monitoring and subsequent identification (and elimination) of a regular – but previously unknown – conductivity spike (captured by the system as shown in **Figure 4**) caused by a cleaner discharge into the system, mixed bed tank usage was reduced by 30% on an annual basis while maintaining the quality necessary for the company's process.

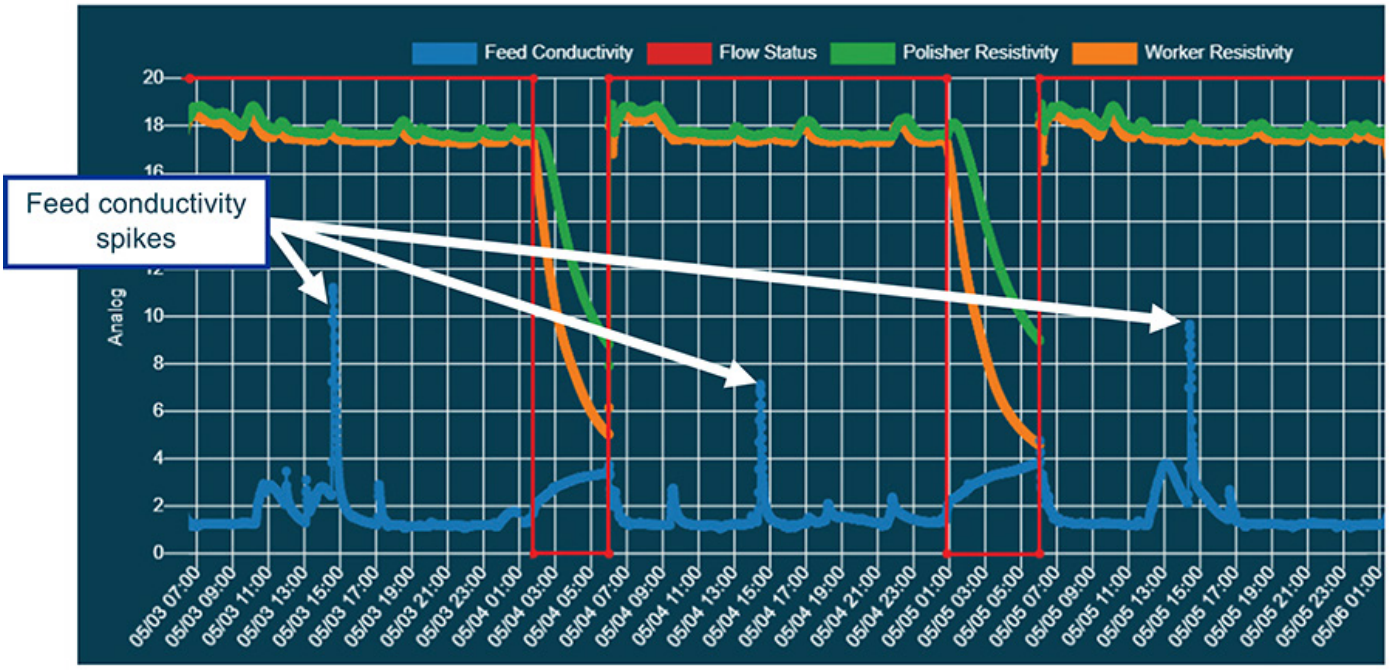

Figure 4. A Water One WX water quality chart showing a daily conductivity spike.

Another manufacturer and assembler of rigid PCBs installed a similar ion exchange system to treat and recover the rinsewater from its finished circuit board washing process. In this application, tank monitoring was initially minimized by performing regular mixed bed tank exchanges based on time, which ensured that the recovered water quality was maintained but did not utilize the full capacity of the ion exchange resin. The system was converted to the novel system, and the resulting continuous monitoring permitted the required recovered water quality to be maintained while reducing annual mixed bed tank usage by 33% and relieving the customer of the time and effort of monitoring the water quality and calling in for tank changes.

Conclusion

Printed circuit board operation and lifespan is directly related to its cleanliness. The cleanliness of the PCBs is in turn directly related to the quality of water used for cleaning and rinsing. Ion exchange is a mature technology for producing and recovering high-quality, clean water for this process. A novel system takes the well-established technology of service ion exchange and couples it with remote monitoring of key water quality parameters to maximize usage of the ion exchange resin and minimize the need to monitor and maintain the system while maintaining required water quality for the process – allowing the user to minimize any concern about recovered water quality and concentrate on its core business.

CHRIS RILEY is technical services director for the Wastewater Ion Exchange (WWIX) business at Evoqua Water Technologies, now part of Xylem (evoqua.com); christopher.t.riley@evoqua.com.

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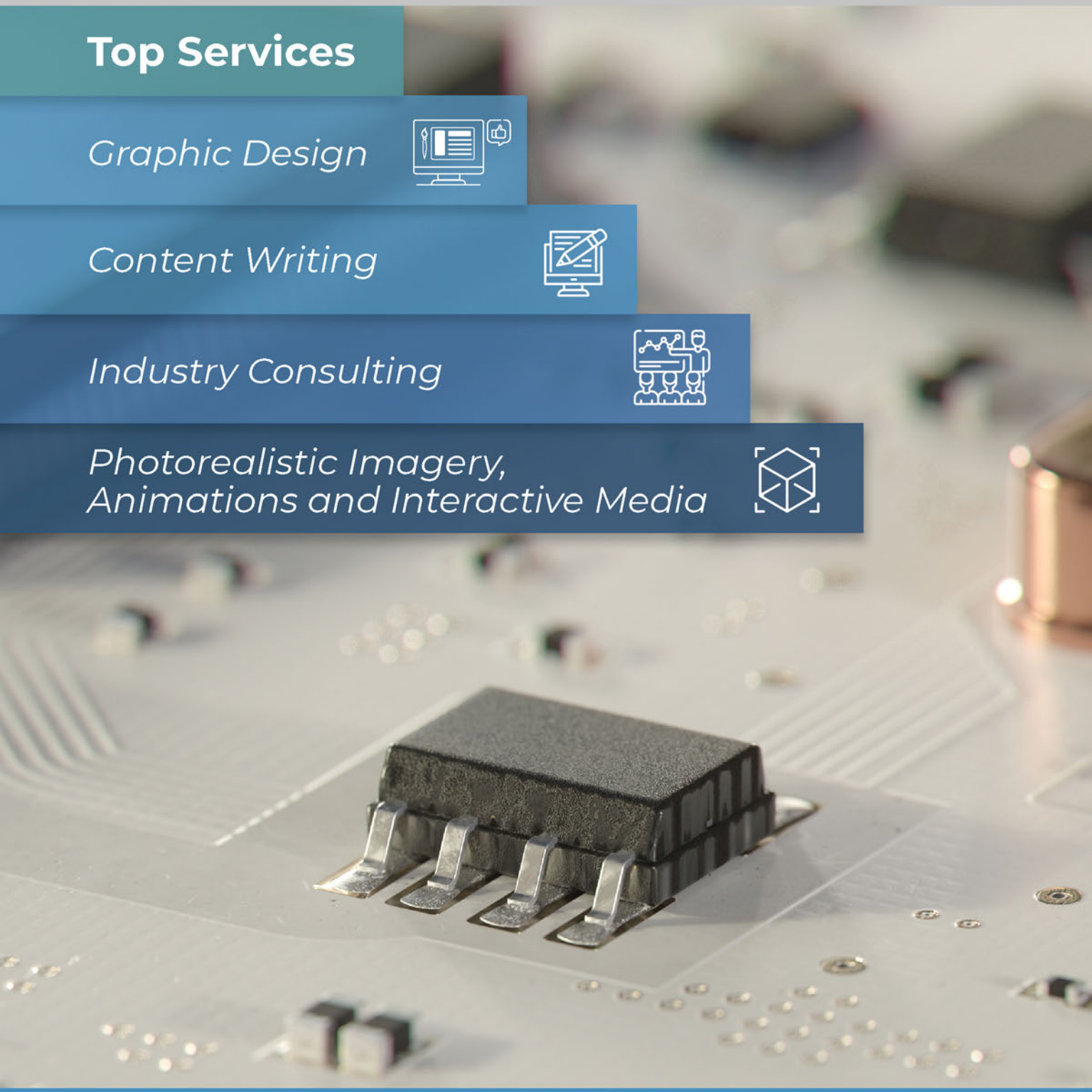

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BOARD QUALIFICATION

Identifying Solder Mask Problems with Simple Tests

Diagnosing sources of crazing, delamination and peeling.

by TIMOTHY O'NEILL

In printed circuit board (PCB) assembly, solder mask integrity is paramount. This protective layer, designed to shield the copper surfaces and prevent solder bridging between components, plays a crucial role in ensuring the reliability and functionality of electronic devices.

Solder masks can face several issues, however: crazing, delamination, peeling, and the presence of waxy or oily residues. These defects can lead to complications like micro solder balling, bridging, and solder snail trails, especially noticeable after wave soldering processes.

Not only do these challenges compromise the PCB's quality and long-term reliability, but they can also lead to significant production rework and increased costs.

Common Causes of Solder Mask Problems

Solder mask issues arise from several factors, ranging from the manufacturing process to the materials used. Some common causes include:

- **Inadequate surface preparation.** For a solder mask to adhere properly, the PCB surface must be clean and free of contaminants. Any residue or oxidation/moisture can significantly affect the mask's adhesion.
- **Incorrect curing.** Solder masks require proper curing to achieve optimal adhesion and durability. Undercured solder masks are susceptible to any liquids and can be easily damaged during the soldering process due to flux absorption and improper volatilization. Insufficient hardener in the solder mask's makeup can also cause it to never fully harden post-curing.
- **Solder mask porosity.** Solder masks can sometimes exhibit porosity depending on the type of solder mask used, the application process, and the curing process. Chemicals such as flux and cleaning agents as well as moisture could seep through these tiny holes. This can lead to reliability issues as well as corrosion or other damage over time.
- **Environmental factors.** The solder mask can absorb chemicals during PCB manufacturing, which may become highly hygroscopic or corrosive. When exposed to field conditions, these absorbed substances can

cause the PCB to experience failures due to the combined effects of humidity, heat and electrical stress.

Nearly all instances of solder mask delamination are related to the PCB itself, rather than to the flux or equipment used in the assembly process. If the solder mask shows visible damage or if oily or waxy residues are present, this could indicate issues with adhesion or improper curing of the mask, or potentially a combination of factors.

Other signs of a problem include solder snail trails, micro solder balling or bridging following the soldering process. Identifying and addressing these issues is crucial to prevent compromised PCB performance and integrity.

Test Protocols

Here are a few simple tests the engineer can do on the shop floor to help zero in on the root cause.

- **Adhesion check: the tape test.** This test involves applying a piece of transparent adhesive tape of at least 2" in length. Press the tape on the board and pull it up quickly at an angle approximately 90° degrees to the PCB surface **(Figure 1)**. If the tape pulls the mask off, it is a sign of an adhesion problem. The official IPC test method (IPC-TM-650, method 2.4.28) calls for 3M Brand 600 ½-inch (aka "Scotch") tape, but if that's not what's in your dispenser, use whatever is.
  If the mask lifts, observe the condition of the copper underneath. If the copper is shiny, it was likely not properly prepared for solder mask application. A matte finish indicates proper cleaning and roughing of the surfaces before mask application.

Figure 1. Tape test for solder mask adhesion.

Cure and hardness checks. Try the following three tests to check the curing and hardness of the mask.

- **Pencil test.** Use a freshly sharpened wooden pencil. Hold it at a 45° angle and press firmly away from you **(Figure 2)**. If the solder mask lifts or gouges, it is not sufficiently hard. This may be the result of improper curing or insufficient hardener added to the mask before curing.
  The pencil used was likely a #2H (we're all familiar with those from standardized tests). Pencils are graded on a hardness scale, and any graphite graded less than #6H should not gouge solder mask. A #6H or a complete kit of varying hardness pencils can be found at art supply stores.

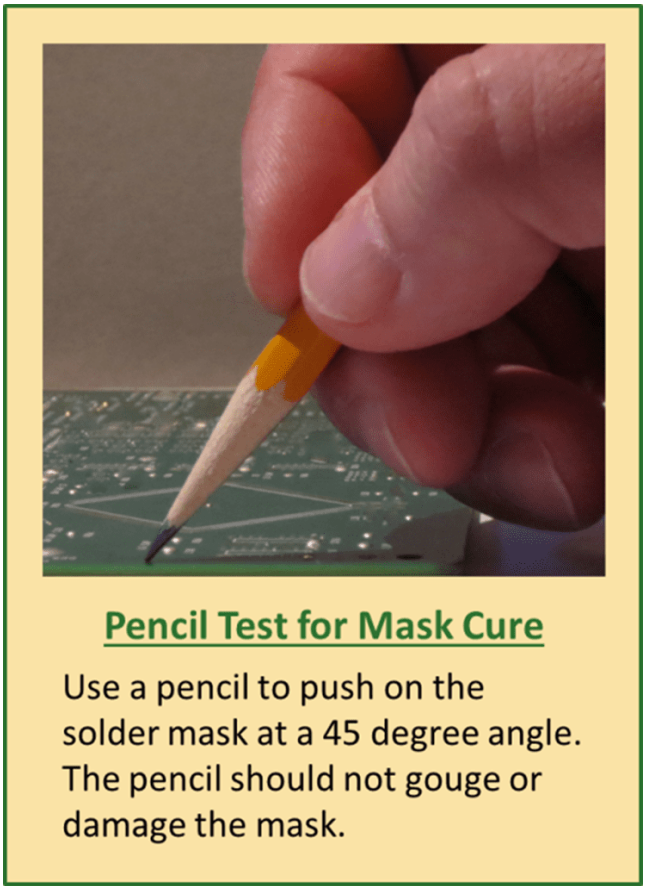

Figure 2. Pencil test for mask cure.

- **Bake test.** Conduct this test by placing the PCB in an oven preheated to 175°C and permit the board temperature to reach 155°C. Once at this temperature, maintain the board at 155°C for exactly 60 min. Ensure that the oven has adequate ventilation to remove any harmful fumes and plasticizers, preventing them from redepositing onto the solderable finishes, which could result in dewetting or poor wetting issues.
  If issues such as crazing, delamination, and the presence of oily or waxy residues are resolved after this treatment, it indicates that the solder mask was undercured, and the additional baking has helped complete the curing process.
  If the problems persist, however, this may suggest that the solder mask's formulation was incorrect, potentially due to an insufficient amount of hardener being added during preparation.

- **Solder mask check wipes.** These wipes are designed for a quick qualitative test to identify undercured

solder mask on PCBs. To use, remove a wipe from the package, ensuring the package is resealed. Rub the wipe on the PCB with moderate pressure for about 10-15 sec. in various areas.

If the solder mask is undercured, color from the resist will transfer onto the wipe, indicating issues with the mask's adhesion or curing **(Figure 3)**. If such a transfer occurs, it suggests the PCB may have defects and should be reported to the supplier for correction.

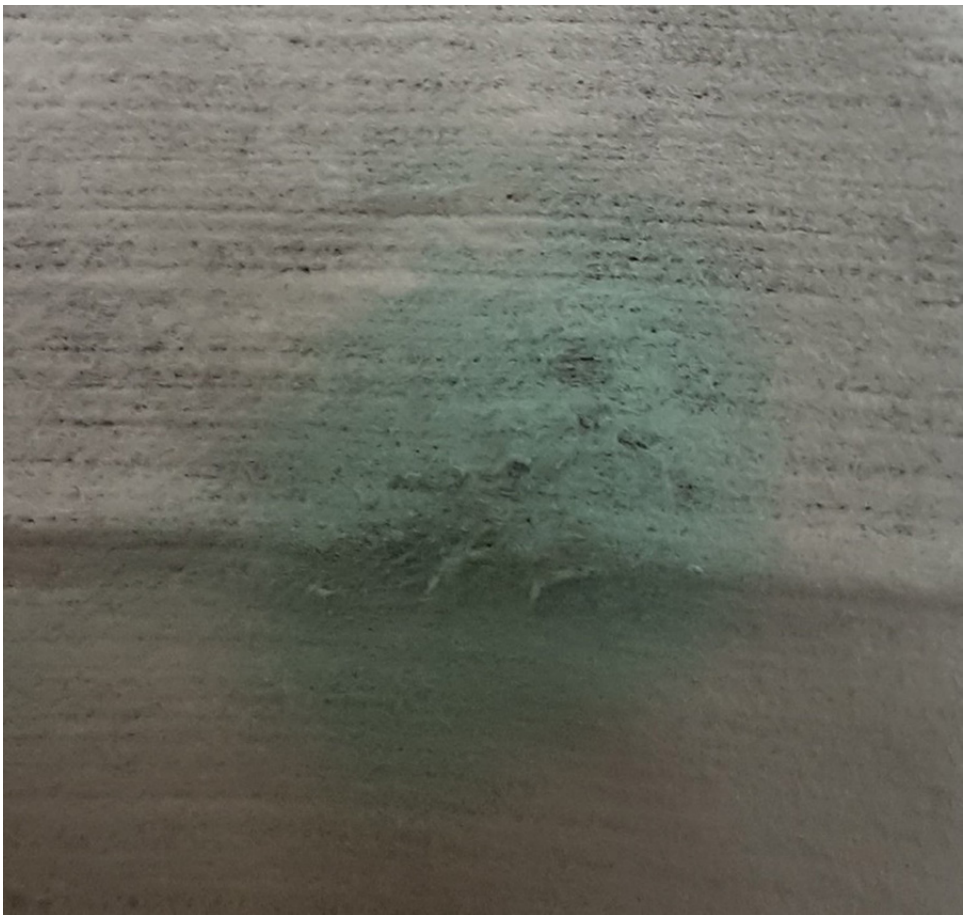

Figure 3. Greenish color deposited on a solder mask check wipe indicating a solder mask curing problem.

Case Study: How Flux Chemistry Can Exacerbate Solder Mask Issues

While solder mask problems typically stem from application issues which can be identified by the checks previously described, interaction between the mask and flux chemistry can also cause problems on rare occasions. Here we describe a situation in which the problem was at least partially flux-related.

In this case, a liquid flux seemed to be interacting with the solder mask, making it appear hazy and crazed, even lifting it from the substrate. The issue appeared to happen most frequently and severely around traces. A review of the wave solder process indicated no unusual steps, parameters, or exposure times that could cause solder mask damage, and the PCB fabricator insisted it was a flux problem.

Troubleshooting and testing. We asked the user to perform a few of the simple solder mask tests while we researched the flux lot number to determine any production changes or other customer concerns associated with it. No changes or concerns on record were found, but this particular flux was a highly specialized, small-batch material. We hypothesized that perhaps some variations could have taken place within its shelf life, so we tested a sample sent back from the user, but again found no issues.

Meanwhile, the mask failed both the tape test and solder mask wipe test. Further investigation of the mask and flux chemistries discovered that the mask was a newer, halogen-free product.

The mask's unique composition and lack of sufficient curing caused it to remain highly porous. As a result, the flux was absorbed into the subsurface of the solder resist, where it could not properly volatilize as expected during the preheating phase.

Once the board encountered the solder wave, the absorbed flux boiled between the resist and copper layers, undermining the adhesion between the solder resist and base copper traces. This information, coupled with the solder mask test failures, helped the assembler demonstrate the problem to its PCB fabricator and drive a resolution.

It's not unusual for the solder chemistry vendor to drive the root cause analysis of soldering issues. In fact, it makes perfect sense. The soldering technical support staff sees so many varied and different processes and problems, they are natural troubleshooters and a great resource for process engineers. Proper evaluation of material performance often relies on tests borne from the cause-and-effect knowledge gained only through experience.

TIMOTHY O'NEILL is director of product management at AIM Solder (aimsolder.com); toneill@aimsolder.com.

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Advantages of Automated Inspection

How does AI contribute to continuous improvement?

DEPENDING ON WHOM you talk to, artificial intelligence (AI) is likely to open amazing possibilities or lead to the end of humanity as we know it. The reality is that when appropriately used, AI eliminates a lot of repetitive tasks that have high levels of variation and cost when done manually. In the quality realm, this opens the door to a discussion about whether a truly automated inspection process is a non-value-added or necessary non-value-added activity.

Manual inspection is costly, and accuracy can vary widely among operators, the time of day the activity is performed, or even the day of the week the activity is performed. Quality philosophy has long held that it is better to prevent defect opportunities (quality assurance) than to try to inspect them out (quality control). If a printed circuit board assembly (PCBA) can be 100% visually inspected by machines during SMT and secondary assembly processes without significant throughput time, however, does it make sense to do so? Let's look at the pros and cons:

Potential benefits include:

- Faster identification of defects earlier in the process, which translates to less rework activity to address the issue
- Inspects against a standard that improves as the machine learns from past experiences
- A check and balance against defects unlikely to be caught in test, which pays for itself when considered against the cost of field failures and customer returns
- Inspection of a PCBA that takes 2-3 min. manually is less than a minute by machine.

Potential disadvantages include:

- Requires machine time and engineering resources
- Won't detect component failures or identify issues in hidden solder joints, so additional testing remains necessary to ensure no defects escape the factory.

At lower volumes, the 100% inspection strategy is unlikely to justify costs. At higher volumes, however, the costs of even a small percentage of returns improves the cost equation. AI tilts this benefit even further by increasing the inspection complexity that a machine can perform. This enables inspection beyond components and solder joints.

In 2022, SigmaTron International's facility in Tijuana, Mexico, began exploring the best way to automate inspection and integrate the captured data into real-time corrective action throughout its entire PCBA assembly process. A July

2022 PCD&F/CIRCUITS ASSEMBLY column, "An Industry 4.0 Approach to Employing 3-D AOI on an SMT Line," discussed the journey of integrating Industry 4.0 capabilities in a Lean Six Sigma framework in this facility's SMT area. A September 2023 PCD&F/CIRCUITS ASSEMBLY column, "Continuous Improvement and Mass Inspection," looked at the challenges of replicating automated inspection in secondary assembly operations.

The initial goal in utilizing 3-D AOI in secondary assembly operations wasn't to do 100% mass inspection. Instead, it was to focus on the projects with the lowest yields to drive a continuous improvement effort to reduce defect opportunities. As the machine's manufacturer upgraded AI module software capabilities, however, it became apparent that more complex inspections were possible, and implementing a 100% automated inspection process was less costly than having manual inspections on areas of the PCBA not traditionally inspected by AOI.

While the end goal is to expand the 3-D AOI's ability to inspect 100% of the board, new inspection steps are being added based on yield trends and customer feedback. For example, labeling issues prioritized the creation of an algorithm designed to verify that not only were labels correctly placed, but also that the correct characters were in place on each label. The normal process for label inspection is just to read and keep information in the database. There were no parameters set to check for the correct information and characters.

Working with the machine's manufacturer, the engineering team created an algorithm that checks keywords such as the correct part numbers and the correct quantity of characters. If the program detects any inconsistencies, the test stops and sends a message.

The team utilizes the C# programming platform to create each new algorithm. Once the machine begins inspecting to the new parameters, production operators or the engineering team can fine-tune based on yield trending. The machine learns from corrections as false calls are identified. Over time, it analyzes its library to determine whether images fit the parameters and will query the operator on situations where clarity is needed. Once the number of false calls drops significantly, it will query to see if the improved parameters can be transferred to other machine libraries, making propagation across equipment easy.

Inspecting in secondary assembly is still more challenging than in SMT. For example, components added in secondary assembly may be too tall for the vision system. The shape of some PCBAs can also create vision system issues. In these cases, changing camera placement or programming can solve the issue.

Broadening the scope of inspection to include elements of the PCBA not traditionally checked by automated mass inspection equipment doesn't actually add an inspection step. Instead, it increases the benefits of the inspection step in terms of the number of items inspected. At the same time, broadening the inspection parameters also broadens the available yield trending data, improving continuous improvement teams' abilities to quickly identify areas of needed process improvement and initiate corrective action.

FILEMON SAGRERO is continuous improvement engineer at SigmaTron International (sigmatronintl.com) and a Six Sigma Black Belt; filemon.sagrero@sigmatronintl.com.

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The PCB Podcast

SEEING **IS BELIEVING**

The Merchants of Menace

The names may change, but the (unwanted) pitches stay the same.

AN UNWANTED CONSTANT in my life is weekly unsolicited queries, like this:

Hey Robert,

With just one signature, I could wire you $10,000,000 if you were willing to sell your company.

I sent you an email Wednesday explaining that ***we have set aside $100,000,000*** *to buy electrical companies.*

We've already bought five companies from this fund and we expect to spend the entire $100,000,000 by the end of 2024.

To find out how much your company is worth and receive an offer of $10 million or more before our fund runs out, please book a call with the link provided below.

Best,
Chad

So attentive, that Chad. Except for the "Hey" part. And the "electrical companies" part. Could be about us; could just as easily describe someone who installs conduit and junction boxes in houses. It's doubtful the guys with the call lists and spreadsheets and quotas know the difference. Or even care.

One week later, in comes this:

Robert,

My name is Dylan, and I am looking to acquire an exceptional company from a transitioning owner. I came across your firm as I was researching the PCBA testing space in California and was impressed with the business you've built. As you look to the future – have you thought about what's next for you, and for your company?

It takes years of dedication to build a company and take care of your employees and their families. I've positioned myself to protect your hard work and legacy for years to come. Do you have 15 minutes this week to discuss your company's next phase of growth?

Best,
Dylan

P.S. To be respectful of your time, I am looking to invest in a business with at least $1.5 million in pretax profit. I am also considering smaller businesses that could quickly grow to that scale. Just send me a quick "no thanks" so I don't send a follow-up note.

"Transitioning owner." Sounds disturbingly like a dead person? Maybe someone moving to a higher level of consciousness in the "PCBA testing space?" What are they teaching kids in school these days?

Then there's that tiresome term "scale." Techie/libertarian cruising altitude-nirvana mashup. Hard to define, but those who know (they're special) know it when they reach it. All cares fade away to insignificance, as net worth makes all things whole, and one never has to apologize.

Extra points for not using "Hey" in the salutation. Nice to know he's done his homework and concluded we're exceptional.

Then there's this:

Robert,

I am a mergers and acquisitions facilitator at Obnoxious Advisors LLC, and I focus on the manufacturing industry.

I am an expert at matching family-owned businesses with strategic financial partners to either grow or sell their business. Our company specializes in experts who use only the first-person singular.

After reviewing publicly available data about your company, I believe it is a good fit for an M&A transaction. I have close relationships with well-funded and active buyers in the industry. They are looking for companies that generate at least $500,000 in EBITDA, where the owner is willing to stay for at least a transition period (one to two years), or for the long run (five to seven years). We favor owners with single-syllable first names: I trust their evaluations; they are my kind.

Under the right terms and at the right price, I hope you would entertain a sale of your company?

Can we schedule a discovery call early next week?

I await your expected response, as the world revolves around us.

Chip (I/me/mine)

Vowell Partners Ltd.

This one is laser-focused (as only a person fond of the pronoun "I" could be) on the manufacturing industry, singular.

Certainly not focused on grammar? (sic)

Some adopt the disarming, faux-familiarization approach:

Hi Rob,

This is Evan from Narcissistic Capital. I just left you a voicemail, and I wanted to provide some context as to the purpose of the call.

I am working closely with my colleague Brad Sheepskin, on behalf of a client of ours active in the NDT space. We are looking for a company that we can use as a platform to grow and scale.

Your company is a top priority for us as our client has specifically asked to connect with you. We would love to discuss in more detail and answer any questions you have.

Let us know a few days/times that work for a quick conversation, and we will send over a calendar invite with a meeting link.

Looking forward to speaking with you.

Kind regards,
Evan Birdsong

Just the kind of guy you'd want to cut a deal with over a few beers in a sports bar. Or in the vacuum of NDT space, where no one can hear you negotiate. He does provide context, free of charge. What would life be without context? Just growing and scaling, I guess.

Or this:

Hi there, Robert,

Have you been thinking about selling your company?

Are you a baby boomer ready to move on?

Asking because I'm personally looking to buy a business where I can utilize my years of marketing experience to take your good, solid, well-run company to the next level.

(FYI, I am NOT a business broker; this purchase is for me.)

IF:

- *the business isn't dependent on just you (meaning you've got a good team of people that can run it w/o you)*

- *sales are between $1 million to $10 million*
- *you're the type of entrepreneur that cares about their employees, customers & suppliers*
- *you haven't listed your business with anyone*

*And **IF** my questions have hit the mark, we should have a conversation.*

Interested in a quick call?

Regards,
Nick

Gatsby Capital

Dearest Nick,

Thank you for your good, solid, well-run sales pitch. Yes, you'll be relieved to know I am thinking, although selling my company is not foremost in my thoughts. Yes, I am a Baby Boomer, ready to move on (from your appeal). As we have already arrived at the next level (without benefit of your years of marketing experience), we'll suffer through the privations of what might have been, had we met and hit the mark with you earlier. Such is life. Parting is such sweet, etc., etc.

Patterns emerge: Ignorance, "space," or "graduation project." Each approach falls into one of these three categories.

First: ignorance.

Chad, in the first letter, indicates he has $100 million on hand to buy "electrical companies."

As noted, he confuses electronics with electricians. The first write code; the latter meet code.

To them, it's just another business, and ignorance of fine distinctions is bliss. As long as it generates $1.5 million in annual EBITDA.

Then there's "space," as in, "I was researching the PCBA testing space in California …."

The testing space: the Final Frontier. Expand your mind, chemically or exponentially.

Our fourth friend Evan professes to represent a client "active in the NDT space."

What does "active" mean?

Burglars are active in the household space. Embezzlers are active in the financial space. Astronauts are active in the Space space. Politicians and marketing geniuses are active in the vapid space.

What's in that space for me?

Last, the graduation project. In our final example, Nick appears to reprise his master's thesis in business school. He seems prepared to deploy family money in a quest to make something of himself beyond video gaming, justifying his parents' eye-watering tuition expenditure, and confirm if the gibberish on the white board in the lecture hall actually has real-world validity. The theory needs testing, and Junior needs a job. Because in theory, there is no difference between theory and practice. In practice, there is. Hence, we're the Lab Rat, and Junior avoids delinquency, on our time. You're welcome, parents.

Five years of weekly appeals to my greed lead me to risk some observations: 1) The players change, but the script is the same; 2) the players themselves are dilettantes, often with little to no operating or technical knowledge of our business or industry; and 3) it's a repackaging process, in which the acquirer hopes to bundle enough assets to make the bundle yet again attractive to the next sucker, er, buyer. To the very few who are lucky go the spoils and a placid retirement. To the rest ….

The paradox is that many who drive this process, who have never organized an entrepreneurial endeavor in their lives, are called Masters of Business Administration. The thought turns the stomach.

Two of my best industry friends responded positively to a similar enticement several years ago. They weren't looking for a takeover relationship (I refuse to say "exit strategy"), but there it was. These things sometimes materialize when you least expect them. The offer was too good to pass up, so they gulped hard and took it, signed the one-year contract, hoping the omniscient acquirers would come through according to the promises they made during cocktails and courtship. Promises to make capex investments; add staff; add marketing; scale up the business, while preserving the infrastructure, talent and tribal knowhow my friends shed blood, sweat, and passion for over 28 intense years of building their pride and joy.

The bubble burst fast. Two years later, underinvestment, poor operating skills, and inattentive and incompetent management have done their work. Market share is down, customers are leaving. What remains of their legacy is memories.

It's our world.

And they don't care.

This is dedicated to Regina, my Editor from Eternity. Today, always, and forever. I owe everything I am to you: I'm a better man for knowing and loving you. I hope, with your guidance and approval never far away, to do something good with myself, and for others, in your honor. My best and my love, always.

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.


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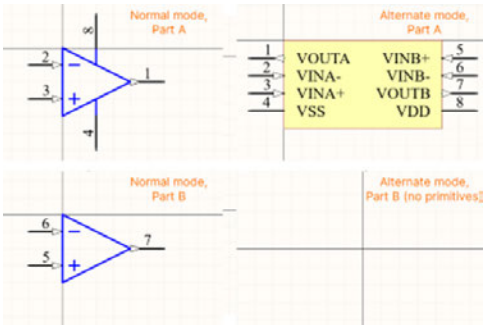


ALTIUM DESIGNER 24.6 ECAD

Altium Designer 24.6 PCB design software now includes the ability to disable automatic updates of drill symbol data. Adds support for the placement of components onto a substrate when footprints contain not just standard pads but also solid regions or fills, enabling the placing of components with more complex-shaped footprints onto substrates, including RF shapes (e.g., antennas). Adds the ability to route along more “natural” lines on the surface of the 3-D substrate by using the new “UV” plane kind for the alignment grid. Rather than the more rigid grids generated using traditional XYZ planes, the UV plane generates a grid based on the surfaces of the substrate, providing more natural gridlines that follow the substrate curves. Now imports designs created using KiCad v. 7 or 8 ECAD.

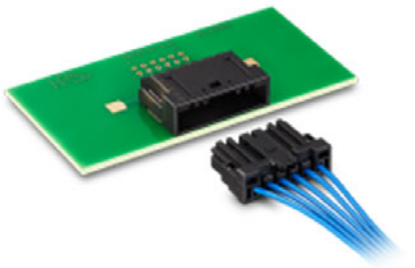
Altium
altium.com

HI-PRINT SD11 INKJET PRINTER

SD11 inkjet printer is a flexible, scalable, modular and reconfigurable system designed for PCB manufacturing. Features flexible configuration capability for three solder mask colors, or two colors plus legend or any other

combination. Also features modular architecture with up to 10 printheads, reportedly creates no waste, and includes integrated printhead maintenance system. Other features include higher NPI and grayscale industrial precision printing, traceable code printing and product ID, and multi-CCD positioning, plus a robust gantry system and a small footprint.

Hi-Print
hi-print.com



HIROSE ZG05HV SERIES WTB CONNECTOR

ZG05HV series wire-to-board connector supports applications up to 125°C, for automotive applications including battery, converter, ECU, inverter and on-board charging connectivity. Features a specialized housing that delivers sufficient creepage and spatial distance between contacts, enabling a high-rated voltage (1,000V) and withstanding voltage (3,000V) in a compact size. Is 0.5mm in size and has a pitch of 3.3mm, enabling space-savings and high performance without compromising reliability. Features a three-point contact design (one spring and two embossed contact points) combined with a double-layered spring to increase contact force and prevent vibration from outside, enhancing reliability in high vibration conditions. Deep contacts within the housing eliminate risk of electric shock during assembly.

Hirose Electric
hirose.com

KICAD V.8.0.4 ECAD

KiCad version 8.0.4 printed circuit design software contains critical bug fixes and other minor improvements since the previous release. Adds sorting to library tree columns, fixes issues in the schematic editor, spice simulator, symbol editor, board editor and more.

KiCad
kicad.org

STACKPOLE RPCA-UP RESISTOR SERIES

RPCA-UP series of resistors now features a 0603 chip size. Offers a 0.33W power rating, where the standard for this size is typically 0.125W. Is AEC-Q200 qualified and is said to deliver exceptional pulse handling thanks to proprietary materials, design and manufacturing processes. Has demonstrated outstanding performance in all AEC-Q200 tests, improving expected failure rate by a factor of at least 10 compared to general-purpose resistors. Offers anti-sulfur performance, passing ANSI/EIA-977 sulfur test with minimal resistance shift at 105°C.

Stackpole Electronics

seielect.com

TELEDYNE LECROY T3AWG6K SERIES AWG

T3AWG6K series high-performance arbitrary waveform generator is for use in a stimulus-response model with the company's high-definition digital oscilloscopes. Offers sample rate up to 12.32GS/s in RF mode, 16-bit vertical resolution, up to 5Vpp output voltage and ±2.5VHW baseline offset, 4Gpts waveform memory per channel, and up to 32 digital channels in sync with analog generation.

Teledyne LeCroy

teledynelecroy.com

TELEDYNE LECROY WAVEMASTER 8000HD OSCILLOSCOPES

WaveMaster 8000HD series of high-definition oscilloscopes now features eight models designed for all stages of product development. Are available in both WaveMaster and SDA variants and offer bandwidths of 6-65GHz. Are said to feature signal characterization performance, validation and debug capabilities, and comprehensive serial data expertise.

Teledyne LeCroy

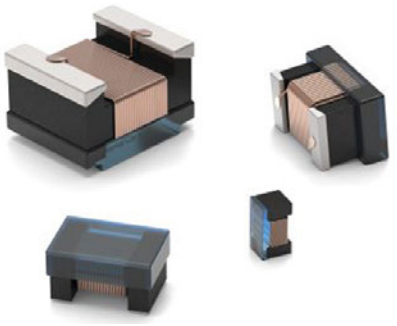
teledynelecroy.com

VISHAY CHA SERIES RESISTORS

CHA series of AEC-Q200 qualified thin-film chip resistors provide high frequency performance up to 70GHz for automotive, space, avionics, telecom and military applications. Is offered in the compact 02016 case size and is available in a wide range of resistance values from 10-500Ω. Are said to offer low internal reactance and exhibit behavior close to a pure resistor over their frequency range, with a nearly flat Z/R curve to 70GHz. Maintain frequency stability after AEC-Q200 tests – validated by their ΔR and Z/R measurements – for performance under harsh environmental conditions. For automotive ADAS, LIDAR, connectivity, and 4-D radar systems; LEO satellites and space communication systems; military guidance and telemetry systems; drones; and RF antennas. Provide limiting voltage of 30V, rated power of 30mW at +70°C, and a temperature coefficient of ±100ppm/°C, with ±50ppm/°C available on request.

Vishay Intertechnology

vishay.com

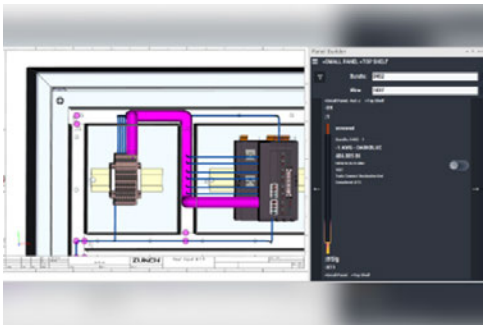


WÜRTH WIRE-WOUND FERRITE SERIES

WE-RFI series now comes in sizes 0402 and 0603, and can be used as inductors for HF applications or as ferrites for interference suppression. Are said to be suitable as low-pass filters (for filtering high-frequency noise), data line filters, supply voltage decoupling, low-frequency radio applications and RFID. As wire-wound ferrites, can attain higher impedances than normal ferrites, even at high frequencies, and over a wider bandwidth while showing no DC bias behavior. As HF inductors, offer high inductance values from 20nH up to 47µH. Are characterized by low RDC and a high rated current of up to 1.91A at ΔT=40K.

Würth Elektronik

we-online.com



ZUKEN PANEL BUILDER 2025

Panel Builder 2025 for E3.series provides a digital solution to support manufacturing tasks such as exporting files for manufacturing equipment and supplying instructions to the operators to install the wires and cables. Replaces traditional method of uncontrolled electronic files and printed paper copies, eliminating installation errors. Automates creation of input data for manufacturing machines to reduce errors and material waste and features a simple user interface to speed up the learning process. Provides visually guided wire installation instructions to the shop floor through an easy-to-use interface, assisting operators in installing control panel wires, and provides electrical panel layout designers with a utility for creating detailed, step-by-step assembly and build instructions for panels, cabinets and electrical enclosures. Supports direct exports to wire processing machines from Schleuniger, Komax, and nVent and allows use of E3.panel's advanced algorithm technology with user requirements to

automatically route wires in the panel enclosure.

Zuken
zuken.com

CA

ITW EAE ELECTROVERT DEEP WAVE OPTION

Electrovert wave soldering machines now include a deep wave option that provides the ability to pump up to a 20mm wave height. The recipe-controlled parameter in the machine software can make changes between different wave heights within 10 sec. Provides flexibility for a lot-size-of-one capability in high-mix soldering applications, and has data logged in the machine software and captured for MES information management applications. Available with the UltraFill 4.0 and DwellMax 4.0 wave nozzle configurations and Auto-Exit Wing option and is offered in combination with short and full nitrogen tunnel options.

ITW EAE
itweae.com

MASTER BOND EP21ARHTND-2 EPOXY

EP21ARHTND-2 two-part epoxy adhesive is designed to withstand prolonged exposure to a range of chemicals. Is said to be a reliable electrical insulator with a volume resistivity greater than 10^{14}Ω-cm at 75°F, and dielectric strength of 440V/mil at 75°F for a 1/8-inch test specimen. Also features a tensile strength of 9,000-10,000psi, and a Shore D hardness of 75-85. Provides heat resistance and is serviceable from -60°F to +400°F. Is capable of curing at room temperature, but to optimize its acid resistance properties a cure schedule of overnight at ambient temperatures followed by a heat cure of 150-200°F for 2-4 hr. or longer is typically recommended. Contains no solvents and is RoHS compliant. Is said to bond to metals, ceramics, composites, rubbers and plastics, and features a smooth paste-like consistency and will not flow or sag once applied, for bonding and sealing applications.

Master Bond

masterbond.com

POLAR INSTRUMENTS GRS200 FAULT LOCATOR

GRS200 fault locator uses proven passive analog signature analysis and compares a faultless assembly with the board under test. Can detect typical faults in electronics production, service and repair quickly and without extensive circuit knowledge. Features analog signature hardware and powerful software with live signature analysis, program mode and CAD data display. Integrates circuit diagrams, assembly photos, repair reports and an optional digital multimeter. Imports more than 20 different formats CAD data, including GenCAD, HyperLynx, IPC-2581 and ODB++, and circuit networks can be graphically highlighted and the associated components displayed.

Polar Instruments

polarinstruments.eu

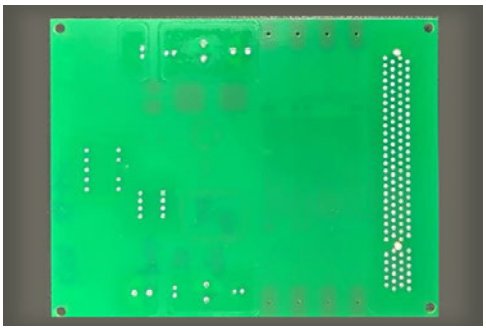
SAYAKA SAM-CT34NSL AUTO-DRY SLICER

SAM-CT34NSL auto-dry slicer is for mass production with high rigidity, precision cutting, and advanced human error prevention features. Offers versatile use, allowing selection between pallet or non-pallet-use depending on PCB shape. Is suitable for various production needs. User-friendly operation is facilitated by an easy program teaching interface via a touch-display, ensuring a simple and efficient setup process. Eliminates V-scoring, prevents sagging during reflow and maintains PCB integrity. Delivers a smooth finish, with cut face ground to perfection, enhancing quality of final product. Is said to minimize stress on PCBs, protecting components and ensuring reliability with more

than 500µm-strain. Optional visual confirmation feature permits cut lines to be confirmed by a monitor. Adjustable cutting speed optimizes efficiency for high-volume manufacturing environments.

Sayaka

sayaka.co.jp



SHENMAO SM-ZR10 FLUX

SM-ZR10 is a rosin-free no-clean liquid flux designed for automatic wave soldering processes. Is halogen-free and complies with RoHS, RoHS 2.0, and REACH, allowing it to meet the highest environmental and safety standards. Uses special organic activators to provide superior wettability and solderability, and is designed to comply with no-clean processes. Ensures a bright and full solder joint appearance, and rosin-free formulation makes related apparatus easier to clean and maintain, reducing downtime and improving overall productivity.

Shenmao America

shenmao.com

In Case You Missed It

Component Placement

"SimPLE, A Visuotactile Method Learned in Simulation to Precisely Pick, Localize, Regrasp, and Place Objects"

Authors: Maria Bauza, *et. al.*

Abstract: Existing robotic systems have a tension between generality and precision. Deployed solutions for robotic manipulation tend to fall into the paradigm of one robot solving a single task, lacking "precise generalization," or the ability to solve many tasks without compromising on precision. This work explores solutions for precise and general pick-and-place. In precise pick-and-place, or kitting, the robot transforms an unstructured arrangement of objects into an organized arrangement, which can facilitate further manipulation. The authors propose SimPLE (Simulation to Pick Localize and placE) as a solution to precise pick-and-place. SimPLE learns to pick, regrasp and place objects given the object's computer-aided design model and no prior experience. The authors developed three main components: task-aware grasping, visuotactile perception, and regrasp planning. Task-aware grasping computes affordances of grasps that are stable, observable, and favorable to placing. The visuotactile perception model relies on matching real observations against a set of simulated ones through supervised learning to estimate a distribution of likely object poses. Last, the authors computed a multistep pick-and-place plan by solving a shortest-path problem on a graph of hand-to-hand regrasps. On a dual-arm robot equipped with visuotactile sensing, SimPLE demonstrated pick-and-place of 15 diverse objects. The objects spanned a range of shapes, and SimPLE achieved successful placements into structured arrangements with 1mm clearance more than 90% of the time for six objects and more than 80% of the time for 11 objects. (*Science Robotics*, June 2024, https://doi.org/10.1126/scirobotics.adi8808)

Defect Detection

"Attentive Context and Semantic Enhancement Mechanism for Printed Circuit Board Defect Detection with Two-Stage and Multi-Stage Object Detectors"

Authors: Twahir Kiobya, *et. al.*

Abstract: Several methods have been proposed to detect PCB defects. Detecting significantly smaller and visually unrecognizable defects has been a long-standing challenge, however. The existing two-stage and multi-stage object detectors that use one layer of the backbone, such as Resnet's third layer or fourth layer, suffer from low accuracy, and those that use multilayer feature maps extractors, such as Feature Pyramid Network (FPN), incur higher computational cost. Founded by these challenges, the authors propose a robust, less computationally intensive, and

plug-and-play attentive context and semantic enhancement module (ACASEM) for two-stage and multi-stage detectors to enhance PCB defect detection. This module consists of two main parts, namely adaptable feature fusion and attention sub-modules. The proposed model, ACASEM, takes in feature maps from different layers of the backbone and fuses them in a way that enriches the resulting feature maps with more context and semantic information. The authors test their module with state-of-the-art two-stage object detectors, faster R-CNN and double-head R-CNN, and with a multi-stage cascade R-CNN detector on DeepPCB and augmented PCB defect datasets. Empirical results demonstrate improvement in the accuracy of defect detection. (*Nature*, August 2024, https://doi.org/10.1038/s41598-024-69207-8)

Microwave Circuits

"Frequency Shift in Microwave Circuits Manufactured with Circuit Board Plotters: Case Study of a Parallel Coupled Lines Filter"

Authors: Luigi Ferro and Emanuele Cardillo

Abstract: Board milling is one of the most widespread methods for manufacturing printed circuit boards from low frequencies to the microwave and millimeter wave range. In this work, the detrimental effect of defects typical of printed circuit board plotters has been investigated. In detail, a systematic frequency shift in the circuit performance has been observed both in terms of S21 and S11 parameters. The performance degradation has been analyzed and attributed to the inaccurate milling depth, which is typical of many plotters, particularly for less recent models. After the conductor removal step, the unwanted milling of dielectric material changes the electrical properties of the microstrip structure, in turn affecting the circuit performance. This circumstance has been investigated by means of electromagnetic simulations performed on the real case study of a parallel coupled lines filter. Therefore, a filter prototype has been realized and measured to confirm the simulated results. (*Electronics*, July 2024, https://doi.org/10.3390/electronics13153100)

Solder Alloys

"Intermetallic Compounds in Solder Alloys: Common Misconceptions"

Authors: David Hillman, *et. al.*

Abstract: Intermetallic compounds (IMC) or intermediate phases are formed between two or more metallic elements in many metal alloy systems. During soldering, an IMC is formed at the soldered interface as the molten solder reacts with an element in the substrate. IMCs also can form within the bulk solder as the joint solidifies. IMCs have critical roles in the solder joint quality and reliability. Unlike most metal alloys, an intermetallic compound typically has a fixed stoichiometry and is in variance with the conventional phases or constituents in the metal system (e.g., alpha and beta). IMCs have a different crystal structure than any of their constituents and some but never all the characteristics and properties of their constituents. Ductility is an important solder joint property, and the low intrinsic ductility of IMCs is associated with brittle behavior and reliability risk in service. A review of published

solder field failures shows little evidence that IMC properties or IMC evolution under service conditions reduce solder joint reliability, however. Most IMC-induced solder joint failures are found to result from incorrect material specification or uncontrolled soldering processes. This work describes the IMCs that occur typically in eutectic Sn63Pb37 solder and near-eutectic SAC 305 or other tin-based Pb-free solder alloys, including how they impact solder joint reliability. The work also describes the potential impact of IMCs on the solder joint reliability for the newest generation of Pb-free high-performance solder alloys. (*Journal of Surface Mount Technology*, July 2024, https://doi.org/10.37665/pmtrnw39)